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PROPULSION/FLIGHT CONTROL INTEGRATION TECHNOLOGY (PROFIT) DESIGN ANALYSIS STATUS

Christopher M. Carlin and William J. Hastings

Boeing Aerospace Company
Seattle, Washington

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National Aeronautics and
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16. Abstract

The Propulsion Flight Control Integration Technology (PROFIT) program is designed to develop a flying testbed dedicated to controls research. This document reports the preliminary design, analysis, and feasibility studies conducted in support of the PROFIT program.

The PROFIT system is built around existing IPCS hardware. In order to achieve the desired system flexibility and capability, additional interfaces between the IPCS hardware and F-15 systems are required. The requirements for additions and modifications to the existing hardware have been defined. Those interfaces involving the more significant changes have been studied in detail. DCU memory expansion to 32K with flight qualified hardware has been completed on a brassboard basis. The uplink interface breadboard and a brassboard of the central computer interface have also been tested. Two preliminary designs and corresponding program plans are presented.

Itis concluded that either system will provide the necessary flexibility and is feasible to build and operate. Specific recommendations are made relative to hardware, future work, and the assembler for DCU software.

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1.0 INTRODUCTION AND SUMMARY

This document reports preliminary design, analysis, and feasibility studies conducted to support development of the PROpulsion Flight control Integration Technology (PROFIT) program. It is the goal of the PROFIT program to integrate existing government owned hardware to create a flexible controls research flying test bed. This facility will provide for testing of:

- o Energy Management Systems
- o Engine Hardware - Sensors, Actuators
- o Engine Control Laws
- o Engine Health Monitoring
- o CCV Techniques - Canards, 2D Nozzles (Thrust Vector Control)
- o Control Redundancy Techniques
- o Fail Operational Systems
- o Aircraft System Integration Techniques and Architecture
- o Automated Plant Parameter Estimation Techniques

These goals have lead, after discussion and review, to the following hardware requirements:

- o Full authority digital electronic control of at least one engine,
- o Full authority thrust modulation capability in both engines,
- o All inlet control functions provided by PROFIT system,
- o Limited authority command capability to Flight Control System,
- o Data interfaces with pilot, central computer bus, telemetry uplink, and downlink,
- o Flexible design to minimize cost of implementing research programs,
- o System hardware/software configured such that total system is not flight critical.

A PROFIT system meeting these requirements may be adapted through software modification to support research in the areas outlined above. Separate research programs may be flight tested concurrently either through co-residence of related software or by time sharing the facility and changing software between flights.

Section 2 of this document presents, without justification, two preliminary system designs which have evolved as a result of studies and discussions during this contract period. The system first conceived emphasizes engine control and involves a lengthy sequence of engine ground tests. The second system emphasizes low cost and early research flight test activities. Many of the configuration selection decisions in these designs are a result of external events or underlying program philosophy and may differ substantially from common practice. Some of these factors are:

1. Bendix/P&WA are developing a set of full authority electro-hydraulic interface hardware for the F-100 engine independent of PROFIT.

2. The PROFIT system shall be configured to be non flight critical.

3. The system shall be as simple as possible consistent with being flexible and reconfigurable.

4. Government owned equipment consists primarily of a flight proven digital computer and DMA controller.* Modifications to this hardware will be limited to peripheral elements mated to it.

Since the computational capacity of the PROFIT digital computer unit (DCU), with 32K words of core memory, will tend to be cycle time rather than

*This equipment is a part of the Integrated Propulsion Control System (IPCS) Digital Propulsion Control Unit (DPCU) described in Reference 1.

memory size limited an extensive analysis of BØM engine control iteration rate requirements was performed. The study, documented in Section 3.0, showed that the engine control can be operated with a calculation interval of 60 milliseconds. It is necessary to perform a portion of the rear compressor variable vane (RCVV) control computation and update its command output at a higher rate to accommodate system dynamics at the high Mach number, low altitude flight conditions. Memory and computation cycle time estimates for typical research software configurations show that there is adequate margin for future programs. Inlet computation rate requirements will be assessed as soon as the inlet simulation becomes available.

The PROFIT system is built around existing IPCS hardware. In order to achieve the desired system flexibility and capability additional interfaces between the IPCS hardware and F15 systems are required. Section 4 documents the progress of design analysis and testing of these interfaces and additions to IPCS hardware. The requirements for additions and modifications to the existing hardware have been defined. Those interfaces involving the more significant changes have been studied in detail. DCU memory expansion to 32K with flight qualified hardware has been completed on a brassboard basis. The uplink interface breadboard and a brassboard of the central computer interface have also been tested.

PROFIT Program Plans were developed for both systems during the contract period and are presented in Section 5. Key aspects of the program, firm selection of test sites for example, are still fluid thus this plan is tentative. However, the tasks to be performed and their sequencing are presented in some detail.

It is concluded (Section 6.0) that either system will provide the necessary flexibility and is feasible to build and operate. Specific recommendations are made relative to hardware, future work, and the assembler for DCU software.

2.0 SYSTEM DESCRIPTION

The two systems discussed below were conceived and documented serially. Sections 2.1 - 2.8 document System A and Section 2.9 documents System B. Where convenient data presented in the System A discussion is referenced by the System B discussion.

2.1 SYSTEM INSTALLATION

Figure 2.1-1 depicts schematically the PROFIT system installation on the left hand side of the F-15. A similar system is installed on the right hand side. Differences in application and operation between the two sets of hardware are achieved through cabling and software differences. System elements are installed and tested sequentially to reduce risk, see Section 5. All black boxes are configured identically to permit interchangeability and reduce complications in configuration control. The following paragraphs describe the system elements in some detail.

Figure 2.1-2 depicts the physical location of system elements about the airplane. Since the Test Set Unit (TSU) is an integral part of the system during ground test it is included. With a few exceptions electronic boxes are mounted in the ammo bay to which cooling air is plumbed. The boxes, based on IPCS experience, are installed in a vibration isloated box which slides into the ammunition bay on existing rails.

The Electronic Air Inlet Control (EAIC) is removed and the inlet pressure transducers are installed in the space created. Based on IPCS experience with these transducers they are installed in a protective box providing vibration and shock isolation and electrical and pneumatic interfaces.

The Bill of Materials (BØM) inlet relay interlocks are retained in situ and interfaced with the IFU to provide the required test and backup functions. The BØM inlet actuators and their associated LVDT's interface directly with the Interface Unit (IFU) and are retained in their BØM configuration.

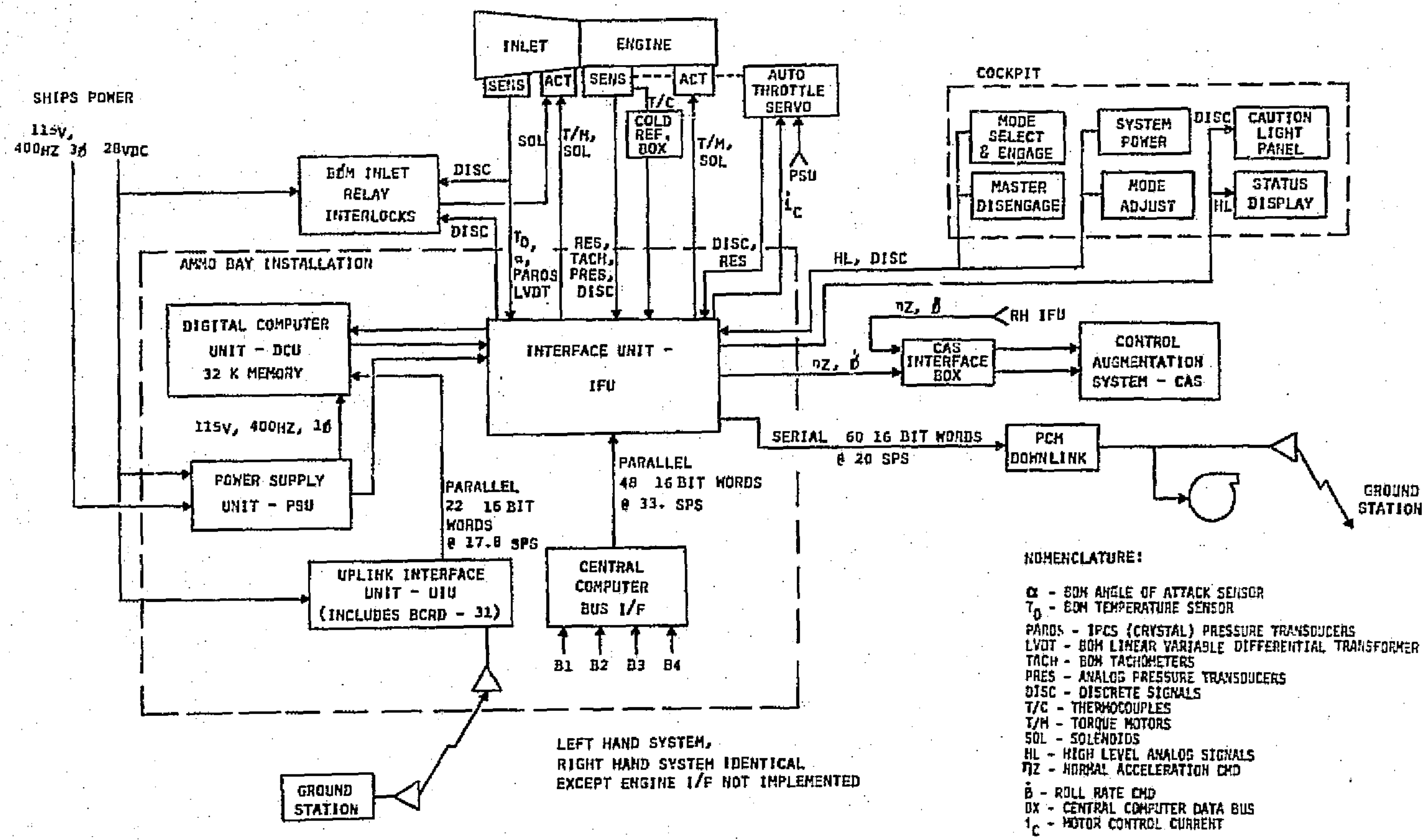

Figure 2.1-1. PROFIT System A Interconnection

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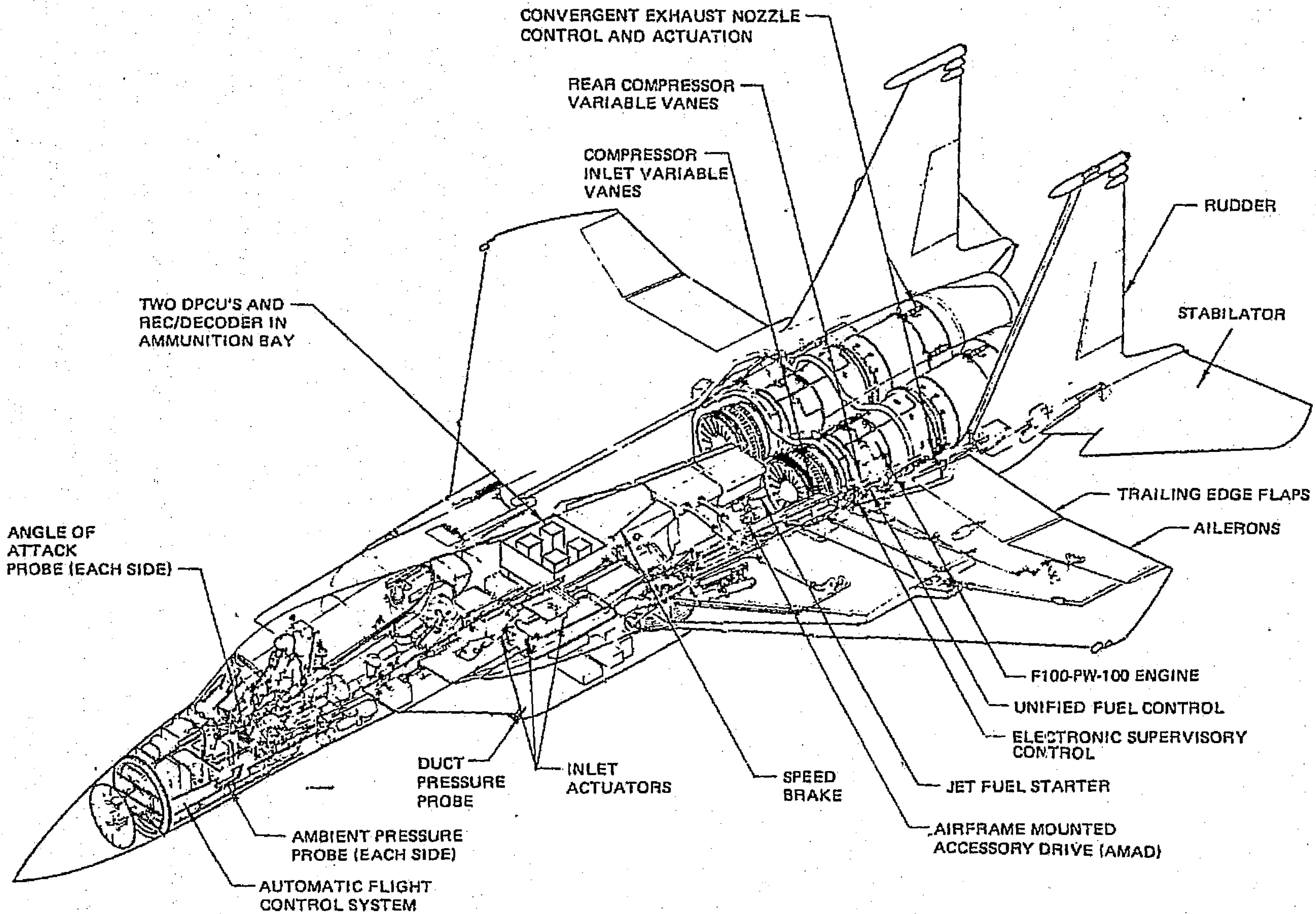

Figure 2.1-2. Aircraft Arrangement

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In addition to BØM temperature probes an array of total pressure probes, see Section 2.5, are installed on the engine. All temperature probes use Cromel/Alumel thermocouples as sensors. A solid state cold reference for each set of Cr/Al junctions is provided in the Cold Reference Box (CRB) used on IPCS. The CRB is installed external to the engine bay to avoid the engine ambient environment but close to the engine bay to minimize Cr/Al wire runs. Engine pressure and speed sensors are engine mounted. Based on IPCS performance strain gage pressure transducers are used mounted in a passively cooled protective container. Servo actuators and related position transducers are all engine mounted and incorporated in control modules distributed about the engine, see Figure 2.1-2. The auto throttle servo is mounted on the PLA shaft external to the fuel control.

Cockpit interface functions are distributed about the cockpit in a manner consistent with their relative importance to the pilot. The master disengage switch is stick mounted to provide rapid response capability in critical situations. PROFIT related caution lights are incorporated in the existing caution light panel to reduce pilot work load. Mode select and engage, mode adjust, power on/off, and status display are distributed about the cockpit consistent with available space and viewing/access requirements.

2.2 INLET

The engine inlet configuration is shown in Figure 2.2-1. The design is a two-dimensional, external-compression, three-ramp inlet with a variable capture area ramp and an air bypass system. The first ramp is used to adjust the capture area in order to lower the bypass requirements at high angle of attack. The second, third and diffuser ramps are mechanically linked together and move proportionally to the third ramp position to provide inlet/engine airflow matching and near maximum pressure recovery. The bypass system is used to trim the inlet airflow to accommodate the inlet, engine and control system tolerances, and the reduced engine airflows above 50,000 feet altitude.

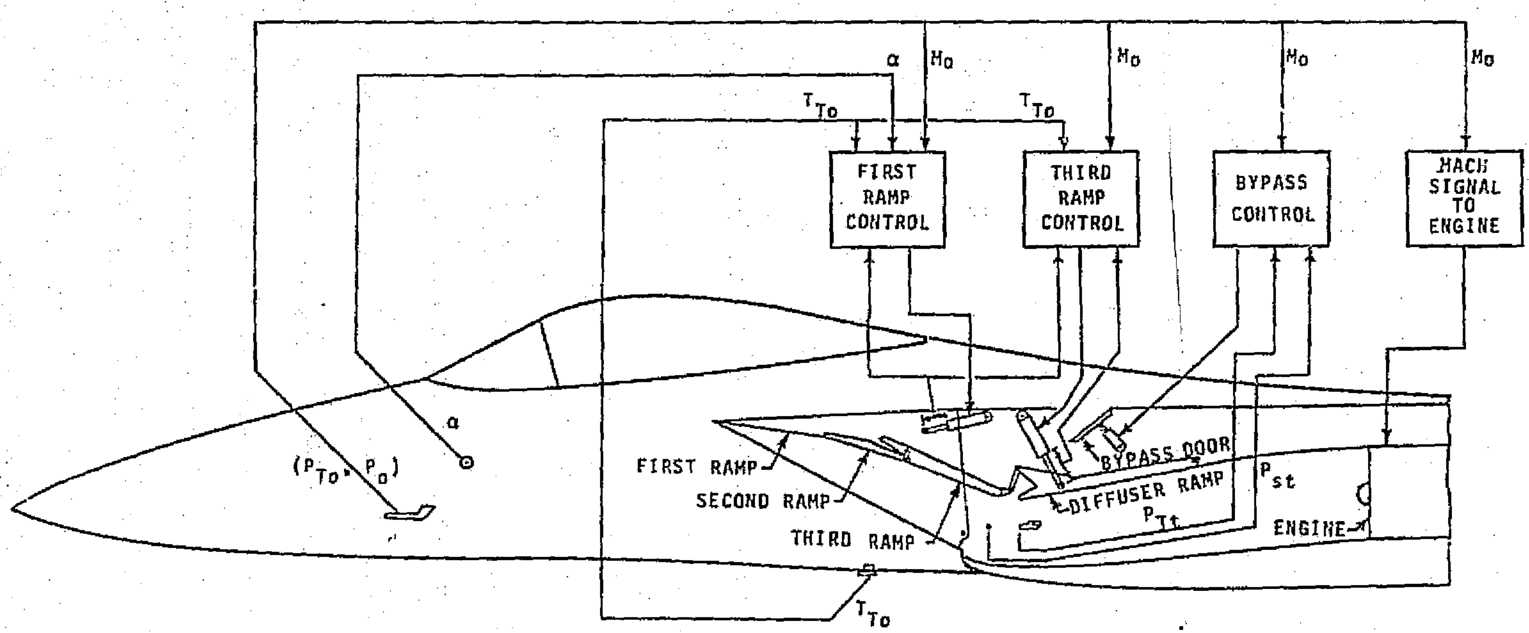


Figure 2.2-1. Inlet Configuration

The inlet surfaces are controlled by three electro-hydraulic actuators. The first and third ramp actuators operate as position servos using LVDT feedback. The bypass door operates as a rate servo to maintain scheduled duct pressure ratio. Commands to the actuators are computed by the inlet control portion of the DCU software and output through the IFU servo section to the BØM inlet actuators.

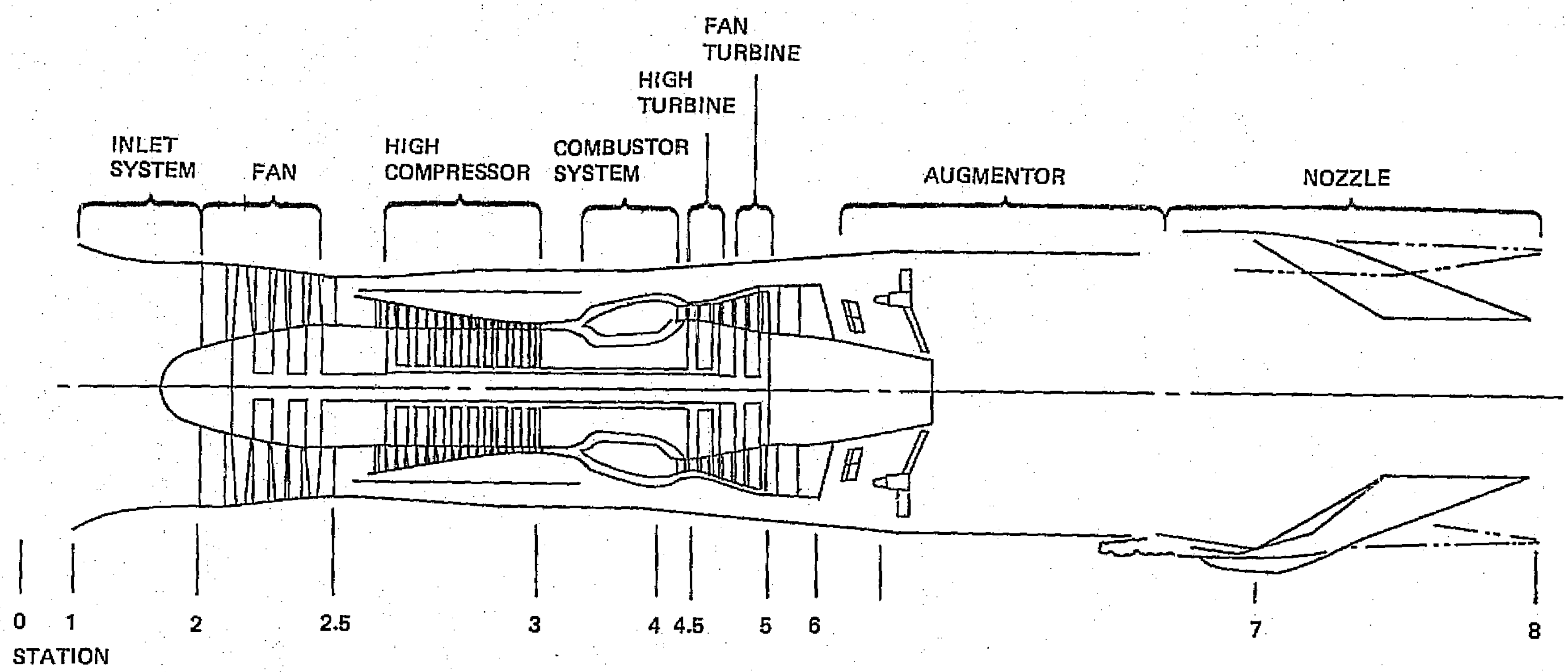
During facility development flight testing, see Section 5., the DCU control software will simulate the left hand BØM control using inputs of total temperature, angle of attack, duct pitot-static and free stream pitot-static signals obtained from aircraft mounted probes. BØM failure monitor and response functions will be provided by the DPCU.

During integrated controls research flight testing the right hand side DPCU will control the RH inlet and the inlet control modes will be revised in both the RH and LH sides to an advanced control algorithm, as yet undefined.

2.3 ENGINE

The Pratt & Whitney F100-PW-100 engine, Figure 2.3-1, is an axial, mixed-flow, augmented, twin-spool, low-bypass-ratio turbofan. A single inlet is used for both the fan airflow and the engine core airflow. Airflow leaving the fan is separated into two flow streams: one stream passing through the engine core and the other stream passing through the annular fan duct. A three-stage fan is connected by a through-shaft to the two-stage, low-pressure turbine. A 10-stage compressor is connected by a hollow shaft to the two-stage, high-pressure turbine. The fan has variable, trailing-edge, inlet guide vanes. These vanes, termed inlet guide vanes (IGV's) or compressor inlet variable vanes (CIVV's), are positioned by the controller to maintain fan stability at low speeds.

The compressor has a variable inlet guide vane followed by two variable stator vanes. These vanes, rear compressor variable vanes (RCVV's), are



See next page for station descriptions

Figure 2.3-1. F100 Component and Station Identification

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Station Description

0	-	Ambient
1	-	Aircraft Inlet
2	-	Engine Inlet
2.5C	-	Fan Discharge Downstream Exit Guide Vanes - Cold Stream
2.5H	-	Fan Discharge Downstream Exit Guide Vanes - Hot Stream
3	-	High Compressor Discharge
4	-	Combustor Exit
4.5	-	Fan Turbine Inlet
5	-	Fan Turbine Exit
6C	-	Augmentor Inlet - Cold Stream
6H	-	Augmentor Inlet - Hot Stream
6M	-	Augmentor Inlet - Precombustion Mixed
7M	-	Exhaust Nozzle Throat
8	-	Exhaust Nozzle Exit

Figure 2.3-1. (cont.)

mechanically linked and the set of vanes is positioned by the controller to maintain compressor stability. Engine airflow bleed is extracted at the compressor exit and discharged through the fan duct during starting. Compressor discharge bleed air is also used to cool the high- and low-pressure-turbine blades, to power the augmentor turbopump, and to supply the airplane environmental control system (ECS).

The main combustor consists of an annular diffuser and a chamber with 16 fuel nozzles. Fuel flow to the nozzles is metered by the engine fuel control, see Section 2.5.

The engine core and fan duct streams combine in an augmentor and are discharged through a variable convergent-divergent nozzle. The augmentor consists of a diffuser section and five concentric fuel manifolds (zones). The augmentor fuel control sequentially turns on the five zones and meters flow in terms of core and duct sectors of the augmentor. Engine airflow is controlled by the convergent divergent nozzle.

2.4 AUTOMATIC FLIGHT CONTROL SYSTEM

The F-15 AFCS consists basically of redundant electronic Control Augmentation System (CAS) operating in series with a mechanical boost and gain change system (Figure 2.4-1). Because of the series feature of the system the airplane can be flown through either system with the other inactive. The PROFIT system takes advantage of this feature to gain control of the longitudinal and lateral axes. CAS functions are retained to provide closed loop response to normal acceleration commands and roll rate commands input by PROFIT through the rear seat stick inputs of the CAS boxes. Directional control is provided by the yaw CAS which maintains zero lateral acceleration. Because of the series system design the PROFIT authority will be limited to 50% of the nominal aircraft capability and aircraft dynamic response will be slowed by lack of a mechanical stick command, since CAS is basically a makeup system.

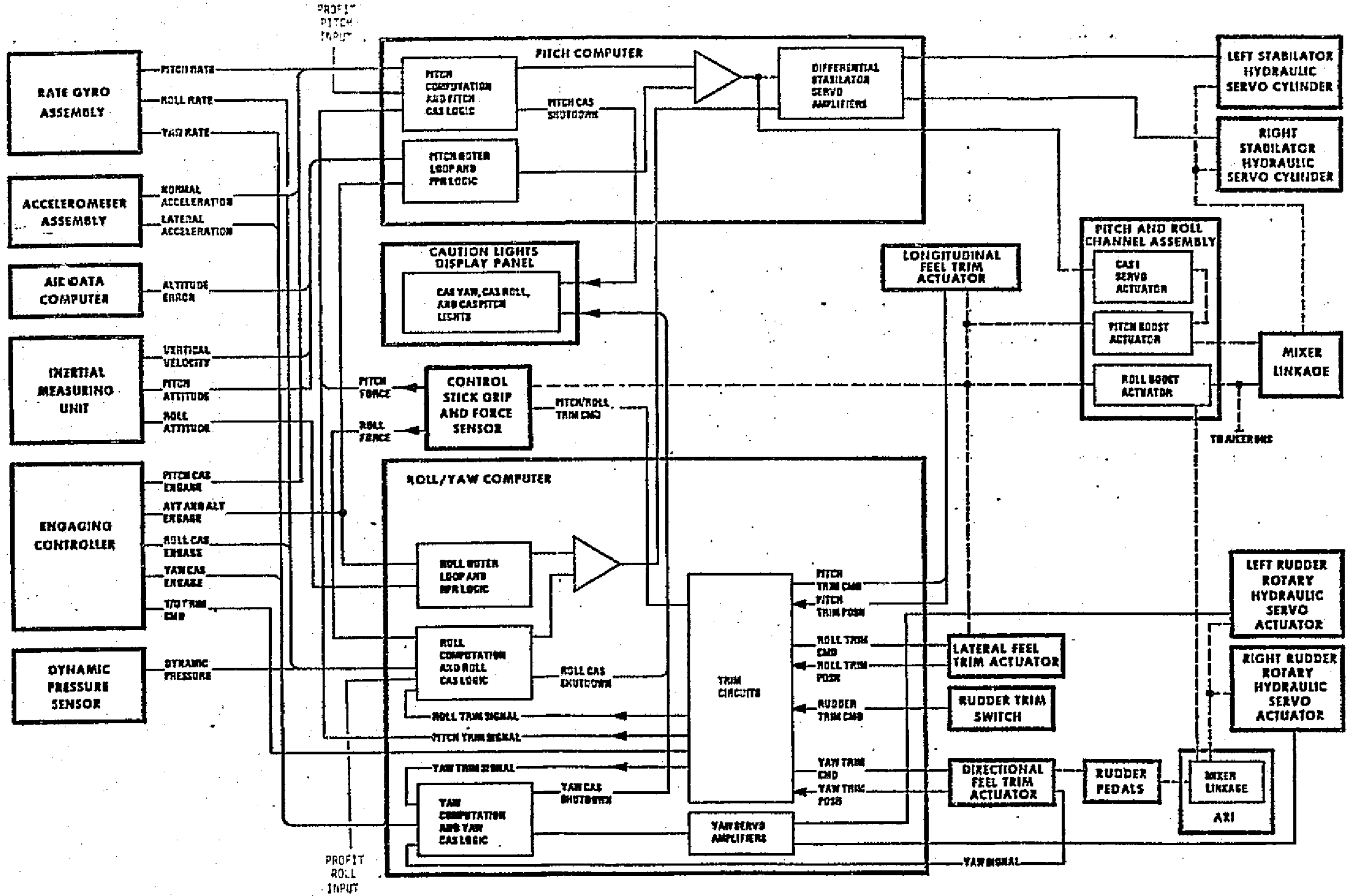

Figure 2.4-1. AFCS Block Diagram

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2.5 PROFIT CONTROL HARDWARE

Figure 2.5-1 is an interconnect diagram of the PROFIT system A hardware. This drawing serves as a design tool in configuration development and as a vehicle for describing the system. After a general discussion of the system the system elements are described in some detail grouped in five categories: servo systems, sensors, digital data systems, computation, and command and control system.

From a hardware standpoint, the Interface Unit (IFU) is the heart of the PROFIT system. With the exception of the input discretes the IFU converts all data flowing to and from the digital computer unit (DCU) to or from a parallel digital format from or to an analog or frequency format.

The servo section of the IFU converts DCU digital output words to analog servo commands. The eleven inlet/engine servos are controlled on a closed loop basis by analog electronics on the dual servo loop closure cards. An exception is the bypass door which is modulated as a rate servo to maintain a desired throat pressure ratio. This loop is closed in the DCU. The CAS modulator is also driven by analog commands. Its output to the CAS is however open loop, depending upon the loop closures in the CAS and outer loop closure through the DCU to obtain the desired response. The remaining D/A outputs are used to drive cockpit displays on an open loop basis.

The IFU serves as a DMA controller to multiplex inputs into the DCU. Two A/D converter/mux systems provide 32 channels of high level ($\pm$5.12 volts) and 32 channels of low level ($\pm$30 mV) analog data to the DMA bus. LVDT data are demodulated and then processed through the high level mux. Ten resolver to digital converters provide engine actuation surface position to the DMA bus and frequency to digital converters provide engine speeds and inlet pressures.

Two sources of digital data are also input to the DCU through the IFU. Data from the central computer bus is multiplexed onto the DMA bus and data from the uplink is input through the DCU input bus. The IFU also outputs parallel digital data from the DCU output bus to the T/M down-link.

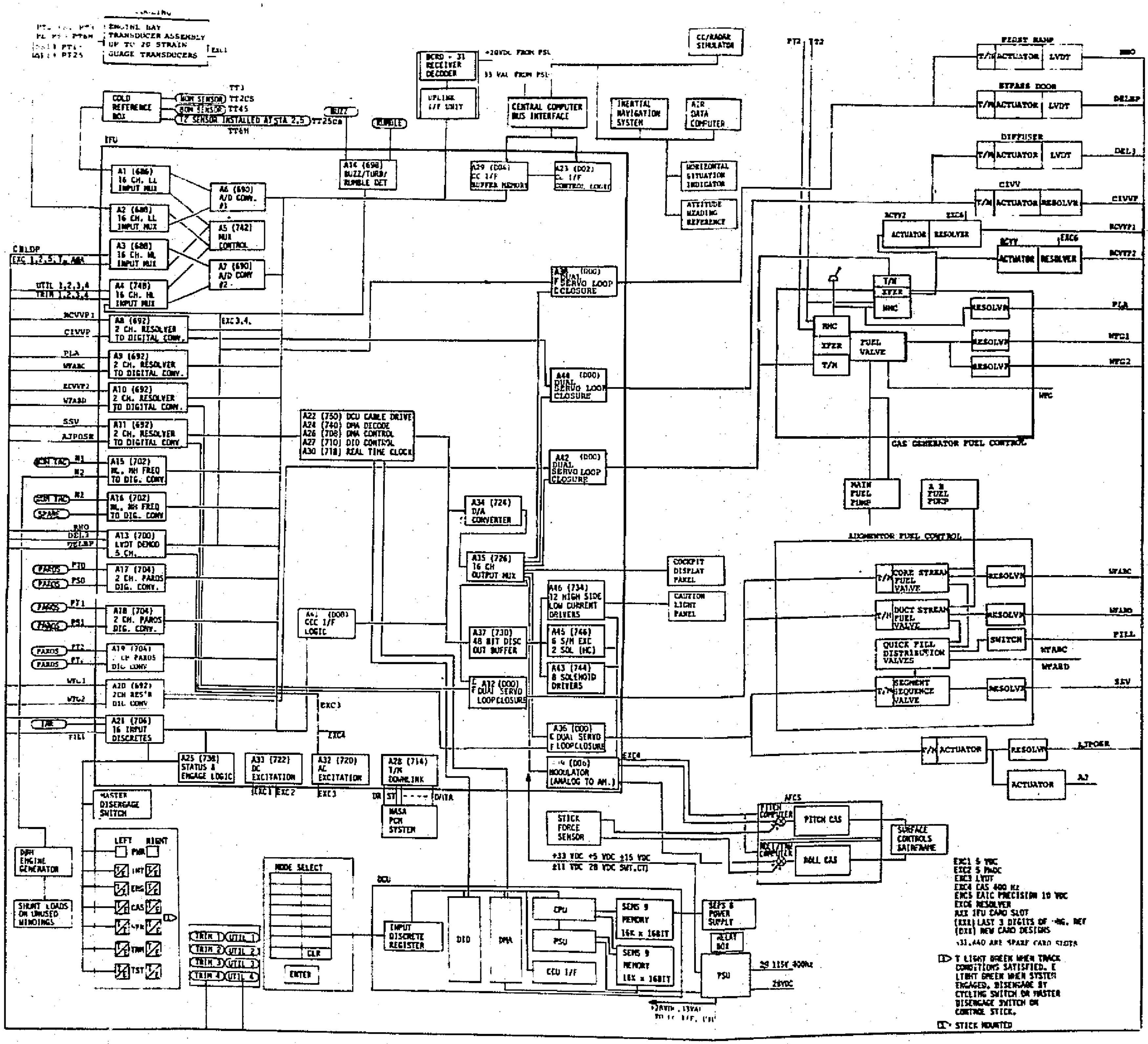

Figure 2.5-1. IFU Diagram

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The IFU also provides a multitude of housekeeping functions including DMA control, input and output discretes, sensor excitation, and status engage logic.

The power supply unit (PSU) provides power to the DCU, the IFU, the Uplink Interface Unit (UIU) and the Central Computer Bus Interface (CCBI).

The DCU provides all controller computations based on inputs from the TSU and outputs resulting commands to the IFU. Secondary mode selection information is input directly from the cockpit interface to the DCU input discrete register.

Transducers are distributed about the airplane and engine to provide extensive data for as yet to be defined purposes. Table 2.5-1 is the instrumentation list for the IFU at this point in time. Figure 2.3-1 defines engine station locations.

2.5.1 Servo Actuation Systems

As shown in Figure 2.5-1 the IFU D/A converter and mux provide analog commands to 16 closed loop servos. Three of these servos are as yet undesignated analog cockpit displays. As shown in Table 2.5-2, 10 of the servos consist of torque motor controlled hydraulic actuators with electronic feedback. Figure 2.5-2 and Tables 2.5-3 and 2.5-4 define the inlet servos and Figure 2.5-3 and Tables 2.5-5 and 2.5-6 define the characteristics of the engine related servos.

Figure 2.5-4 depicts the CAS command interface. Two D/A channels provide inputs to a modulator which in turn drives the aft seat stick inputs of the pitch and roll CAS computers.

The auto throttle system, Figure 2.5-5, is assembled using the electromechanical servo components from the F-14 Approach Power Control Unit and servo loop closure elements in the IFU. An analysis of this system is documented in Section 4.14.

TABLE 2.5-1 PROFIT PRELIMINARY CONTROL INSTRUMENTATION LIST

ENGINE VARIABLES

VARIABLE	NOMENCLATURE	REMARKS
N1	LOW ROTOR SPEED	BOM TRANSDUCER, REDUNDANT
N2	HIGH ROTOR SPEED	BOM TRANSDUCER, REDUNDANT
PT2	SEE FIGURE 2.3-1 FOR STATION DESIGNATIONS	BOM PROBE
PS2		DEEC PROBE
PT25		DEEC PROBE
PT3		P&W 1165 KIT
PS6		BOM PROBE
PT6M		BOM TRIM PROBE
ΔP/PT13		MVC PROBE
PT13, PS13		MVC PROBE
TT2CS		BOM PROBE
TT2.5CS		BOM TT2 PROBE & ADAPTER
TT3		P&W 1165 KIT
TT4.5(FTIT)		BOM PROBE
TT6HAVG		P&W 1164 KIT

ENGINE ACTUATORS

VARIABLE	NOMENCLATURE	REMARKS
WFG	GAS GENERATOR FUEL FLOW	DEEC FUEL CONTROL, REDUNDANT
WFABC	AUGMENTOR FUEL FLOW (CORE)	DEEC FUEL CONTROL, REDUNDANT
WFABD	AUGMENTOR FUEL FLOW (DUCT)	DEEC FUEL CONTROL, REDUNDANT
SSV	SEGMENT/SEQUENCE VALVE POSITION	DEEC FUEL CONTROL, REDUNDANT
AJPOSR	AJ POSITION REQUEST	DEEC FUEL CONTROL, REDUNDANT
RCVVP	RCVV POSITION	DEEC FUEL CONTROL, REDUNDANT
PLA	POWER LEVER ANGLE AT FUEL CONTROL INPUT SHAFT	DEEC FUEL CONTROL, REDUNDANT
CBLDP	CUSTOMER BLEED POSITION	MVC
AJPOSA	AJ POSITION ACTUAL	P&W KIT

TABLE 2.5-1 PROFIT PRELIMINARY CONTROL INSTRUMENTATION LIST (CONT)

ENGINE FUEL CONTROL VARIABLES

VARIABLE	NOMENCLATURE	REMARKS
PF2	MAIN FUEL PUMP DISCHARGE PRESSURE	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF1A	AUGMENTOR FUEL PUMP DISCHARGE PRESSURE	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4	MAIN CONTROL DISCHARGE PRESSURE	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF1	MAIN PUMP INTERSTAGE PRESSURE	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4A1	AUGMENTOR CONTROL DISCHARGE PRESSURE (1)	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4A2	AUGMENTOR CONTROL DISCHARGE PRESSURE (2)	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4A3	AUGMENTOR CONTROL DISCHARGE PRESSURE (3)	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4A4	AUGMENTOR CONTROL DISCHARGE PRESSURE (4)	P&W KIT, STRAIN GAUGE TRANSDUCERS
PF4A5	AUGMENTOR CONTROL DISCHARGE PRESSURE (5)	P&W KIT, STRAIN GAUGE TRANSDUCERS

INLET VARIABLES

VARIABLE	NOMENCLATURE	REMARKS
PTO	AMBIENT TOTAL PRESSURE	BOM PROBE, PAROS TRANSDUCER
PSO	AMBIENT STATIC PRESSURE	BOM PROBE, PAROS TRANSDUCER
PT1	BOM THROAT PRESSURE TAP	BOM PROBE, PAROS TRANSDUCER
PS1	BOM THROAT PRESSURE TAP	BOM PROBE, PAROS TRANSDUCER
ALPHA	AIRCRAFT ANGLE OF ATTACK	BOM PROBE, TRANSDUCER
TTO	AMBIENT TOTAL TEMPERATURE	BOM PROBE, TRANSDUCER

INLET INPUT DISCRETES

VARIABLE	NOMENCLATURE	REMARKS
IGTA	GROUND TEST MODE A	
IGTB	GROUND TEST MODE B	
AMOF	B POSITION MODE SWITCH	

TABLE 2.5-1 PROFIT PRELIMINARY CONTROL INSTRUMENTATION LIST (CONT)

INLET ACTUATOR POSITIONS

VARIABLE	NOMENCLATURE	REMARKS
RHO	FIRST RAMP ANGLE	BOM LVDT
DEL3	THIRD RAMP ANGLE	BOM LVDT
DEL13P	BYPASS DOOR ANGLE	ADD LVDT

INLET OUTPUT DISCRETES

MBLK	MACH BLOCK	
ILFL	INLET FAILURE BUZZ/SJ	

ENGINE DISCRETES

MODE	INDICATES DIGITAL OR HYDROMECHANICAL CONTROL	DEEC FUEL CTRL SWITCH
PR/TMP DG	INDICATES DEEC PRES. OR TEMP SENSOR FAILURE	DEEC FUEL CTRL SWITCH
FILL	INDICATES AUG. MANIFOLD FILL COMPLETE	DEEC FUEL CTRL SWITCH

AIRFRAME VARIABLES

ADC - BUS 1/3

RT	MSGLBL (SELWD)	WD POS	WORD LABEL	OFP LOC	LSB POS	PARAM LABEL	NUM BIT	PARAMETER NAME
20	IADC01 (103A)	1	ITASPD	0076	14	IASPDT	15	TRUE AIRSPEED
					15	ITASPV	1	TRUE AIRSPEED VALIDITY
		2	ITRADA	0077	14	IAATKT	15	TRUE ANGLE OF ATTACK
					15	IAATKV	1	TRUE ANGLE OF ATTACK VALIDITY
		3	IHBALT	0078	15	IHBALT	16	PRESSURE ALTITUDE + VALIDITY
		4	IIASPD	0079	14	IASPDI	15	INDICATED AIRSPEED
					15	IIASPV	1	INDICATED AIRSPEED VALIDITY
		5	ILOAOA	0074	14	ILAOAD	15	LOCAL ANGLE OF ATTACK
					15	ILAOAV	1	LOCAL ADA VALIDITY
		6	IMCHNO	007B	14	IMACHN	15	MACH NUMBER
					15	IMCHNV	1	MACH NUMBER VALIDITY

TABLE 2.5-1 PROFIT PRELIMINARY CONTROL INSTRUMENTATION LIST (CONT)

AIRFRAME VARIABLES (Cont)

ADC - BUS 1/3 (Cont)

RT MSGLBL (SELWD)	WD POS	WORD LABEL	OFP LOC	LSB POS	PARAM LABEL	NUM BIT	PARAMETER NAME
	7	IPRTIO	007C	14	IPRRAT	15	PRESSURE RATIO
				15	IPRRTV	1	PRESSURE RATIO VALIDITY
	8	IRAIRD	007D	14	IAIRDN	15	RELATIVE AIR DENSITY
				15	IAIRDV	1	RELATIVE AIR DENSITY VALIDITY
	9	ISTADA	007E	14	ISIAOD	15	OPTIMUM ANGLE OF ATTACK
				15	ISTAOV	1	OPTIMUM AOA VALIDITY
	10	IBCALT	007F	15	IBCALT	16	BAROMETRIC CORRECTED PRESS. ALT

IMU - BUS 2/4

RT MSGLBL (SELWD)	WD POS	WORD LABEL	OFP LOC	LSB POS	PARAM LABEL	NUM BIT	PARAMETER NAME
20 IIMU01	1	IDVALT	0086	0	IINSVL	1	INS VALIDITY
(503C)				1	IATIVI	1	INS ATTITUDE VALIDITY
	2	IBIALT	0087	15	IBIALT	16	INERTIAL ALTITUDE
	3	IPPLAT	0088	15	IPPLAT	16	PRESENT POSITION LATTITUDE
	4	IPPLAT	0089	1	IPPLAT	2	PRESENT POSITION LATITUDE
	5	IPPLON	008A	15	IPPLON	16	PRESENT POSITION LONGITUDE
	6	IPPLON	008B	1	IPPLON	2	PRESENT POSITION LONGITUDE
	7	IPICHI	008C	13	IPTCHI	14	PITCH
	8	IROLLI	008D	13	IROLLI	14	ROLL
	9	ITUHDI	008E	13	ITUHDI	14	TRUE HEADING
	10	IVELNS	008F	14	IVELNS	15	NORTH - SOUTH VELOCITY
	11	IVELEW	0090	14	IVELEW	15	EAST - WEST VELOCITY
	12	IVELVT	0091	14	IVELVT	15	VERTICAL VELOCITY
20 IIMU02	1	IACCNS	0082	10	IACCNS	11	NORTH - SOUTH ACCELERATION
(5053)	2	IACCEW	0083	10	IACCEW	11	EAST - WEST ACCELERATION
	3	IACCVE	0084	11	IACCVE	12	VERTICAL ACCELERATION

TABLE 2.5-1 PROFIT PRELIMINARY CONTROL INSTRUMENTATION LIST (CONT)

AIRFRAME VARIABLES (Cont)

HSI BUS 2/4

RT	MSGLBL (SELWD)	WD POS	WORD LABEL	OFP LOC	LSB POS	PARAM LABEL	NUM BIT	PARAMETER NAME
20	IHSI02	1	IHSICS	0096	10	IHSICS	11	COURSE SET
	(4057)	2	IHSIHS	0097	10	IHSIHS	11	HEADING SET
		3	IRGICN	0098	13	IRGTCN	14	TACAN DISTANCE
		4	IRRICN	0099	12	IBRICN	13	TACAN BEARING
		5	IHSIX1	009A	0	ITVABX	1	BEARING RELIABILITY ALARM
					1	ITVARX	1	DISTANCE RELIABILITY ALARM
					2	ILSLVR	1	LOCALIZER RELIABILITY ALARM
					3	ILSGSR	1	GLIDESLOPE RELIABILITY ALARM
					4	ILSMOM	1	MIDDLE/OUTER MARKER
		6	ILSLVD	0098	7	ILSLVD	8	LOCALIZER DEVIATION
		7	ILSGSD	009C	7	ILSGSD	8	GLIDESLOPE DEVIATION

AHR BUS 1/3

RT	MSGLBL (SELWD)	WD POS	WORD LABEL	OFP LOC	LSB POS	PARAM LABEL	NUM BIT	PARAMETER NAME
20	IAHR02	1	IPTCHA	00AC	11	IPTCHA	12	PITCH ANGLE
	(2053)	2	IROLLA	00AD	11	IROLLA	12	ROLL ANGLE
		3	IMAGHD	00AE	11	IMAGHD	12	MAGNETIC HEADING

GROUND COMMANDS/UPDATES

The DPCU will accept 22 words from the UPLINK at ~ 18 samples/sec.

TABLE 2.5-2
PROFIT SERVO LOOPS

CONTROLLED VARIABLE	INPUT DEVICE	POSITION MEASUREMENT	LOCATION
First Ramp	T/M	LVDT	INLET
Bypass Door	T/M	LVDT	INLET
Diffuser	T/M	LVDT	INLET
CIVV	T/M	RESOLVER	CIVV MASTER CYLINDER
RCVV	T/M	RESOLVER (DUAL)	RCVV MASTER CYLINDER RCVV SLAVE CYLINDER
WFG	T/M	RESOLVER (DUAL)	GAS GENERATOR FUEL CONTROL
WFABC	T/M	RESOLVER	AUGMENTOR FUEL CONTROL
WFABD	T/M	RESOLVER	AUGMENTOR FUEL CONTROL
SSV	T/M	RESOLVER	AUGMENTOR FUEL CONTROL
AJ	T/M	RESOLVER	CONVERGENT EXHAUST NOZZLE CONTROL
ETAZ	DEMOD	-	PITCH COMPUTER
PHIDØT	DEMOD	-	ROLL COMPUTER
PLA	LHS NONE (SOFTWARE) RHS A/C SERVO MOTOR	RESOLVER	AUTOTHROTTLE ACTUATOR (RHS) (GAS GENERATOR CONTROL LHS)
Cockpit Displays (3)	HI - IMPEDANCE VOLT METER OR EQ.	-	COCKPUT PANEL

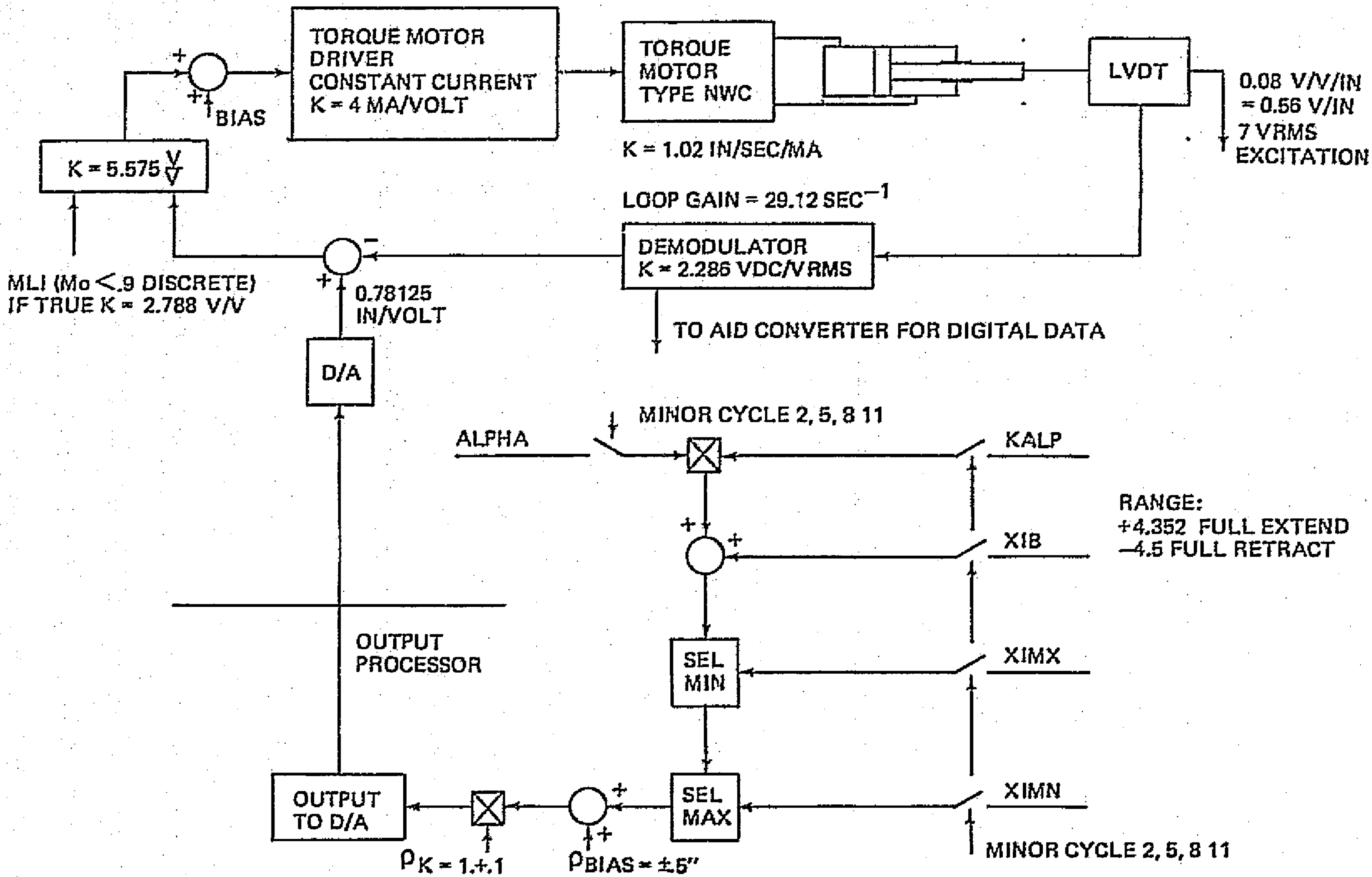


Figure 2.5-2a First Ramp Servo

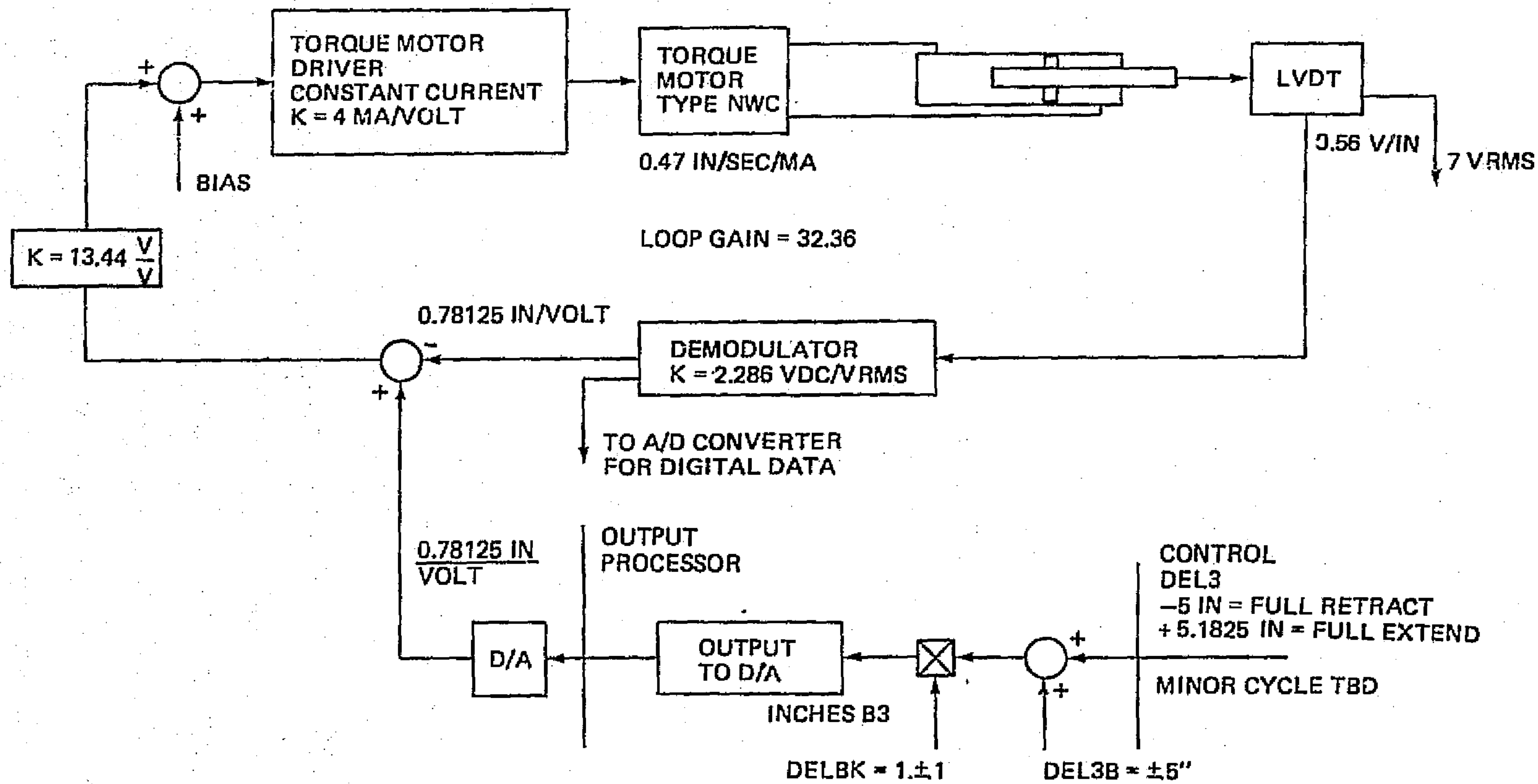


Figure 2.5-2b Third Ramp Servo

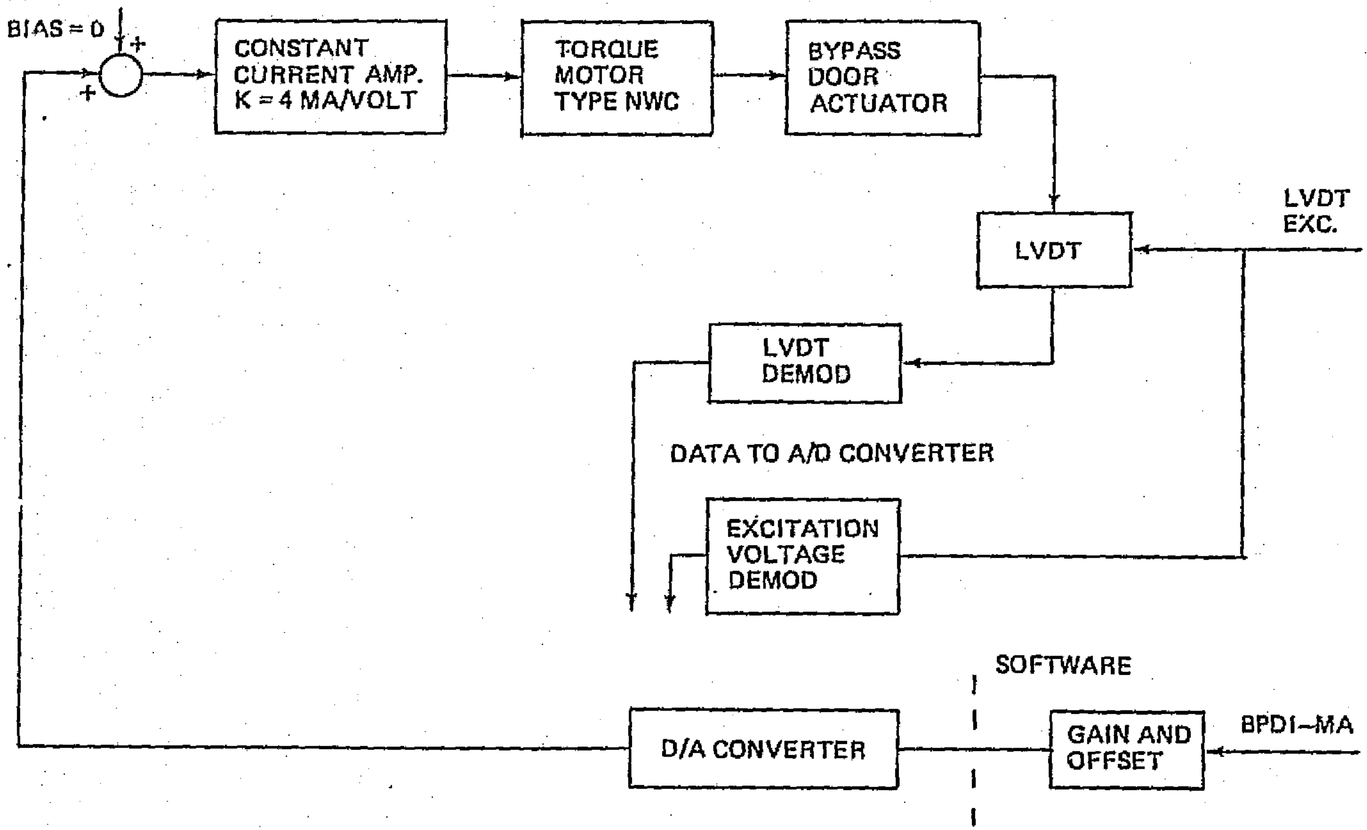


Figure 2.5-2c Bypass Door Servo Loop

TABLE 2.5-3
TYPE NWC SERVO VALVE CHARACTERISTICS

Coil - All Units

D.C. Resistance	=	125. ± 12.5 OHMS @ $70^{o}F$
Rated Current	=	± 20. ma
Max Current	=	±40. ± 3. ma
Coil Configuration	=	Parallel Aiding
Inductance	=	.58 henries @ 50 hz

VALVE CHARACTERISTICS

Unit	Gain (Nominal)	Null Bias	+ Rate Limit	- Rate Limit	Servo Open Loop Gain
First Ramp	+ 1.02 in/sec/ma	0.	+ 21. in/sec	-21. in/sec	29.12 sec^{-1}
Bypass Door	+ .681 in/sec/ma	0.	+ 18.3 in/sec	-18.3 in/sec	Variable
3rd Ramp	+ .47 in/sec/ma	0.	+ 10. in/sec	-10. in/sec	32.26 sec^{-1}

TABLE 2.5-4
LVDT CHARACTERISTICS

BYPASS DOOR LVDT CHARACTERISTICS

Excitation	9V rms $\pm$ 10% 1 Khz $\pm$ hz Power Drain: 2.0 VA max.
Output Signal	At full stroke: 5 volts rms min
Sensitivity	Not yet defined $\pm$ 3% or 30 mv. whichever is greater
Linearity	Within $\pm$ .5% of full stroke voltage of the best straight line.
Phase Shift	$\pm 10^{0}$ max.
Null Voltage	Not to exceed 30 mv rms.
Full Stroke	Not yet defined
Schematic	

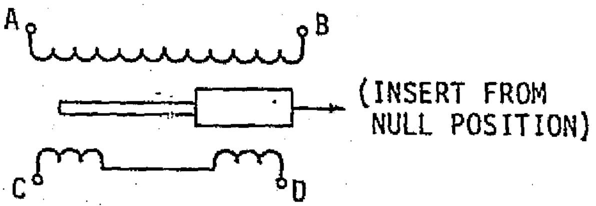


TABLE 2.5-4 (Cont.)

FIRST RAMP LVDT CHARACTERISTICS

Excitation voltage	7 volts A.C. (RMS) $\pm$ 25. mv
Excitation frequency	2.5 K Hz + 0.1%
LVDT Primary Input Impedance	300 ohm $\pm$ 25% (resistive) } at 2.5K Hz 64 ohm $\pm$ 53% (inductive)
Phase shift	5^o maximum
*Sensitivity (Scale factor)	0.08 volts/volt/inch
LVDT Output Impedance	500 ohm maximum at 70^oF (575 ohm maximum at 275^oF)
*Null Position	0. in phase volts to be 4.425 $\pm$ 0.010 inches from full retract position
Total stroke (nominal)	$\pm$ 4.425 inches from null
Null quadrature voltage	30. mv. (at 7. VRMS excitation) max.
EAIC load on LVDT secondary	10 K ohm $\pm$ 1% (resistive)
*Local slope variation	(% of sensitivity) $\pm$10.% max. (Defined as incremental change from .08 v/v/inch sensitivity measured over .100 inch increment throughout entire stroke in either direction)
*Combined Accuracy (Linearity and	$\pm$ 0.7% of stroke maximum error at $75.^oF \pm 5^oF$. (stroke = 4.425 inches)
*Temperature Error	% of stroke maximum error (stroke - 4.425 inches)
Maximum Allowable Error	Sum of Combined Accuracy and Temperature Error

*Defined with an LVDT secondary resistive load of 10K Ω $\pm$1.%

DIFFUSER RAMP LVDT CHARACTERISTICS

Excitation voltage	7 volts ac (RMS) $\pm$ 25. mv
Excitation frequency	2.5K Hz + 0.1%
LVDT Primary Input Impedance	300 ohm $\mp$ 25% (resistive) } at 2.5K Hz 64. ohm $\mp$ 53% (inductive)
Phase Shift	5^o maximum
Sensitivity (Scale factor)	0.08 volts/volt/inch
LVDT Output Impedance	500 ohm maximum at 70^oF (575 ohm maximum at $275.^oF$)
*Null Position	0. in phase volts to be 5.085 $\pm$ 0.010 inches from full retract position

TABLE 2.5-4 (Cont)

Total Stroke (nominal)	± 5.085 inches from null
Null quadrature voltage	30. mv. (at 7. VRMS excitation) max.
EAIC load LVDT secondary	10K ohm ± 1% (resistive)
*Local slope variation	(% of sensitivity) ± 10.% max. (Defined as incremental change from .08 v/v/inch sensitivity measured over .100 inch increment throughout entire stroke in either direction)
*Combined Accuracy (Linearity and Sensitivity)	± 0.7% of stroke maximum error at 75.0 ± 5.0F. (stroke = 5.085 inches)
*Temperature Error	% of stroke maximum error (stroke = 5.085 inches)
Maximum Allowable Error	Sum of Combined Accuracy and Temperature Error.

*Defined with an LVDT secondary resistive load of 10K Ω ± 1.%.

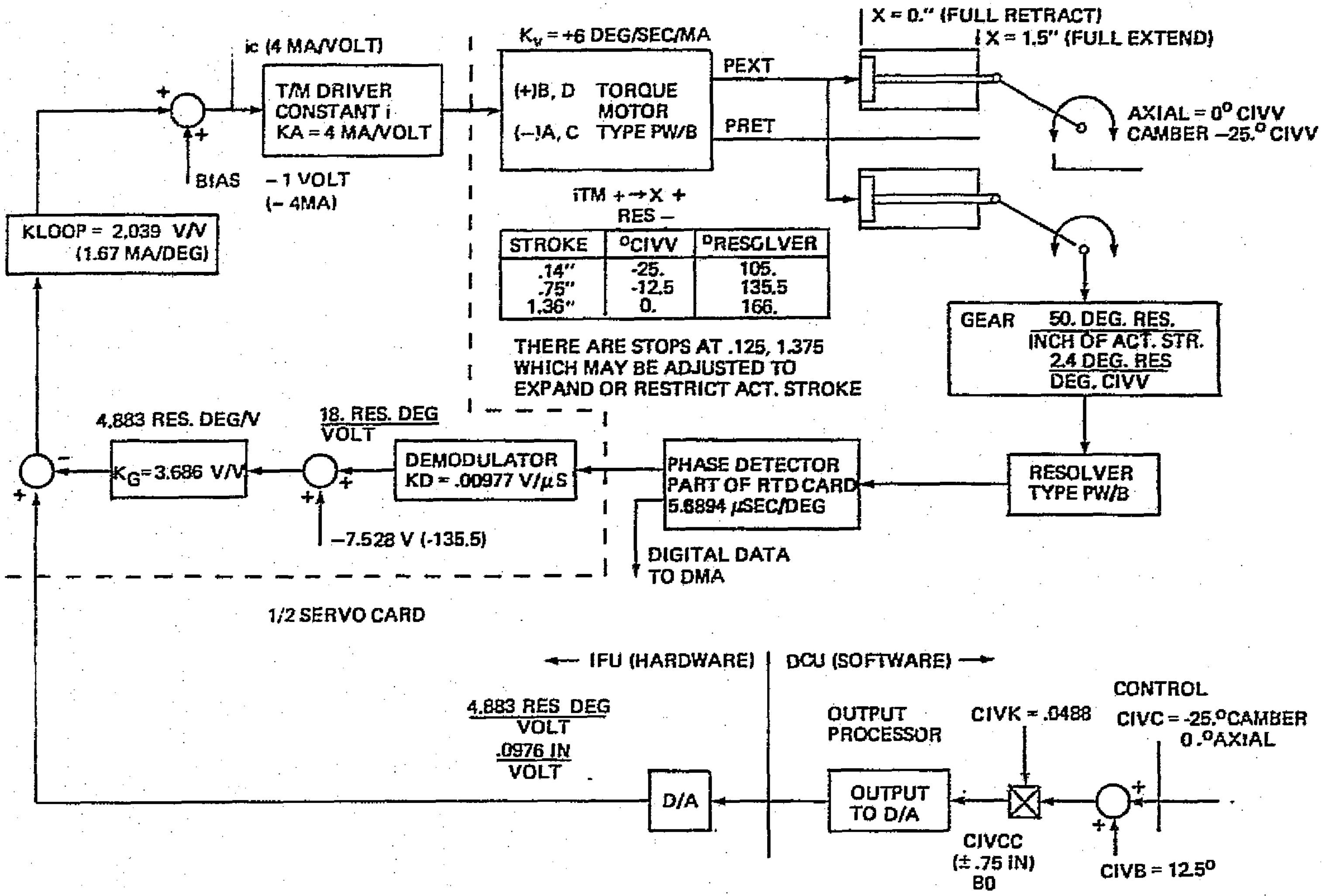


Figure 2.5-3a CIVV Servo Loop

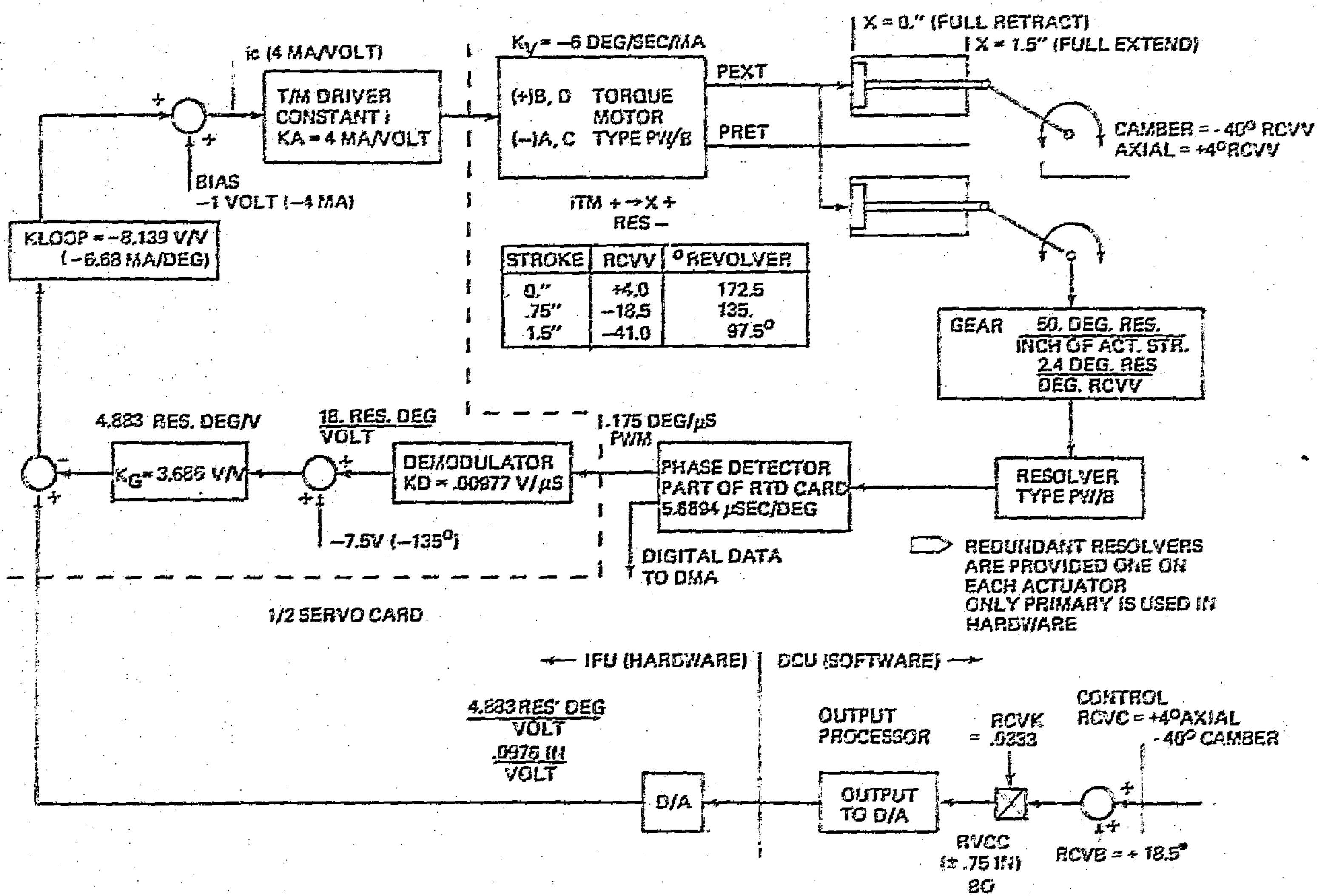


Figure 2.5-3b RCVV Servo Loop

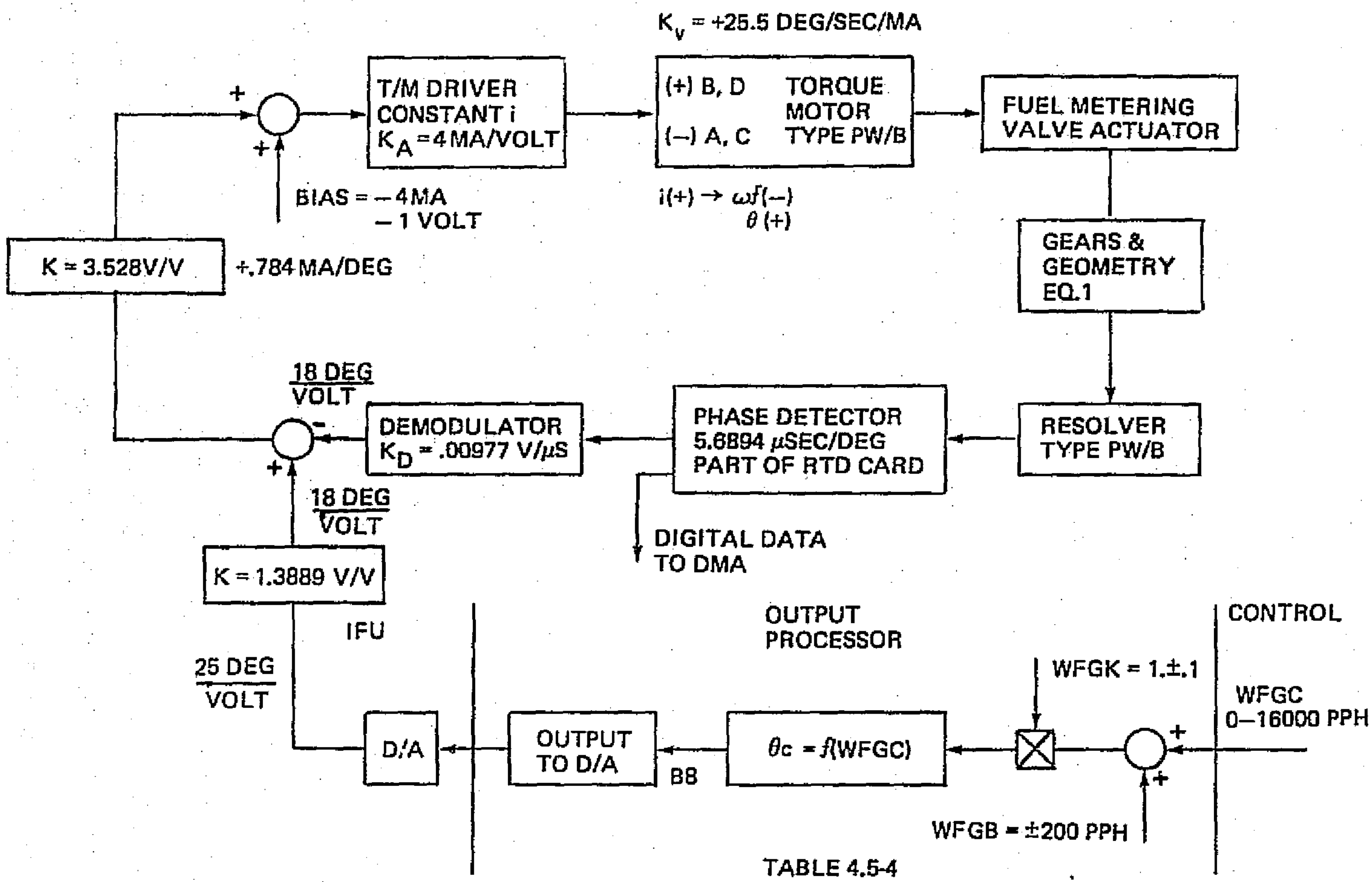


Figure 2.5-3c Main Fuel Servo

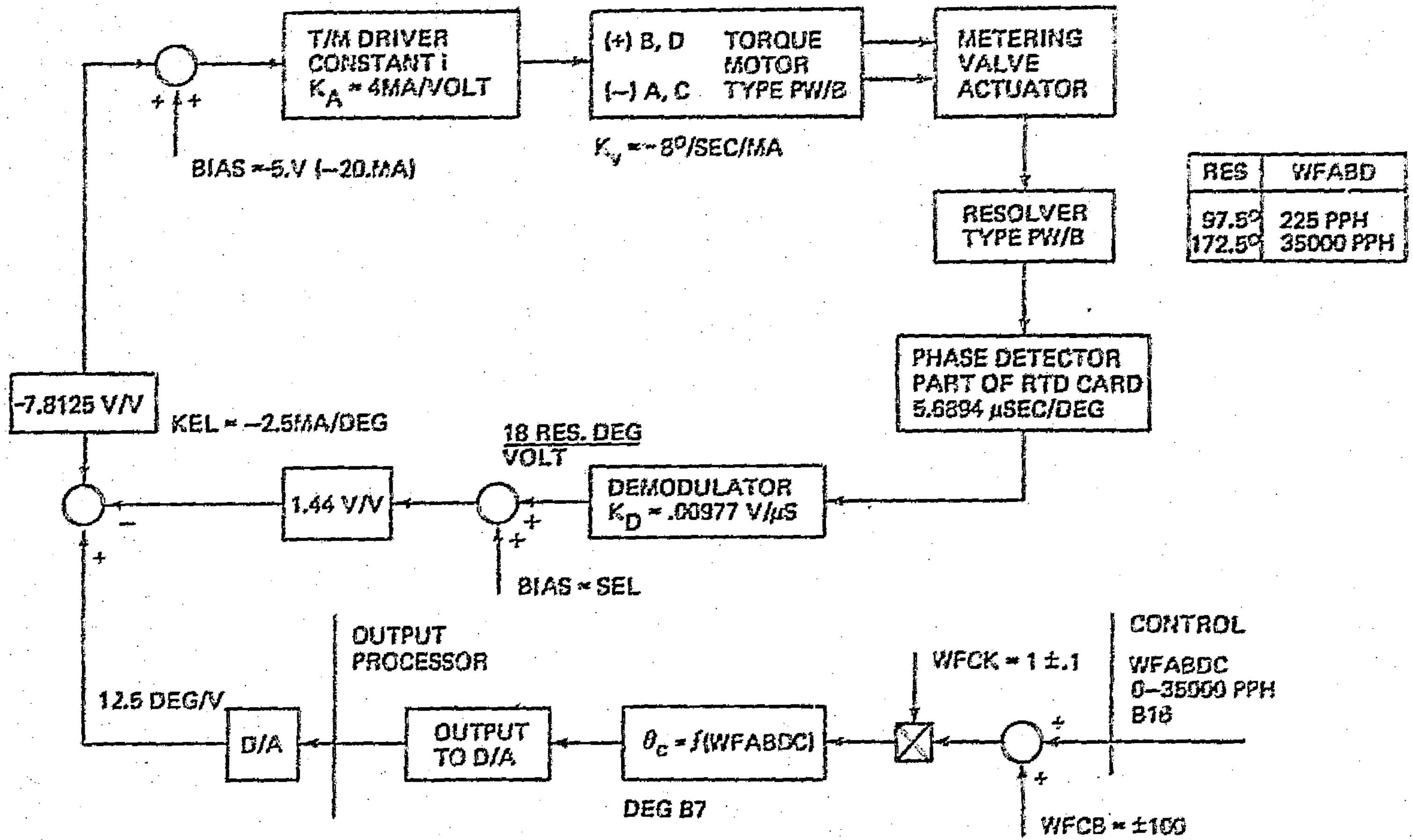


Figure 2.5-3d A/B Duct Fuel Flow Servo

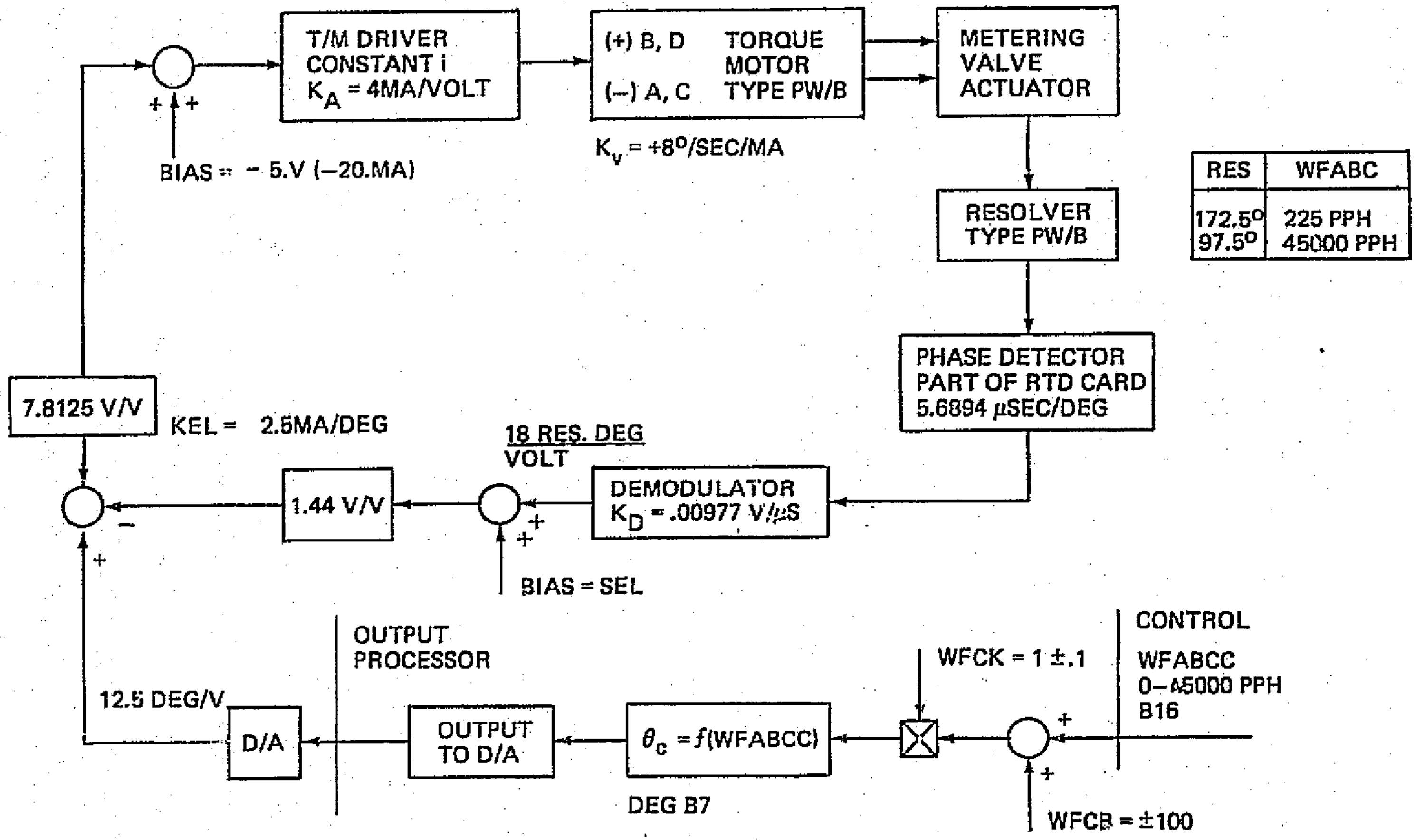
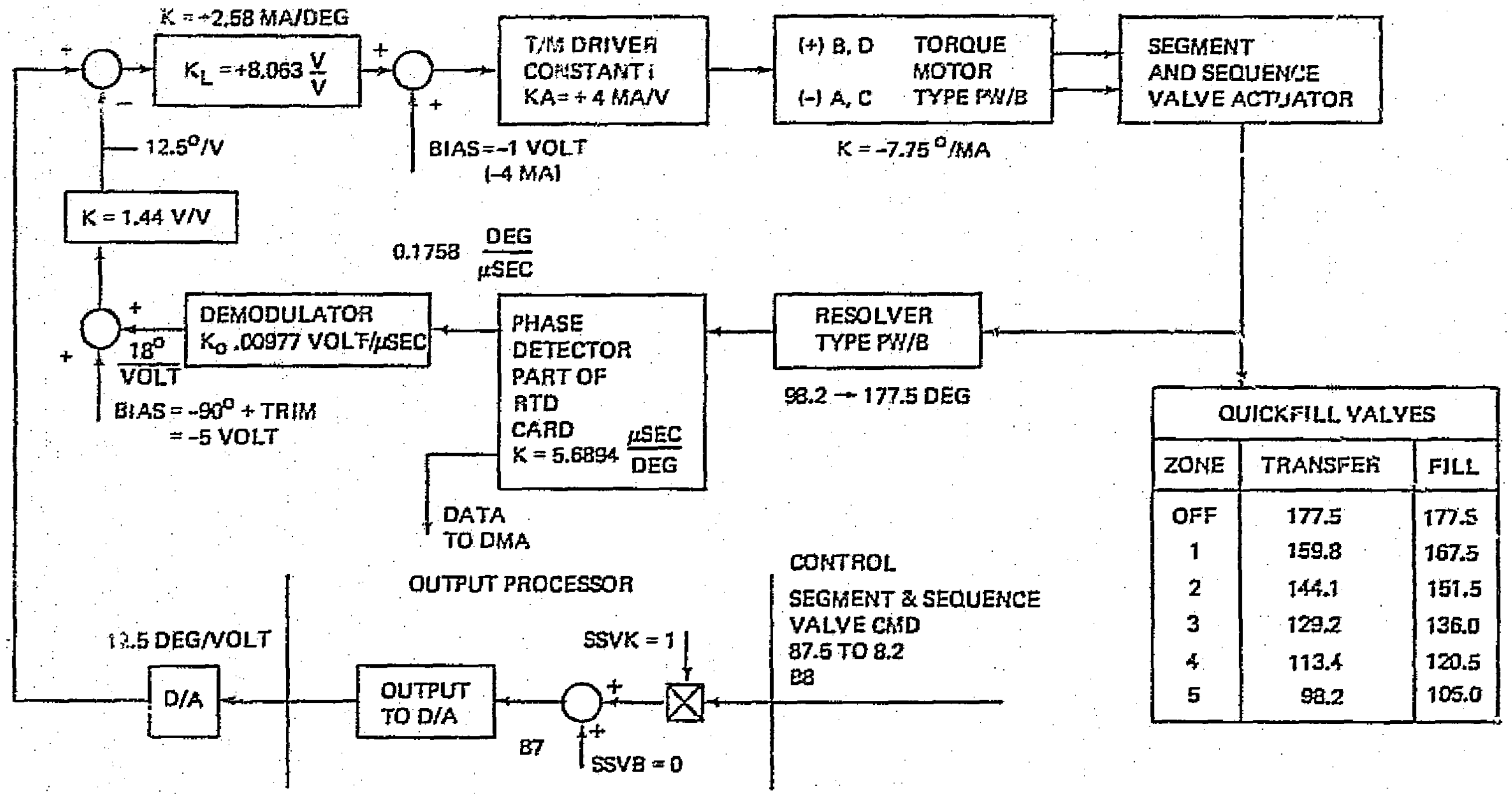


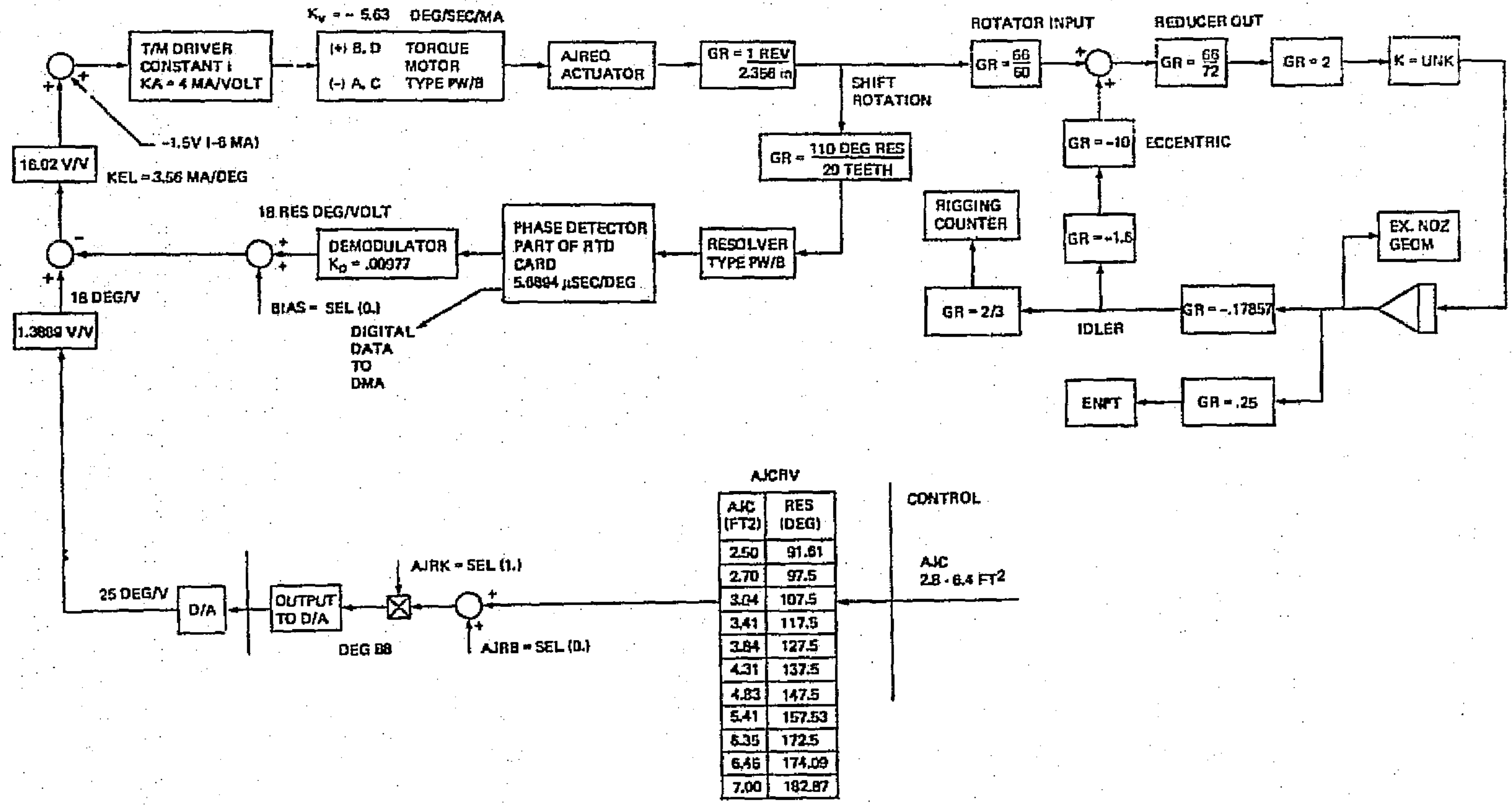
Figure 2.5-3e A/B Core Fuel Flow Servo



QUICKFILL VALVES

ZONE	TRANSFER	FILL
OFF	177.5	177.5
1	159.8	167.5
2	144.1	151.5
3	129.2	136.0
4	113.4	120.5
5	98.2	105.0

Figure 2.5-3f Segment and Sequence Value Servo Loop



AJC (FT2)	RES (DEG)
2.50	91.61
2.70	97.5
3.04	107.5
3.41	117.5
3.84	127.5
4.31	137.5
4.83	147.5
5.41	157.53
6.35	172.5
6.46	174.09
7.00	182.87

Figure 2.5-3g Nozzle Servo

TABLE 2.5-5

TYPE PW/B SERVO VALVE CHARACTERISTICS

COIL ALL UNITS

D.C. RESISTANCE	=	158 OHMS/COIL
RATED CURRENT	=	± 20 ma
MAX CURRENT	=	± 57 ma
COIL CONFIGURATION	=	DUAL PARALLEL AIDING
INDUCTANCE	=	.238 HENRIES/COIL

VALVE CHARACTERISTICS

UNIT	GAIN (NOMINAL)	NULL BIAS	+ RATE LIMIT	- RATE LIMIT	SERVO OPEN LOOP GAIN
RCVV	-6. DEG/SEC/MA	-4. MA	+120. DEG/SEC	-120. DEG/SEC	40. SEC^{-1}
CIVV	+6. DEG/SEC/MA	-4. MA	+120. DEG/SEC	-120. DEG/SEC	10. SEC^{-1}
SSV	+7.75 DEG/SEC/MA	-4. MA	+155. DEG/SEC	-155. DEG/SEC	20. SEC^{-1}
WFG	+25.5 DEG/SEC/MA	-4. MA	+510. DEG/SEC	-510. DEG/SEC	20. SEC^{-1}
WFAC	+8. DEG/SEC/MA	-20. MA	+160. DEG/SEC	-160. DEG/SEC	20. SEC^{-1}
WFAD	-8. DEG/SEC/MA	-20. MA	+160. DEG/SEC	-160. DEG/SEC	20. SEC^{-1}
CENC	-5.63 DEG/SEC/MA	-6. MA	+112.5 DEG/SEC	-112.5 DEG/SEC	20. SEC^{-1}

TABLE 2.5-6a

PROFIT RESOLVER DEFINITION

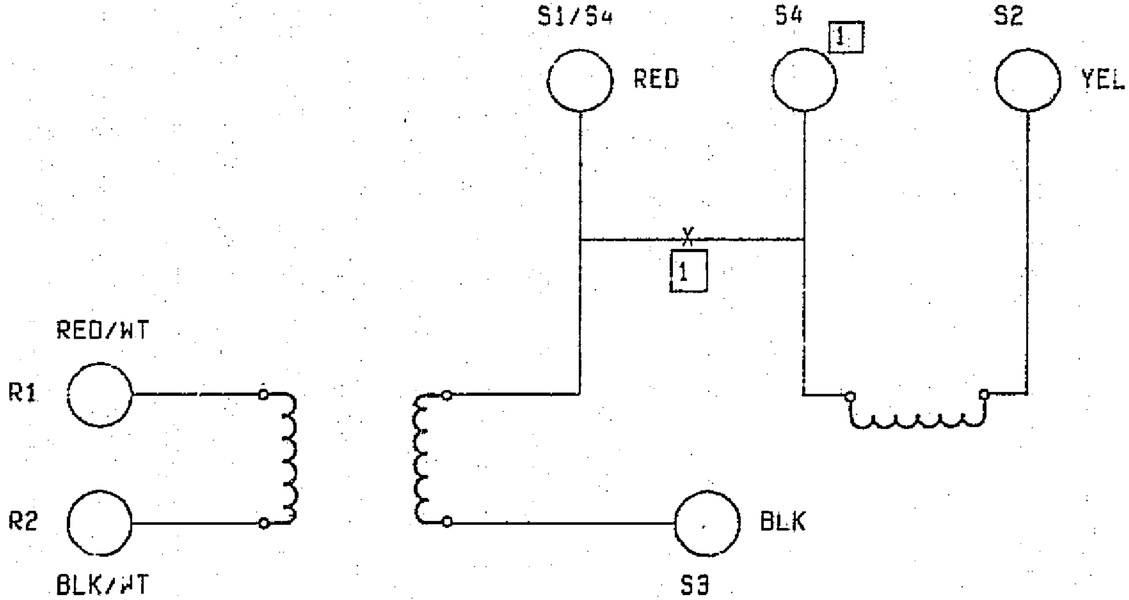
Primary voltage	7 volts
Primary frequency	1460 Hz
Input Current	.010 amp
Input Power	.015 watt
Impedance ZRO	128 plus J572
ZSO	28 plus J155
ZSS	28 plus J14
Output Voltage	3.5 volts
DC Resistance (rotor)	56.8 ohms ±10%
DC Resistance (stator)	5.9 ohms ±10%
Phase Shift	5.6 degrees

As Defined in DEEC Spec Bendix 184659

Voltage and Frequency	9 V, 1000 Hz (18 V, 1000 Hz max.)
Current	.0224 amps ±10%
Power	.044 watts ±20% unloaded
Impedance - Nominal ZR	95 + J392
ZS^o	18.6 + J106
ZS^o_s	22.5 + J9.5
Dielectric	400 Vo rms 1 min. 60 Hz
Insulation Resistance	50 megohms min. @ 500 VDC
Secondary Voltage	4.5 ±3% volts
Phase Shift	8.5 degrees lead to no load
Electrical Error	±7 minutes max.
Null Voltage Total	30 millivolts max.
D.C. Resistance Rotor	56.8 ohms ±10%
Stator	7.5 ohms ±10% each winding

As Defined for IPCS Bendix 184783

Based on conversation with Jim Rupp at Bendix, 184659 and 18473 are electrically identical. Thus PROFIT will continue to use 9V/1 Khz excitation as on IPCS.



RESOLVER EQUATION:

E (S1-S3) = Ø.5E (R1-R2) COS θ   E (S4-S2) = Ø.5E (R1-R2) SIN θ

WHERE θ IS THE MECHANICAL SHAFT ANGLE AS VIEWED FROM THE SHAFT END, INCREASING IN THE CCW DIRECTION, AND WHERE ZERO DEGREES (NOT OBTAINABLE) IS DEFINED AS THE POSITION WHERE E (S4-S2) IS ZERO AND INCREASES IN PHASE WITH E (R1-R2) WITH CCW ROTATION.

$\boxed{1}$ MAIN FUEL RESOLVER ONLY TO PERMIT ROTATION IN EXCESS OF 9Ø DEGREES.

TABLE 2.5-6b PROFIT RESOLVER SCHEMATIC

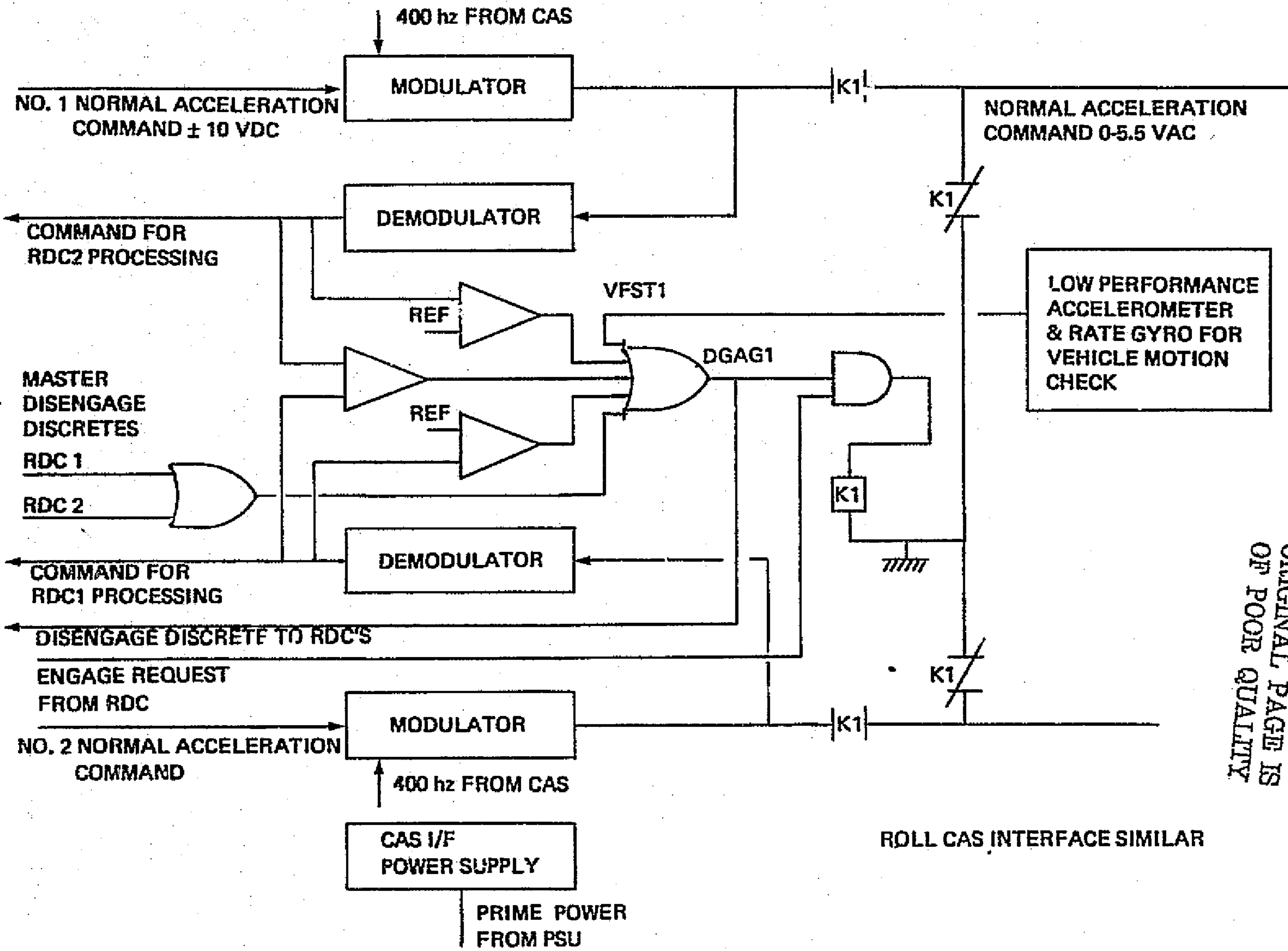


Figure 2.5-4. Pitch CAS Interface

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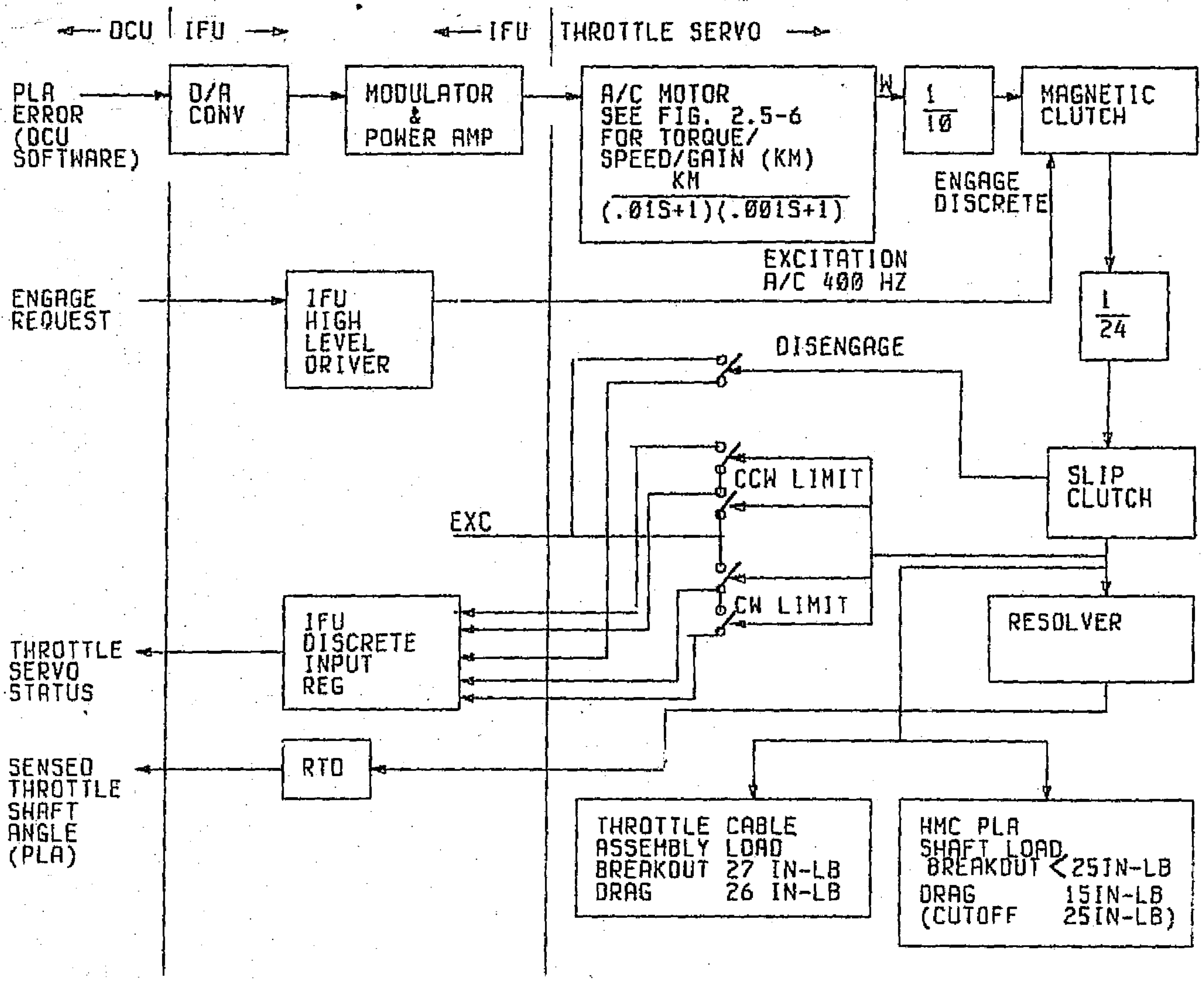

Figure 2.5-5. Autothrottle Servo Diagram

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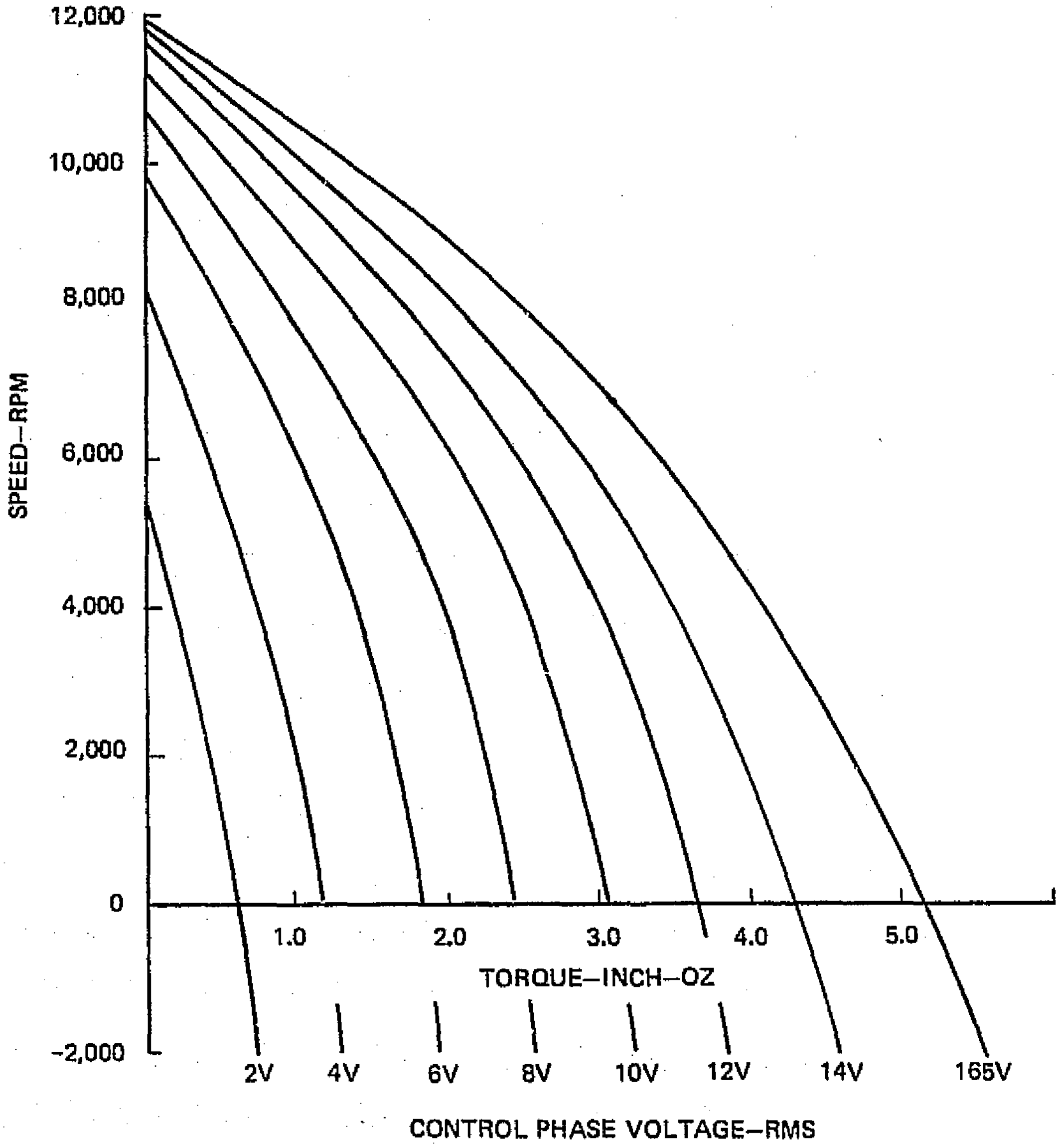


Figure 2.5-6. Typical Motor Speed Torque Curve

2.5.2 Control Sensors

There are three types of engine instrumentation, tachometers, pressure transducers, and thermocouples. Transducer selection is dictated by IFU compatibility, IPCS experience, and availability of F-100 BØM hardware.

Engine speed information is provided by two different BØM tachometer types. N2 information is obtained from a winding on the engine generator. N1 information is obtained from a hub mounted magnetic impulse tachometer. Characteristics of these devices are shown in Table 2.5-7. IFU modifications required to accommodate them are discussed in Section 4.6.

Engine temperature information is supplied by an array of thermocouples, Figure 2.5-7 A separate solid state cold reference is provided for each measurement by the cold reference box, used on IPCS in both the airplane instrumentation system and the IPCS system. The cold reference box is installed in a relatively benign area forward of the engine bay. A relatively high reference temperature is provided for the FTIT thermocouple to keep its output voltage within the ± 30 mv range of the low level A/D converter.

Engine pressure information is obtained from strain guage transducers similar to those successfully used on IPCS, Table 2.5-8. A system error analysis using tolerance data obtained from IPCS has not been performed to date but will be required. Sensor performance can be improved, if necessary by, installing thermocouples in the transducer box assembly which will house the strain guage transducers and by more frequent ground calibration checks of the transducers.

Engine face pressure (P2), critical in measuring engine pressure ratio (EPR), is obtained from a quartz crystal pressure transducer plumbed to a hub mounted pickup. Figure 2.5-8 depicts the arrangement of the engine pressure and temperature probes.

TABLE 2.5-7

TACHOMETER INTERFACES

N1 TACHOMETER

Fan Speed (N_1) signals are supplied form a dual element magnetic sensor mounted to detect the frequency of pulses generated by 38 magnetic lobes in the engine N_1 rotor assembly.

Signal Range:	1,800 r/min to 15,000 r/min
Frequency Range:	1139.94 Hz to 9499.5 Hz
Waveform Output:	Waveform is a distorted sinusoid, fundamental frequency = 0.6333 N_1.
Voltage Output:	Minimum peak positive pulse is 300 millivolts at N_1 = 1420 r/min. Maximum peak positive should not exceed 60 volts at N_1 = 12700 r/min.

N2 TACHOMETER

The high compressor speed (N_2) signal is derived from the single phase generator power winding that supplies the EEC 20 volt power. The generator has nine-pole pairs and is geared to the compressor rotor at a ratio of 1.073 to 1.

Therefore: frequency (Hz) = 1.073 (9/60) N_2 (r/min) = 0.16095 r/min.

Signal Range:	7300 r/min to 18000 r/min
Frequency Range:	1174.935 Hz to 2897.1 Hz
Voltage Output:	20 volts min. at 3700 r/min. 25 volts max.
Waveform:	Sinusoid

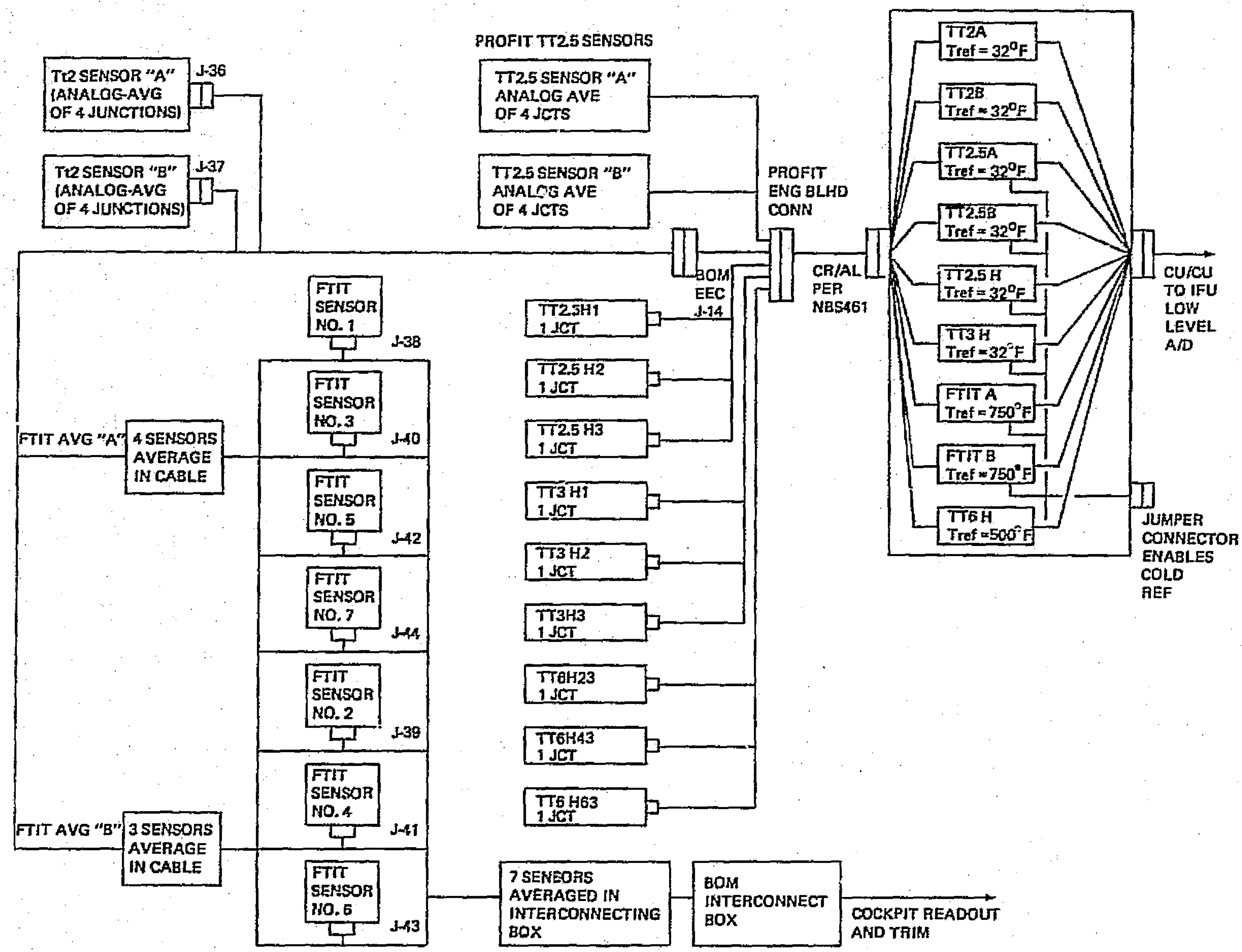
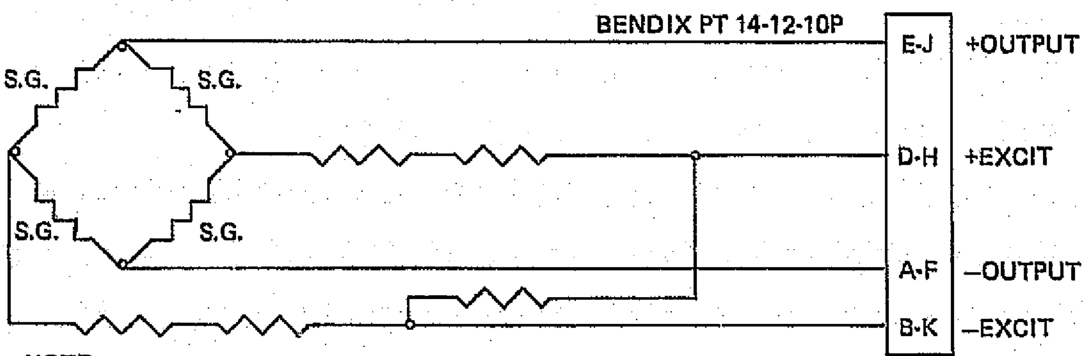


Figure 2.5-7. Engine Thermocouple Array and Interconnection

Table 2.5-8. M-B Alinco Pressure Transducer Characteristics

Sensitivity (full scale)	3.0 mV/V ± 0.25%
Recommended excitation	10 volts AC or DC
Max excitation	20 volts AC or DC
Input resistance @ 77°F (ohms)	350 ± 3.5 ohms
Output resistance @ 77°F (ohms)	350 ± 3.5 ohms
Insulation resistance @ 77°F	5,000 megohms @ 50V
a) Non-linearity* (% FS max)	±0.15
b) Hysteresis (% FS max)	0.1
c) Non-repeatability (% FS max)	±0.05
a, b, & c combined (% FS max)	±0.2
Zero pressure output @ 77°F	±1.0
Compensated temp range	−100°F to +250°F
Sensitivity shift w/temp	+0.25% FS/100°F
Zero shift with temp	+0.25%/FS/100°
Safe over pressure	> 500% FS
Maximum over pressure	> 2,000 PSI
Natural frequency (kHz, approx)	~ 3 to 8 kHz
Output from vib (max % FS/g)	~ 0.025



NOTE:

DATA ARE TYPICAL FOR 300 psia TRANSDUCER.
PARAMETERS VARY WITH TRANSDUCER RANGE.

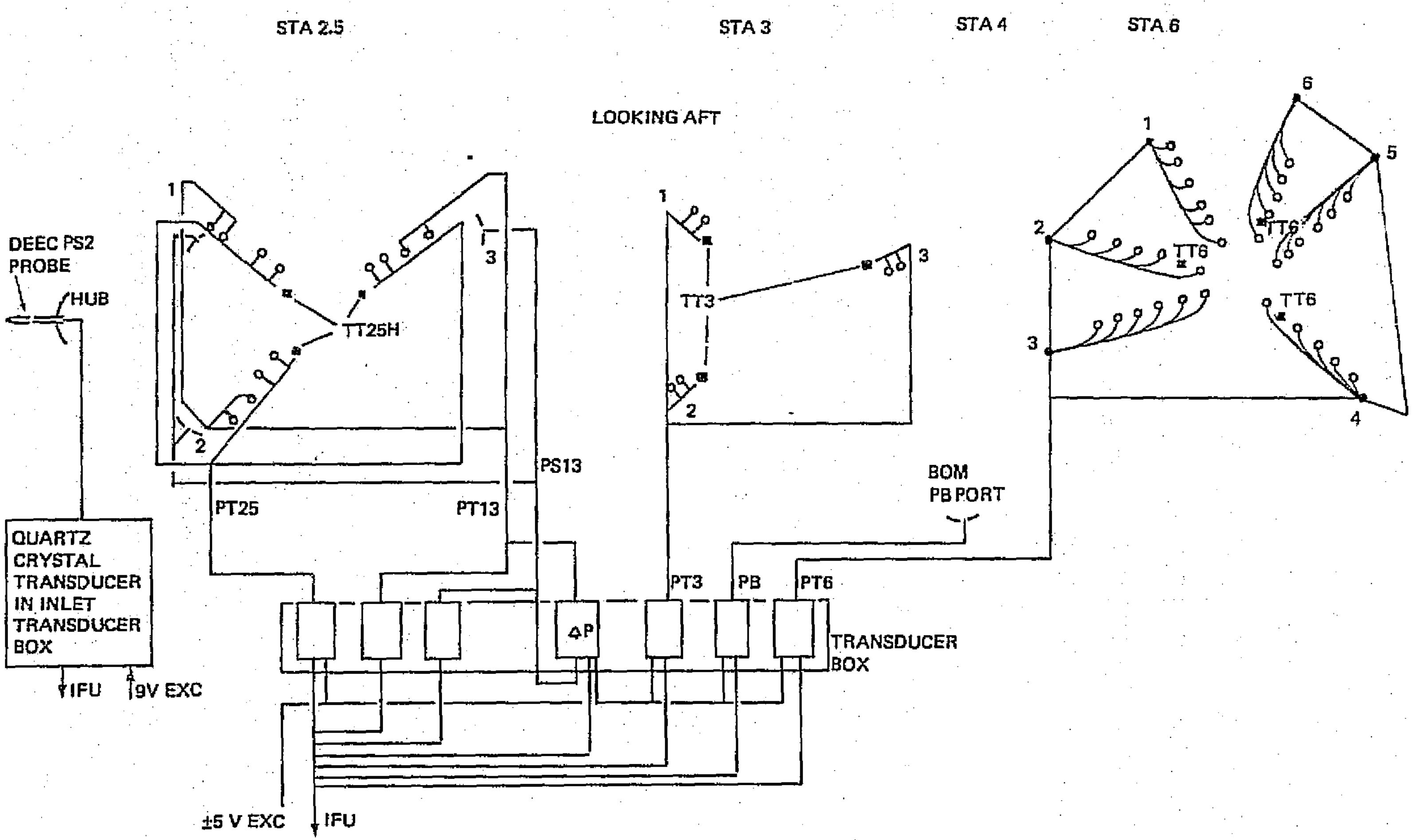


Figure 2.5-8. Engine Pressure Rakes, Manifolding, and Transducers

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The inlet transducer locations and plumbing are shown in Figure 2.5-9. The four inlet pressures are measured by quartz crystal transducers connected to BØM pneumatic lines in place of the BØM vibrating can transducers. Quartz crystal transducers were used successfully on IPCS and have the advantage, relative to vibrating can transducers, of being relatively temperature insensitive, Table 2.5-9, and IFU compatible.

The BØM total temperature probe connections to the EAIC are removed and the probes are wired to their respective IFU inputs and excitation. Characteristics of these probes are shown in Figure 2.5-10.

The BØM angle of attack probe connections to the EAIC are removed and the probes are wired to their respective IFU inputs and excitation. Characteristics of these probes are shown in Figure 2.5-11.

Figure 2.5-9 does not draw distinctions with regard to wiring and connectors. It is probably desirable to leave existing BØM cables to the EAIC intact and then merge angle of attack, total temperature and pressures into a single harness at the inlet pressure transducer box, see section 4.1.4, rather than breaking into BØM cables at the individual transducers.

2.5.3 PROFIT Digital Data Interfaces

There are three digital data links between PROFIT and its environment - the T/M uplink and T/M downlink and the F-15 Central Computer bus. All three systems have a bit parallel time division multiplexed interface with the IFU. Each system operates through a different PROFIT system bus.

The telemetry downlink provides a means for DPCU data to be incorporated in the airplane PCM bit stream (see Section 2.7). The airplane PCM system requests parallel data from the DPCU on an interrupt basis and DCU software places the desired data on the output bus for access by the PCM system. The IFU provides necessary buffering between the DCU and PCM system. This system was used on IPCS and is discussed in Reference 1.

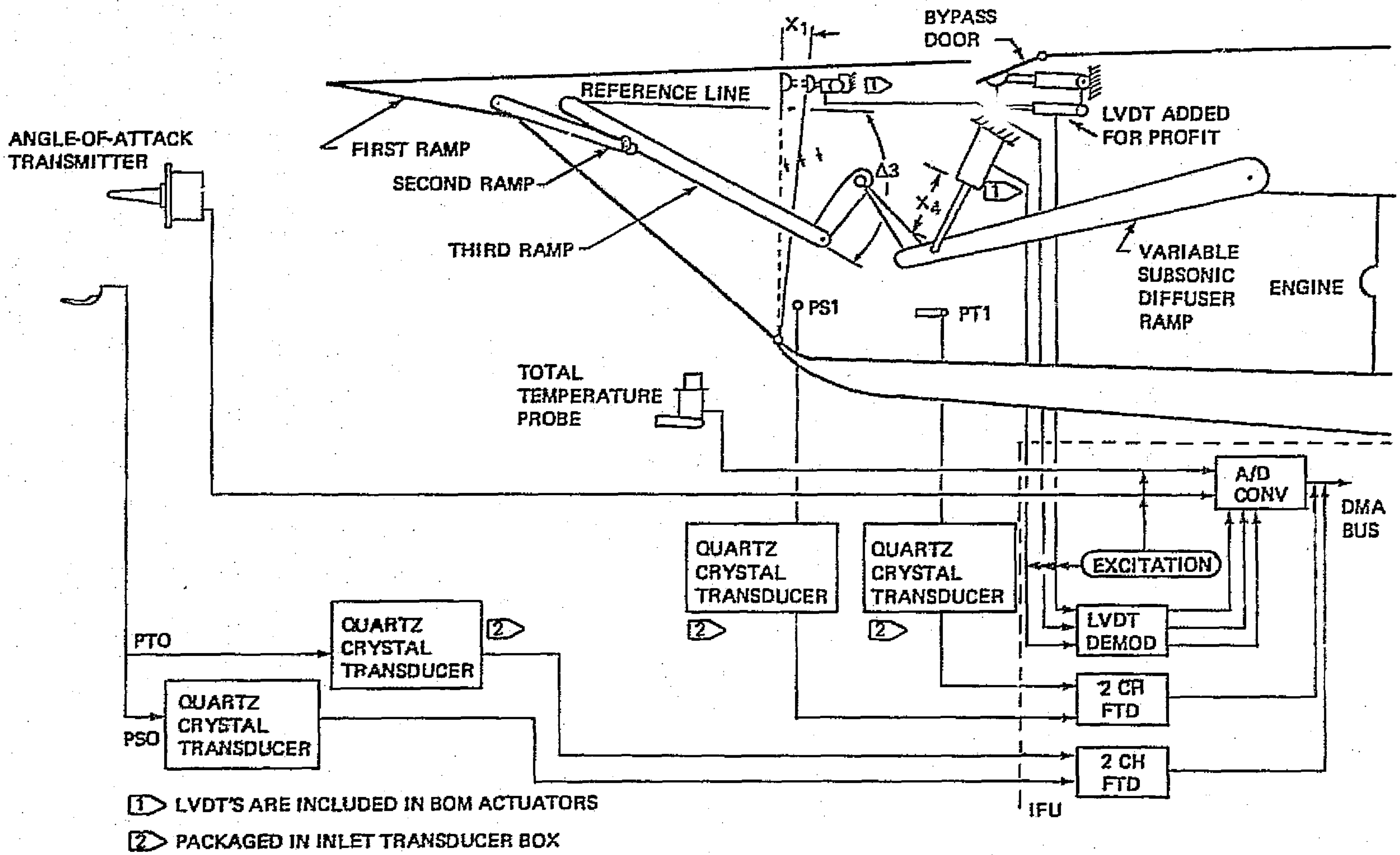


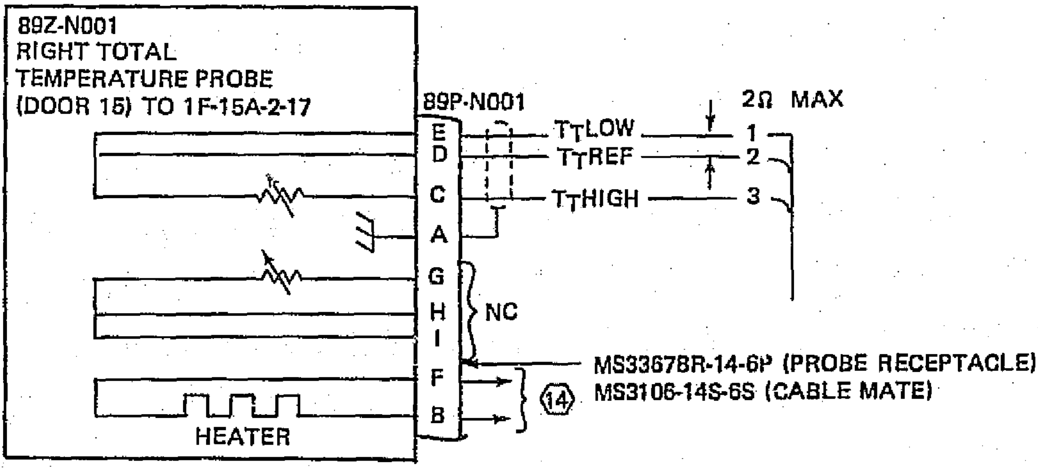
Figure 2.5-9. Inlet Transducers

TABLE 2.5-9
INLET PRESSURE TRANSDUCER CHARACTERISTICS

Repeatability	0.005% FS
Hysteresis	0.005% FS
Null Stability (6 months)	0.008% FS
Temperature Null Shift	0.0004%/^{o}F (0.0007%/^{o}C) FS
Temperature Span Shift	0.0026% of Reading/^{o}F (.0047%/^{o}C) FS
Acceleration Sensitivity	0.0008%/G FS
Vibration Sensitivity	Negligible FS
Nominal Frequency Excursion (Zero to Full Scale)	40 kHz to 36 kHz
Operational Temperature Range	-65^{o}F to 225^{o}F (-54^{o}C to 107^{o}C)
Operational Vibration Spectrum	MIL-E-5400-III
Power Requirements	6V, 0.001A
Size	0.89 x 1.56 x 1.56 in. (2.26 x 3.97 x 3.97 cm.)
Weight	6 ounces (0.17 Kgm)
Output Impedance	<200Ω
Connector	Pigtail
Pressure Fitting	MS-33656-2
Max Overpressure	1.2 * FS

PART NUMBER [1]	RANGE	APPLICATION
245-A-002	0-45 PSIA	PTO
230-A-002	0-30 PSIA	PSO
245-A-002	0-45 PSIA	PT1
230-A-002	0-30 PSIA	PS1
245-A-002	0-45 PSIA	PT2

[1] Paroscientific transducers typical



RIGHT TOTAL TEMPERATURE PROBE
LEFT PROBE SIMILAR

T °C		RATIO	T °C		RATIO	T °C	RATIO
-200		0.16996	80		1.31502	370	2.39402
-190		0.21374	90		1.35388	380	2.42946
-180		0.25719	100		1.39261	390	2.46479
-170		0.30032	110		1.43123	400	2.50000
-160		0.34314	120		1.46973	410	2.53510
-150		0.38569	130	I/F	1.50810	420	2.57007
-140		0.42799	140	RANGE	1.54636	430	2.60492
-130		0.47004	150		1.58451	440	2.63967
-120		0.51186	160		1.62254	450	2.67429
-110		0.55345	170		1.66049	460	2.70880
-100		0.59485	180		1.69824	470	2.74319
- 90		0.63607	190		1.73592	480	2.77746
- 80		0.67709	200		1.77348	490	2.81161
- 70	— 73.4	0.71795	210		1.81092	500	2.84565
- 60		0.75866	220		1.84825	510	2.87957
- 50		0.79921	230	— 232	1.88546	520	2.91338
- 40		0.83963	240		1.92254	530	2.94705
- 30		0.87992	250		1.95951	540	2.98062
- 20		0.92007	260		1.99637	550	3.01407
- 10		0.96009	270		2.03311	560	3.04741
0	I/F	1.00000	280	PROBE	2.06972	570	3.08062
10	RANGE	1.03979	290	RANGE	2.10622	580	3.11371
20		1.07947	300		2.14261	590	3.14670
30		1.11901	310		2.17888	600	3.17956
40		1.15845	320		2.21502	610	3.21231
50		1.19777	330		2.25106	620	3.24493
60		1.23698	340		2.28607	630	3.27744
70		1.27606	350		2.32276	640	3.30984
			360		2.35845	650	3.34211

RESISTANCE RATIO = RT/RO
R_0 = 50 Ω

MAX SENSING CURRENT = 15 ma
SEE MIL-P-27723 FOR FURTHER DETAILS

Figure 2.5-10. Total Temperature Probe Characteristics

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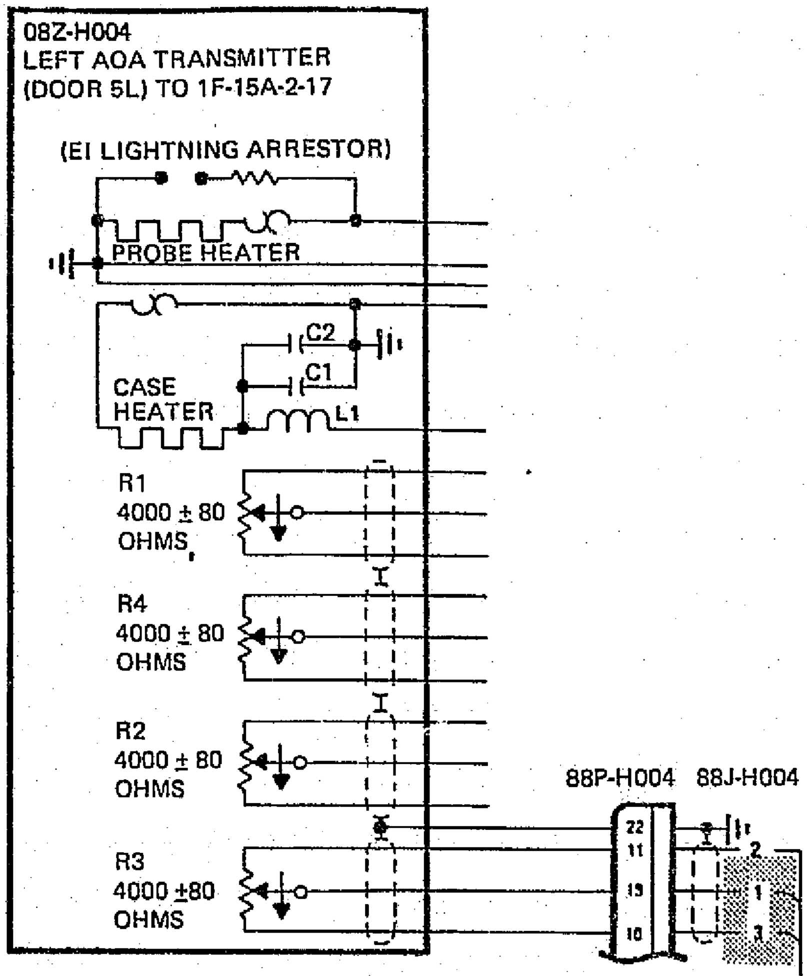

LEFT UNIT SHOWN
RIGHT IS SIMILAR

POTENTIOMETER CHARACTERISTICS

TOTAL RESISTANCE	4000 OHMS ± 2%
MAXIMUM EXCITATION	35 VOLTS
SCALE FACTOR	9/7% ± 0.005% TOTAL RESISTANCE PER DEGREE OF CONE TRAVEL
INDEPENDENT LINEARITY	0.15% OF TOTAL RESISTANCE
RESOLUTION	0.04% OF TOTAL RESISTANCE
POWER RATING (MINIMUM)	0.75 WATTS CONTINUOUS AT 70°C

ALIGNMENT

THE POTENTIOMETER SHALL BE ADJUSTED SO THAT THE AERODYNAMIC CENTER CORRESPONDS TO A WIPER POSITION OF 50% ± 0.15% OF THE TOTAL RESISTANCE.

Figure 2.5-11 Angle of Attack Transmitter Characteristics

The telemetry uplink is a new feature added to the IPCS hardware for PROFIT to permit ground manipulation of the onboard software and system outputs. Its design is documented in Section 4.2.

The central computer data bus of the F-15 contains, or can contain if the appropriate peripherals are installed, an overwhelming amount of information. The nominal set of information available on the S/N 2 airplane is shown in Table 2.5-1. An interface for converting the bus serial data to parallel, selecting a menu of data from that on the bus, and buffering it for DPCU access via the DMA bus has been designed, assembled, and tested. The design of this interface is discussed in Section 4.4.

2.5.4 PROFIT Digital Computer Unit (DCU)

The PROFIT DCU (HDC-601) consists of a central processor unit (CPU), 16K x 16 bit core memory, power supply, 2.5 Mhz crystal clock, and associated wiring, mounting, and cooling facilities. The CPU is constructed of TTL flat-pack circuitry mounted on 13 printed circuit (P/C) cards. The CPU is not packaged along functional lines; e.g., the A register is a part of the CPU P/C cards A1, A3, A5, and A7. The CPU contains timing control, interface addressing (I/O and interrupt channels), direct-memory access (DMA), and arithmetic processing functions. The functional elements of the CPU are shown in Table 2.5-10. Timing circuits provide signals to sequence data processing. Control circuits interpret commands and ensure that the required circuits are activated to accomplish a given processing operation. Interface circuits provide the capability to transfer computer compatible data to and from the external devices. Addressing circuits permit random access of memory and the means by which addresses can be altered. Arithmetic circuits, incorporating double precision capability, provide parallel processing of arithmetic functions in two's complement form. Eight-four instructions are provided.

TABLE 2.5-10

CENTRAL PROCESSOR FUNCTIONAL ELEMENTS

A Register

B Register

Program Counter

Memory Address (Y) Register

External Priority Interrupt

External Interrupt Register

Discrete Decode Function

Instruction Decode

Timing

Direct Input/Output Channel (DIO)

Direct Memory Access Channel (DMA)

Adder

F Register (4 Bits of OP Code)

M Register

Shift Counter

Index Register

Interrupt Mask Register

Interrupt Control

The DCU power supply is a switching regulator operating at 10 kHz from a Royer oscillator. The 5-Vdc output is used for feedback control of the regualtor. The other output voltages track the 5-Vdc power as a function of the switching regulator power transformer turn ratios. Protection and monitor circuits are provided to protect against over voltage, over current, and to provide normal power up/down control.

The 16K (16384 words) core memory supplied by Electronic Memories and Magnetics Inc. is a cubic model SEMS 9. Word size is 16 bits, and there is no hardware parity bit. Construction is of the coincident current configuration with the inhibit current and sense lines as a common line for each bit. The read/write cycle time for the memory is 1.2 microseconds. Section 4.3 documents expansion of the DCU memory capacity from 16K words to 32K words.

2.5.5 PROFIT Command and Control

As shown in Table 2.5-11 command and control functions are organized into different categories to assure correct identification of critical ones and rational allocation of all of them. Three categories of functions are identified - automatic status and engage functions, uplink command functions, pilot command functions.

Automatic status and engage functions include automatic failure detection and response, and control system transfer and engage logic. Uplink command functions are at this time undefined but will include trajectory commands and gain scheduling. The uplink will not be provided with the capability to force system disengagement or engagement unless specific program requirements are identified which would make this function desireable. Pilot command functions include discrete activities such as system on/off engage/disengage and mode selection and continuous functions such as trajectory command generation and system gain variation.

TABLE 2.5-11

COMMAND AND CONTROL FUNCTIONS

STATUS/ENGAGE	PILOT COMMANDS	UPLINK COMMANDS	
Engage Permission	Power On/Off	Basic	Gain Change
System Status	Mode Engage Request		Inertial Trajectory
Auto Disengage	Mode Selection		Throttle Position
Auto Power Off	Mode Disengage	Advanced Operations	Logic Changes
	Master Disengage		Algorithm Changes
	Gain Change		
	Manual Trajectory Tracking		
	Manual Throttle		

A preliminary tabulation of engage, disengage criteria is presented in Table 2.5-12. This will be expanded as studies continue.

2.6 PROFIT SYSTEM SOFTWARE

The goal of the PROFIT system is to reduce the cost of research flight testing by reconfiguring software rather than hardware and thus increasing utilization of the flight test vehicle. In order to achieve this goal, PROFIT software must be readily adaptable to changing research requirements and provide overhead functions - data processing, safety logic, sensor processing, in modular form so that institution of differing research programs will require modification or substitution of related modules rather than complete reprogramming. Expansion of the DCU memory to 32K relaxes somewhat the emphasis on optimum core utilization. Conversely IPCS experience and EEC code permit use of core optimum coding in some areas since requirements in these areas are well understood.

The PROFIT SOFTWARE SYSTEM DEFINITION DOCUMENT, Reference 2, provides a detailed software definition. The intention of the following paragraphs is to provide insight into the software structural concept and the interfacing of hardware and software functions.

2.6.1 Software Concept

PROFIT software is constructed of modules, see Figure 2.6-1. By defining the input data base available to applications modules, the output data base generated by them and the status engage interface requirements for them the systems integrator and applications module developer can coordinate in such a manner as to permit development of applications modules independent of each other and the host program.

TABLE 2.5-12

STATUS AND ENGAGE PRELIMINARY SUMMARY

ENGAGE ALLOWED IF:	Master Disengage false and Track Criteria for selected modes are met and Sensors required for selected mode are OK
MASTER DISENGAGE TRUE IF:	Pilot Request or Auto Power Off
MODE DISENGAGE TRUE IF:	Mode Red Line exceeded or Mode related critical component failure - Sensors - Central computer bus parity error - Uplink I/F checksum error
AUTOMATIC SYSTEM POWER OFF IF:	Software cycle incomplete or IFU power failure or DCU power failure or Electronics overtemp or Hardware bite failure or DCU self check failure

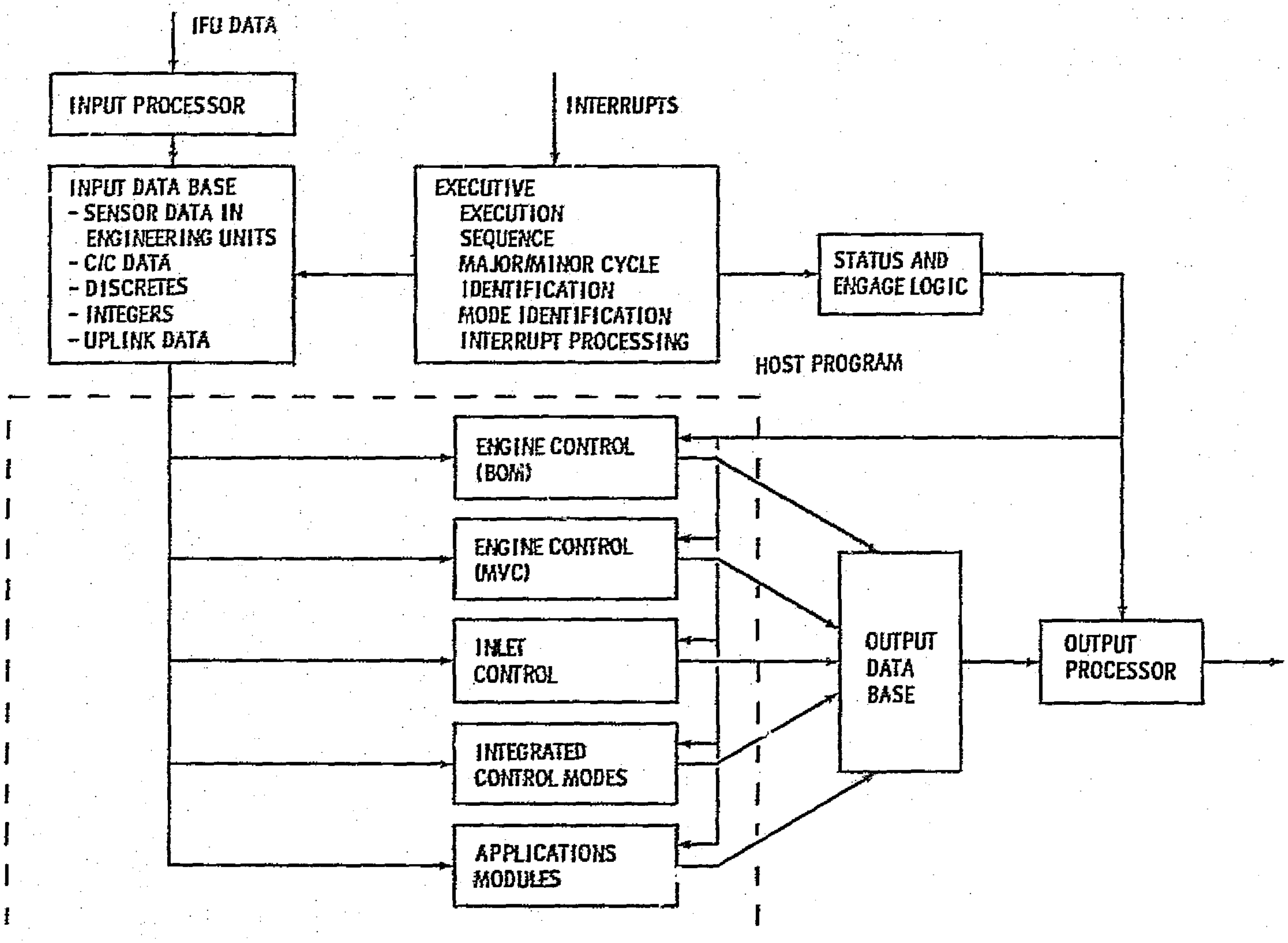

Figure 2.6-1. Flight Software Module Concept

The input processor converts raw IFU data to binary scaled engineering units, or integers or discrete flags, and stores the data in sector 0 (memory locations '0 through '777) for access by all modules. These data are filtered to varying degrees either by analog prefilters or by averaging of data samples acquired at higher than the basic program cycle (major cycle) rate.

Additionally all input data are limit checked to identify gross failures, broken wires and the like. A suitable failure word is contained in the data base to permit other modules to recognize relevant failures. In addition to sensor generated input data two sets of digital multiplexed data are transferred to the input data base. These are central computer bus data and uplink data. Table 2.5-1 defines the available data. Central computer bus data is not failure checked, although a bus parity error is identified in the failure word and c/c bus data updating is stopped until the pilot resets the c/c bus system. Uplink data frames are checksummed before transfer to the input data base. A checksum error will cause the last valid data to stay in the input data base and set a flag in the failure word. Again pilot action is required to clear the system.

Four typical application module types are shown in Figure 2.6-1. Any, some, or all of these may be incorporated in the flight software depending upon current research program emphasis. Additionally as yet unidentified applications modules may be incorporated. In general these modules will process input data to create commands for engine, inlet, or airframe effectors and cockpit displays. The commands will be placed in the output data base from which the output processor will obtain them, convert them to IFU compatible format and output them to the IFU if the Status & Engage Logic has enabled control of the commanded effectors.

The Status and Engage Logic working through the Output Processor controls engagement of plant effectors in response to information from the input data base. This information includes pilot engage, disengage requests, sensor failure information generated by software, match between plant state and

controller requested state, and hardware BITE failure indications. This logic is paralleled in hardware such that engagement can only be achieved if both a software and a hardware path are enabled.

The EXECUTIVE CPC provides sequencing of both the host program and the applications modules. With reference to Figure 2.6-2, each real time clock interrupt causes a pass through the executive, marking the end of a minor cycle. The executive counts minor cycles and determines the completion of a major cycle. All control computations and control data input/output are completed at least once each major cycle. Other functions, primarily digital telemetry data/input/output are carried out through the DCU interrupt structure on a basis asynchronous to the real time clock. The DIO bus is used under interrupt control to interface with the telemetry system. All other data transferred into the memory enters through the DMA bus permitting calculations to continue as data is transferred. Care must be exercised therefore, in establishing timing between data input and control computations to insure that the desired data sample is available for the computation.

Figure 2.6-3 is a timing diagram of the major functions in the software. It serves to display the relationships between data input operations, applications module execution, and house keeping functions. The F100 engine simulation is currently configured to reflect this timing (Section 3.1). The major cycle interval shown in the figure is 60 msec. Due to restrictions on input sample intervals the next feasible major cycle interval is 90 msec.

The main fuel valve and RCVV positions are input every five msec and checked for hardover or disagreement between resolver 1 and resolver 2 (figure 2.6-4). Two sequential indicated fuel valve failures cause the status and engage logic to disengage engine control. Following fuel valve processing the N1, N2 tach data are input and accumulated for inclusion in the data base as major cycle average in the 11th minor cycle. N1, N2 data are checked for out of range on a minor cycle basis.

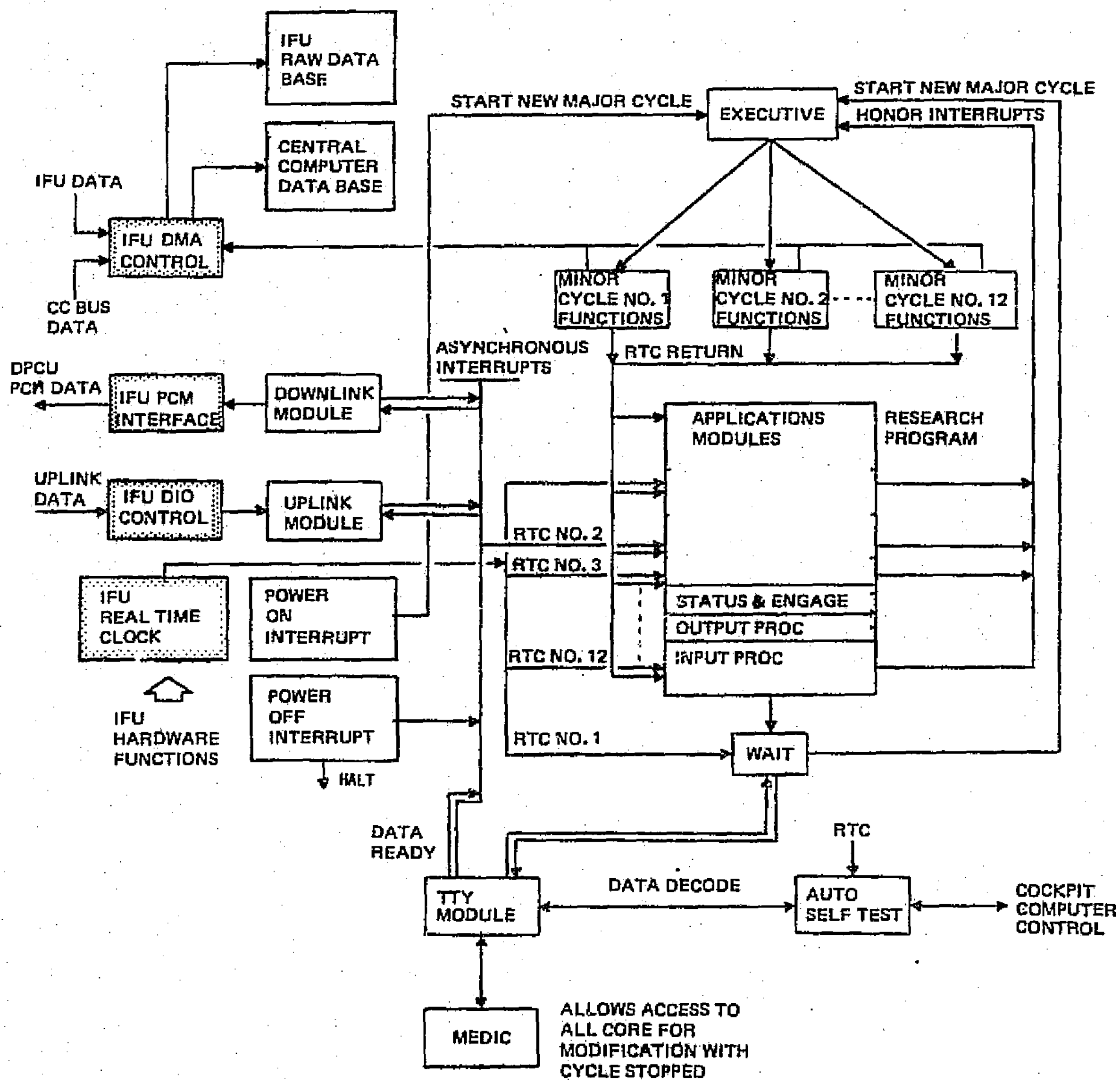

Figure 2.6-2 PROFIT Software Configuration Concept

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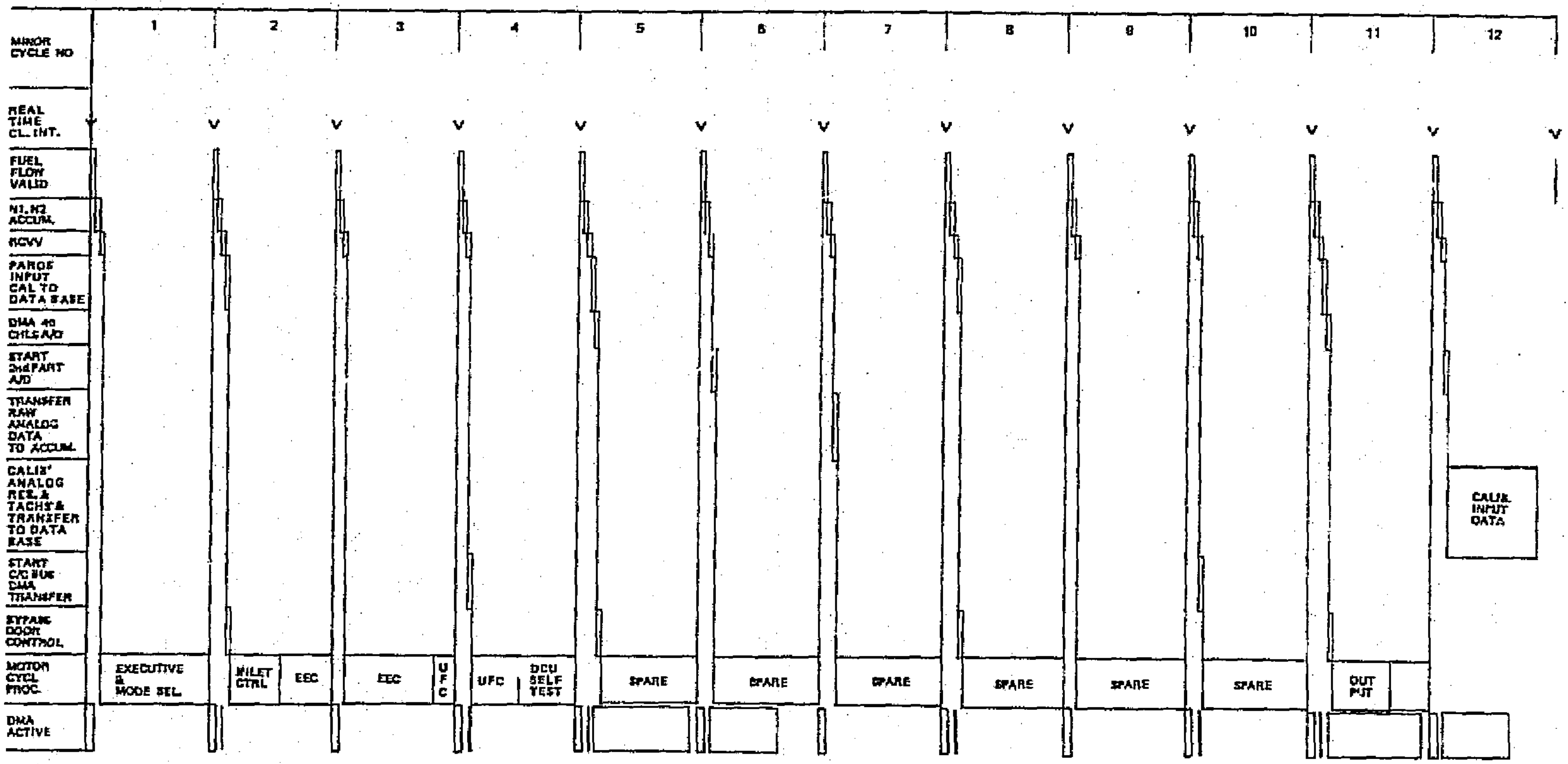

NOTES:

- DRAWING NOT TO SCALE
- UPLINK/DOWNLINK INTERRUPTS NOT SHOWN. REQ. 4.4 MSEC PROC. TIME
- DMA ACTIVE—DMA CONTROLLER IN OPERATION DATA TRANSFERS OCCUR USUALLY AT MUCH LESS THAN MAX RATE

Figure 2.6-3. PROFIT Real Time Executive Execution Sequence

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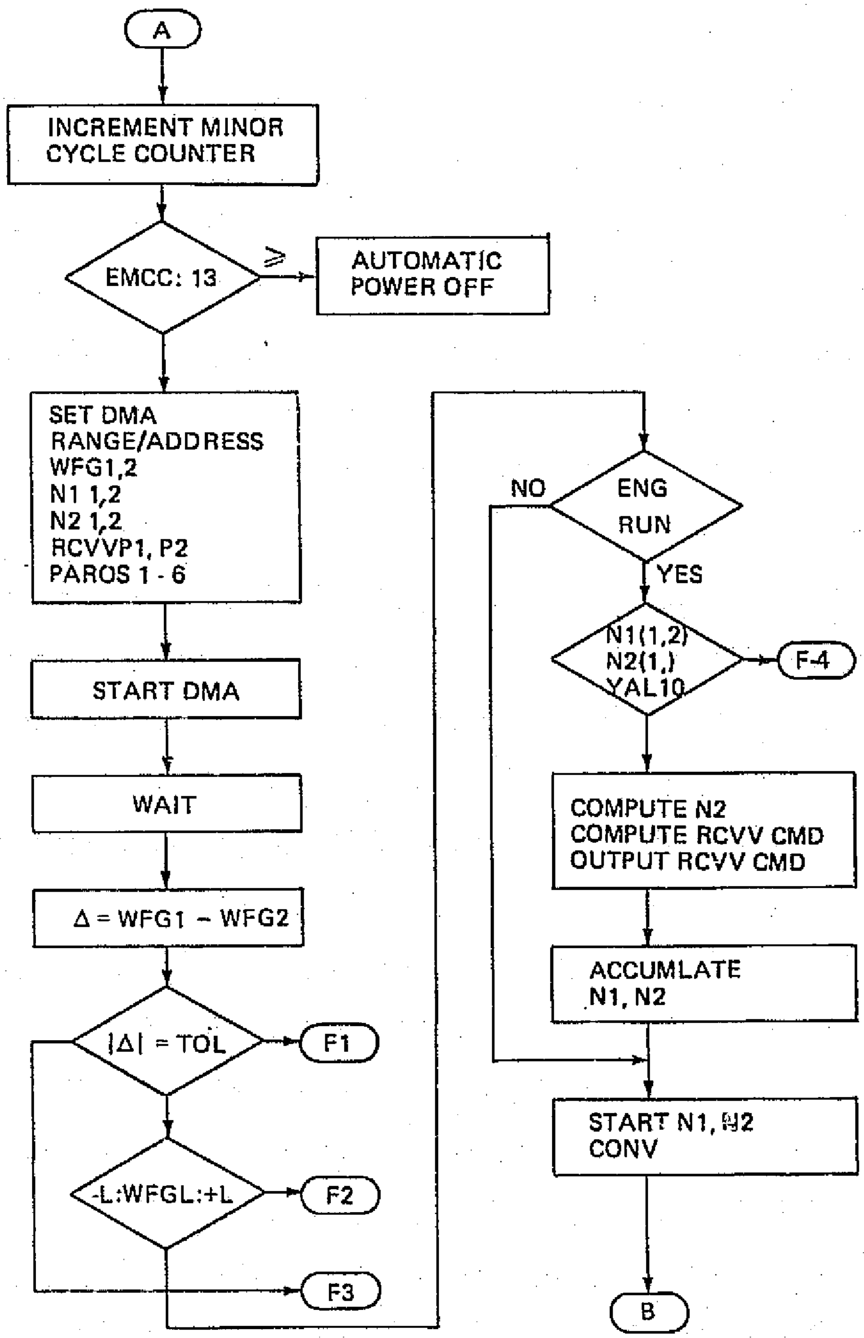

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Figure 2.6-4. Minor Cycle Executive Logic

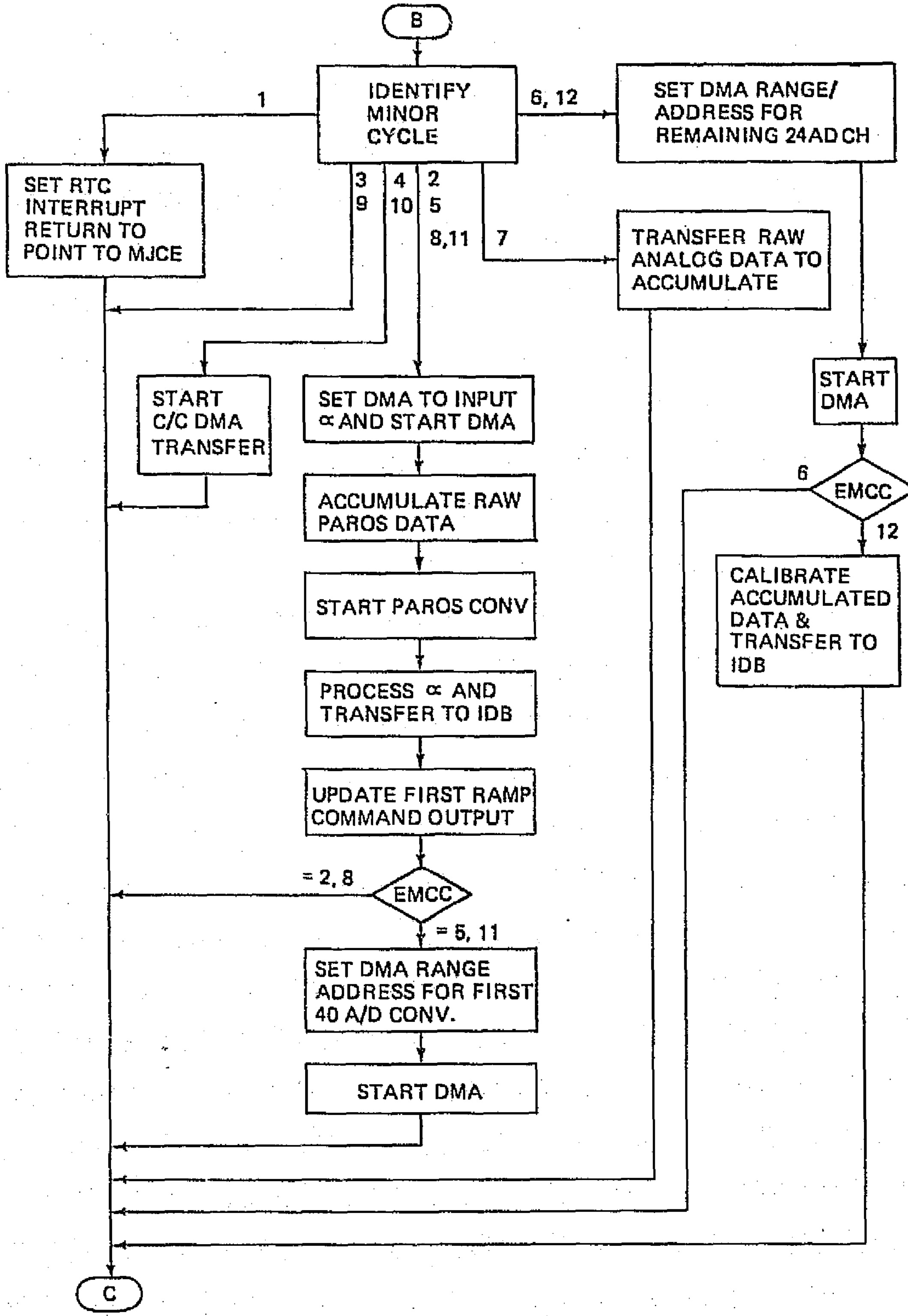

Figure 2.6-4. Continued

Quartz crystal pressure transducer data are input every 3rd minor cycle and accumulated to update the data base every major cycle. Analog data are input every 30 msec. through the DMA system. Data input during minor cycles 5 and 6 are buffered during the 7th minor cycle and then averaged with the data input during the 11th and 12th minor cycles. The bulk of sensor data conditioning is then done during minor cycle 12 and the input data base is fully updated at the completion of the major cycle. Central Computer data is input from the buffer memory (updated asynchronously at 20 SPS) during minor cycles four and ten. Uplink data and T/M data are processed on an interrupt basis as indicated. All actuator commands are output at the beginning of minor cycle one. In addition RCVV commands are output every minor cycle to improve system response at high Q conditions. Bypass door control processing and control output may also be output more than once per major cycle.

The executive sequences execution of applications modules and executive functions with respect to the input output and interrupt processing described above. As indicated in the current timing budget substantial spare processing time is available for expanded applications modules.

2.7 DATA SYSTEM

The data processing system will rely to a great extent on the hardware and software successfully employed on the IPCS program. The primary source of data will be the RDC. Digital data are available at the rate of 1200 words per second per RDC (60 words, including a synch word, at 20 samples per second). It is likely that multiple sets of 60 words will be available to provide additional capability. The specific requirements for facility instrumentation to supplement the computer will be identified during the early part of the program. In general, facility instrumentation will be used to provide steady-state calibration, record operating conditions, identify failed control sensors, and provide backup signals for post event analysis for failed control sensors.

The majority of the data processing will be common to all the system tests. Some differences do exist between operation on the aircraft and at the ground test facilities. Paragraph 2.7.1 describes the flight system which is the basis for the system at all facilities. The system for other test facilities is discussed in paragraph 2.7.2.

2.7.1 Flight Test Data

Data from aircraft instrumentation and the two 60 word data sets from the computer systems will be recorded using an onboard CT77 PCM system. The interface between the computers and the CT77 will be the same as on IPCS. Data will be recorded on an onboard tape recorder and telemetered to the ground for recording and display. The computer data will include control sensor measurements, data from the central computer bus, variables calculated in the control, and data from the uplink. The capability will exist to change sets of parameters using a cockpit switch or uplink command. Uplink data from the Remote Augmented Vehicle (RAV) facility will be recorded separately. Figure 2.7-1 illustrates the data flow.

The telemetered data will be displayed during the flight. The specific requirements have not been defined, but some form of PROFIT system status indicators will be needed along with strip charts and possibly digital readout.

The post flight processing is also shown in Figure 2.7-1. The data from the aircraft, using the recorded telemetered data if possible, will be formatted for the CYBER computer. The CYBER program, PROGDAB, calibrates the data, merges the aircraft and RAV data, compresses and stores the data in rotating mass storage for subsequent processing. Only gross editing is required up to this point (for example not including long periods of time going to a test condition).

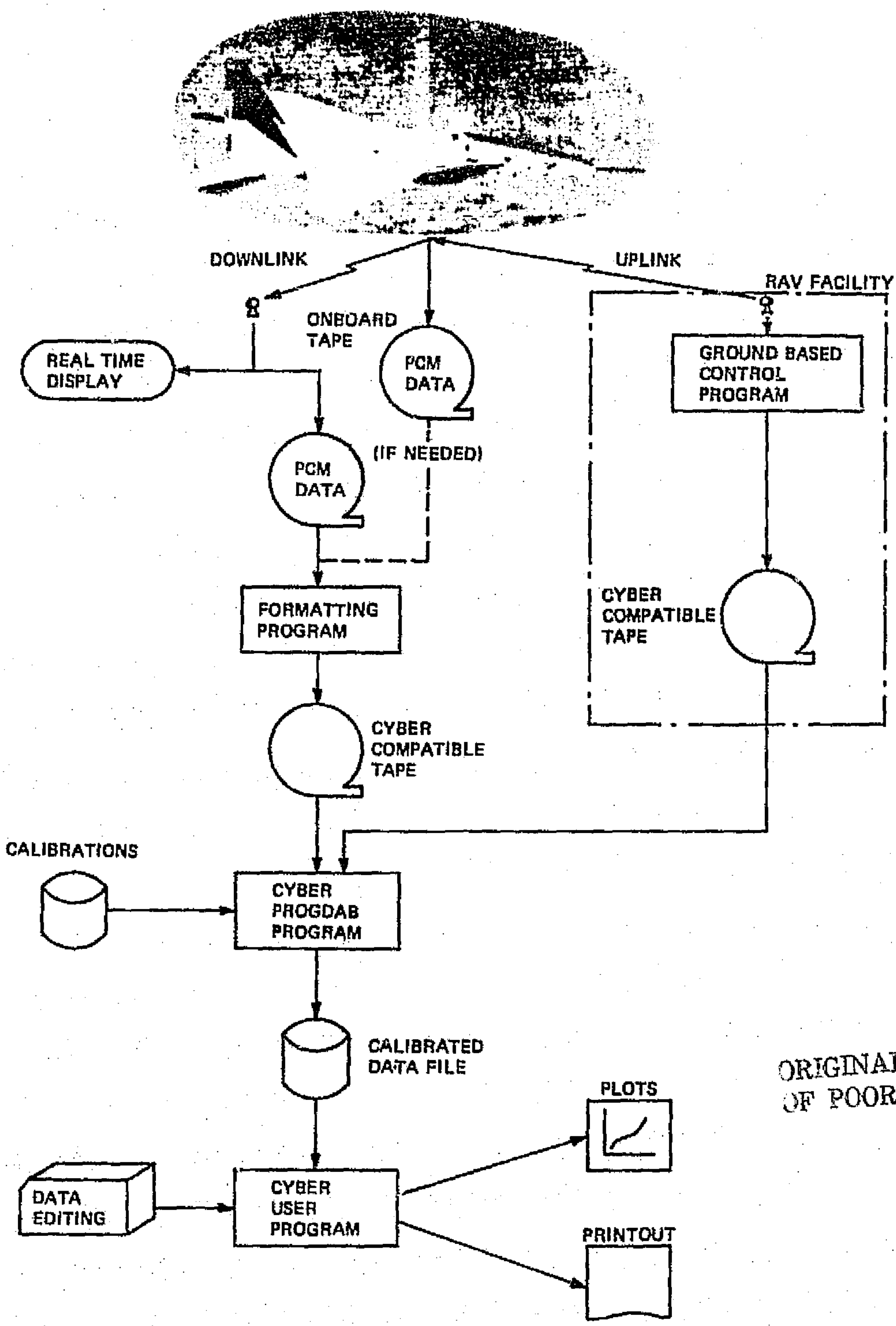

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Figure 2.7-1. Flight Test Data Flow

The last step is processing by the user program. This program will perform any required calculations and print or plot data for selected time intervals. It is at this stage that the detailed editing is done in selecting the variables and periods of time to be printed and plotted.

2.7.2 Ground Test Data

The same digital data from the control computer will be used at the ground tests. The test set recorder monitor panel will provide the necessary interrupts and receive the data. The data will be displayed on the octal readout, one variable at a time, and recorded as serial PCM data. This much of the system, shown in Figure 2.7-2, is identical to the IPCS system. Additional capability has been added to permit on-line display of the digital data. Decommutation and channel selection hardware (Section 2.8) acquire 16 of the digital variables. These data will be displayed on strip charts. Any 16 channels can be selected easily. This combined with the ability to read and decom the data from the tape recording provide rapid turn around of any of the 59 data variables during the test running. In addition the data can be read into the test set computer to provide display of a full frame of digital data.

Facility instrumentation will be recorded on the normal facility data systems. There will be sufficient control instrumentation in the PROFIT system to provide the needed transient data. Thus only steady-state facility instrumentation will be required. The plans for the ground tests presented in Section 5.1 identify some of the requirements for such instrumentation.

Post event processing of the data from the control computer will be done at DFRC. This approach greatly reduces the cost and complexity of processing the data from the ground tests. Rapid on-site availability of all the digital data is the key to this plan. Analysis of test events for trouble shooting and system debugging can be done from the control computer data and the routinely available printouts of the facility data. Post event analysis

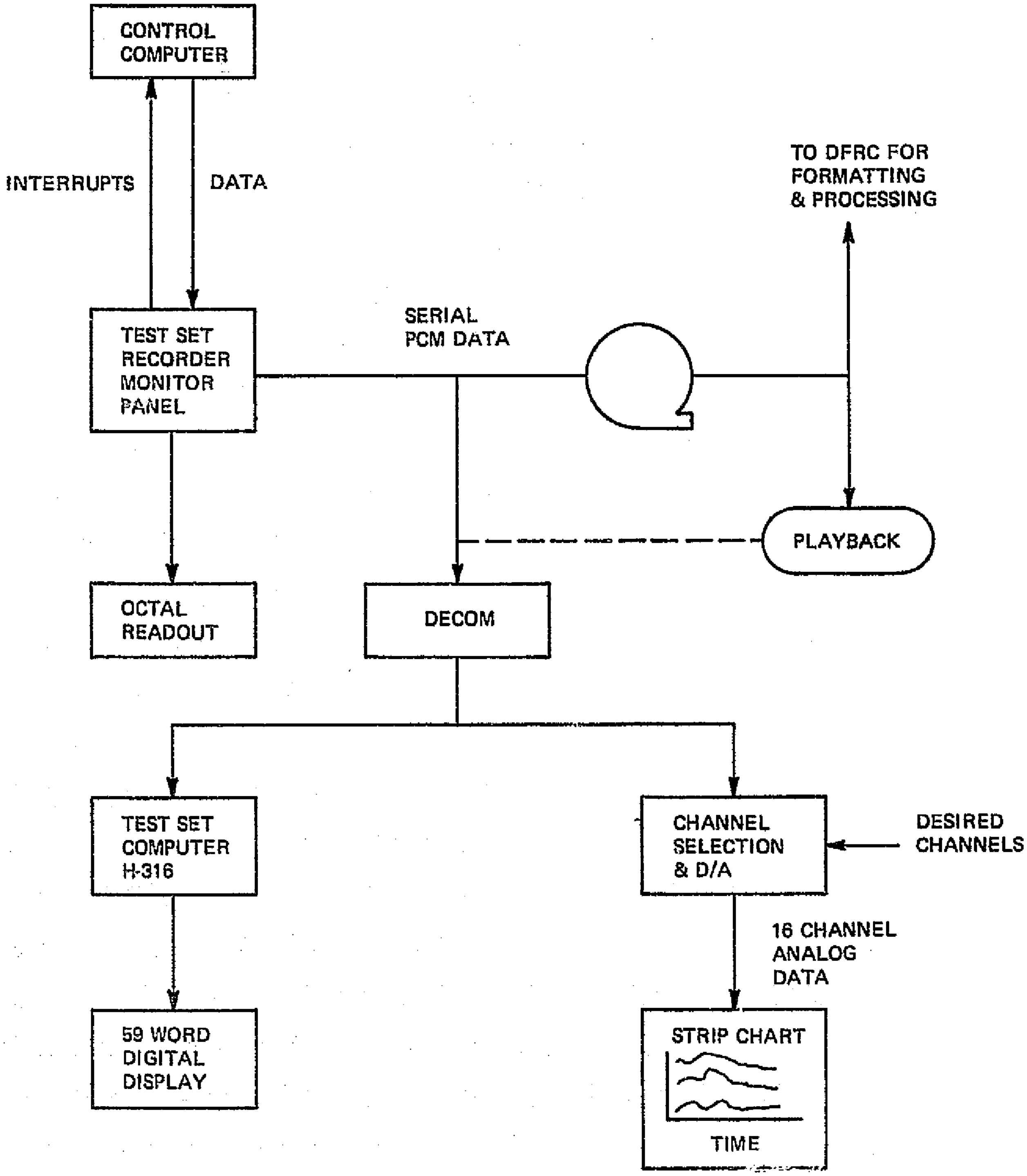

Figure 2.7-2. Ground Test Data Flow

leading to changes in control laws or major changes in the testing can be performed at DFRC. In those cases where it is necessary data could be sent to DFRC and processed within two days of a test event.

The same computer programs will be used for processing the data from the ground tests as are intended for the flight test data. This reduces the programming cost associated with data processing and provides early checkout of the flight data processing programs.

2.8 GROUND SUPPORT EQUIPMENT

Ground Support Equipment (GSE) includes all non airplane installed hardware and software required to support development, testing, and operation of the PROFIT. GSE is separated into four categories:

1. Real Time Simulation
2. Data Acquisition, Display and Processing
3. Trouble Shooting Equipment
4. DCU Communications Equipment

The following paragraphs discuss the operation and arrangement of the complement of GSE depicted in Figure 2.8-1. The considerations in the selection of GSE are discussed in Section 4.5.

There are two sets of GSE hardware. One is installed in fixed racks around the F-15 "Iron Bird" (Figure 2.8-1) and the other is installed in a van or trailer to support engine testing at sites other than DFRC. At the completion of Altitude Test the simulation equipment is removed from the van and left at LERC, since it is duplicated at DFRC and required for ongoing LERC activities, and the van returns to DFRC, see Section 5., to support airplane ground engine runs and the MVC SLS engine stand runs through its data display capability.

2.8.1 Real Time Simulation

Section 4.5 details both real time simulation (RTS) requirements and the rationale behind the selected approach. Summarily the RTS must permit verification of flight software without requiring flight software modifications to accommodate the RTS and it must be inexpensive both in terms of purchased hardware and development requirements. The system depicted in Figure 4.5-3 meets these requirements.

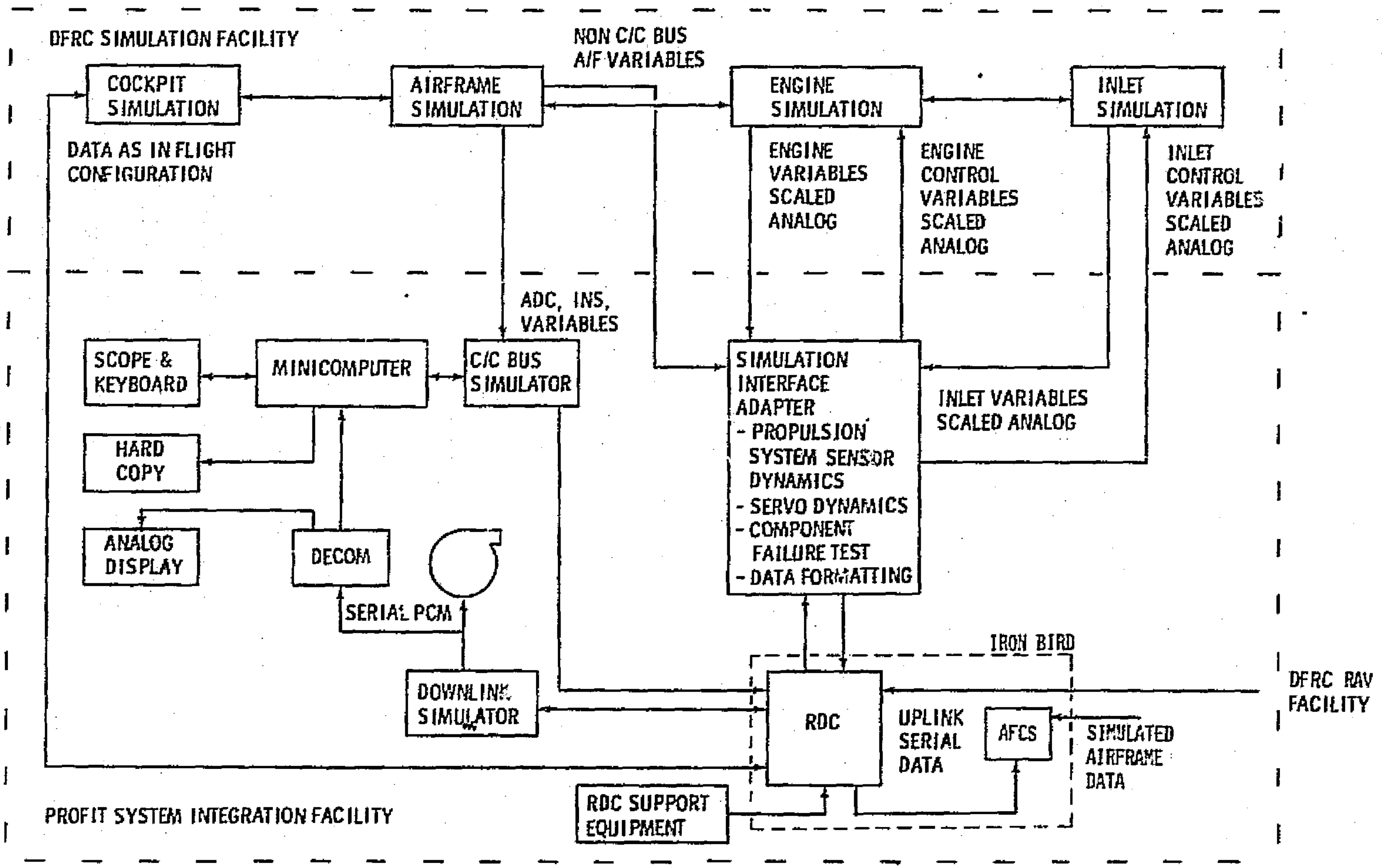

Figure 2.8-1. System Installation with DFRC Iron Bird

The heart of the system is an EAI 2000 parallel processor (or equivalent). This is used to simulate the plant dynamics of the inlet and engine. Component maps for the engine and inlet are stored in the H316 computer and sampled at a 5 msec rate. The engine portion of this simulation is operational on a similar pair of computers at LERC supporting the MVC programs. The inlet portion of the simulation will be derived from a McAIR F15 inlet simulation and merged with the engine simulation. Servo actuator and sensor dynamics and formatting are incorporated in the Simulation Interface Adapter (SIA), derived to some degree from the SIA built for IPCS. Since no testing of airframe integrated control modes at engine test sites is anticipated no capability for airframe dynamics is built into the portable portion of the GSE. Provision is however made for the H316 to format dummy data for transmission to the airplane interfaces (Central Computer and Uplink) to ensure proper exercising of DPCU hardware and software during cell tests.

Two DPCU's are available at all cell tests. One is used to control the engine under the test. The other serves as a spare and is coupled to the GSE to provide real time simulation capability in parallel with engine testing. A cockpit simulation and PLA resolver are provided to permit full testing of pilot interfaces both on the simulation and in live engine tests.

The fixed simulator at DFRC provides further capabilities. A complete "Iron Bird," a retired aircraft, is provided and interfaced with the DFRC digital simulator. One set of PROFIT flight hardware is installed on the airplane in flight configuration and used to test either left hand or right hand side software. DPCU CAS outputs are run through an interface box to provide identical inputs to CAS. The interface box also provides an access point to verify CAS response to simulated system failures. Since this simulator will be used to test integrated control modes, provision is made for both the central computer bus and uplink data to be generated by the DFRC Digital Simulator. A plug in inlet and airframe simulator and changeover

capabilities are provided so that the full Real Time Simulation may be operated as an entirely electronic simulation or with the hydraulically powered "Iron Bird" to meet prevailing test requirements.

2.8.2 Data Acquisition, Display and Processing

Data from both the RTS and actual engine running is obtained from the 60 word 20 SPS PCM downlink bit stream. As indicated in Section 2.7 these data are eventually processed through an extensive analysis program. However the equipment shown in Figure 4.5-2 provides for real time data display and immediate playback of test events, in addition to recording data for later processing.

Although real time display is limited to 16 of 60 channels, switching is provided to rapidly rearrange the data menu as required by test events. In addition to the 16 continuous channels discrete words are separately displayed. The demuxed data are also passed to the H-316 which provides engineering unit display and hard copy of processed data.

2.8.3 Trouble Shooting Equipment (TSE)

TSE consists of an assortment of standard test gear and a basic tool bit. Two items are significant additions relative to IPCS. One is an oscilloscope. During IPCS field tests it was difficult to obtain adequate oscilloscopes, hence it is included. The second is a set of breakout boxes for all IFU cables to permit direct monitoring as required of all signal lines. Although seldom required they are inexpensive to build and indispensable when needed.

2.8.4 DCU Communications Equipment

This equipment, all residual IPCS hardware (Computer Control Unit, Teletype and Paper Tape Reader), is used to load object tapes and patch tapes into the 601 DCU and interrogate the 601 core. Because the CCU cables are only

6 feet long this equipment must frequently be placed close to the flight hardware and then removed. Thus it will be placed on a mobile cart to permit moving it about as required.

2.9 SYSTEM B DESCRIPTION

System A described above achieves all PROFIT objectives. It has, however, two disadvantages - the initial capital investment is substantial and research payoffs don't start for roughly three years, see Section 5. System B described below was conceived to remove these two disadvantages. As such it is a three phase program, see Section 5.2. In the development phase a system, Figure 2.9-1, suitable for energy management studies (terrain following and intercepts) is developed using minimumally modified existing hardware. This configuration is used for the trajectory management phase. In the propulsion control phase the initial system is expanded to incorporate engine and inlet control functions. The following paragraphs discuss the two systems sequentially treating the propulsion control system as an increment to the initial system.

2.9.1 Software

The basic modular software concept, Figure 2.9-2, is retained from System A studies. Rather than implementing all identifiable host program functions initially, as had been planned, structured programming techniques will be applied and stubs provided for all identifiable requirements. Only development phase requirements will be implemented beyond stubs during the development phase. In this phase the test module will exercise the central computer, flight control system, and uplink interfaces. In order to avoid saturating the mechanical trim system it will be turned off when the research digital control (RDC) is engaged.

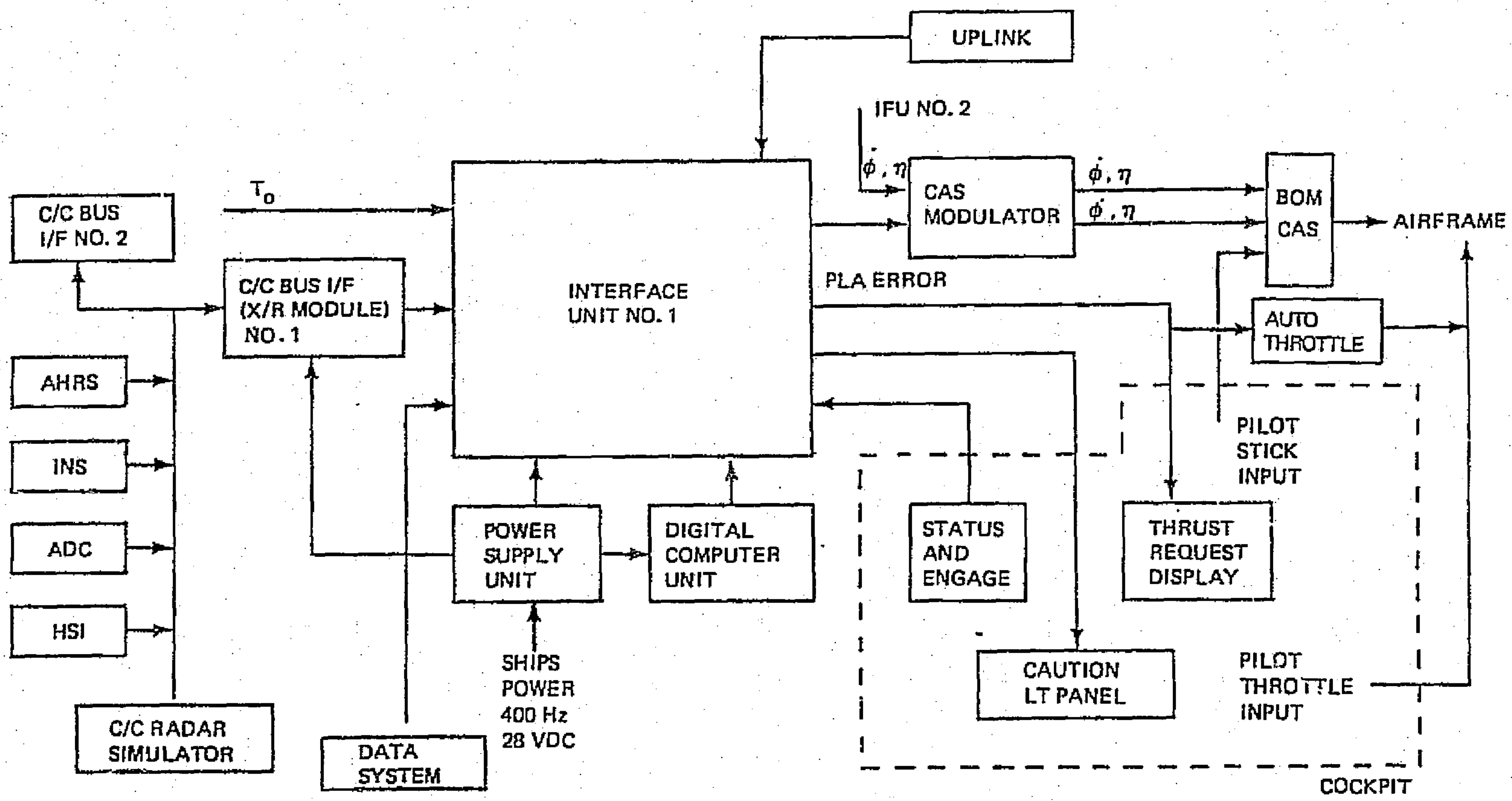

Figure 2.9-1. PROFIT Development Phase Configuration--System B

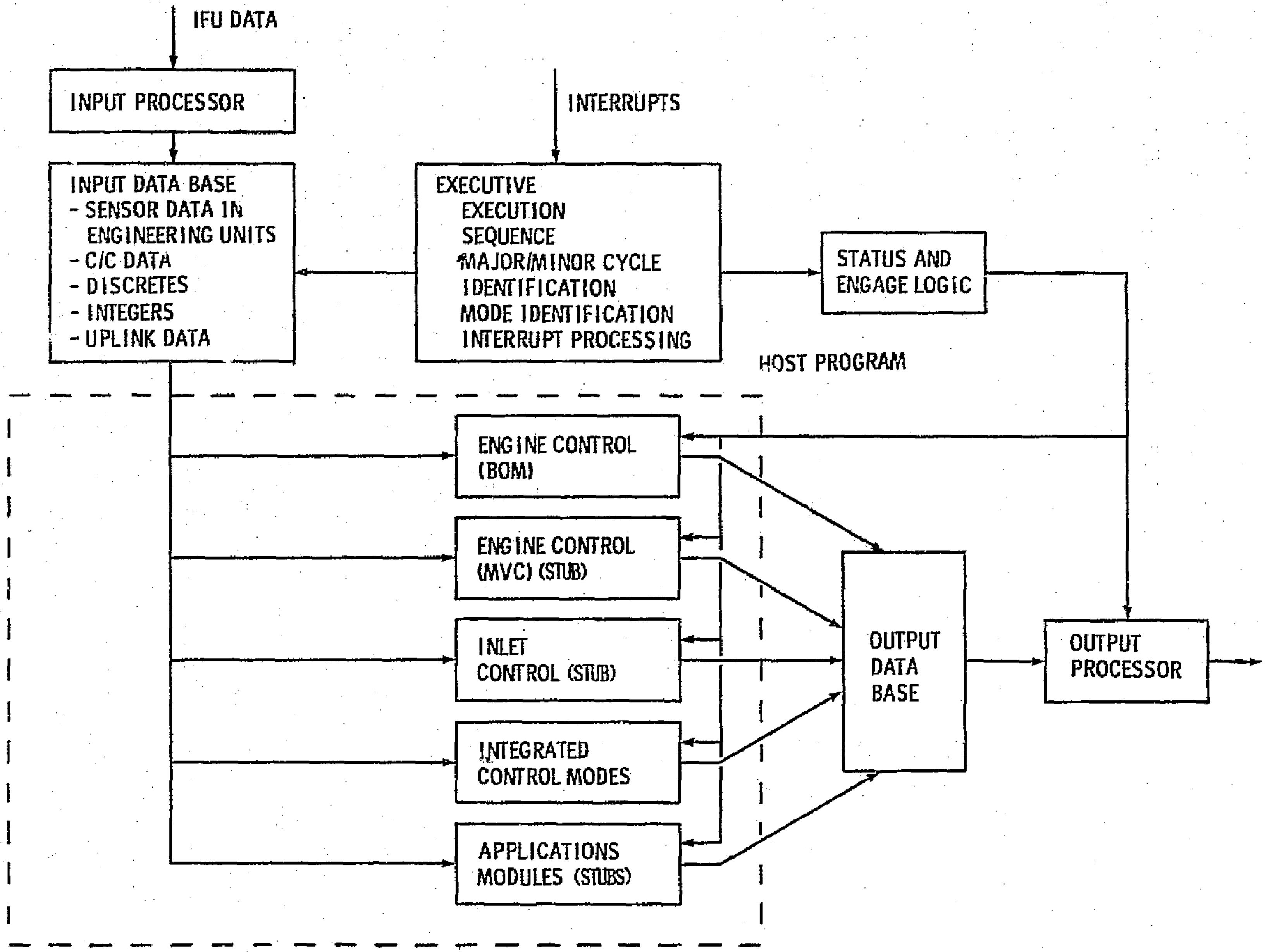

Figure 2.9-2. PROFIT Flight Software Concept--System B

2.9.2 Data Display and Reduction System

Using existing IFU hardware and software the RDC is compatible with the CT-77 PCM system. For ground or verification tests available GSE can be used to easily implement real time data display in the hangar, see figures 2.9-1, 3.

2.9.3 RDC Input Data (Development Phase)

During the development phase the RDC receives data from four sources - The BOM To Sensor, the Central Computer Bus, the Uplink, and the autothrottle - discussed below.

2.9.3.1 To Sensor

The To Sensor is a platinum resistive element device. Its characteristics are shown in Figure 2.5-10. The IFU will provide 5.ma constant current excitation to the device and measure voltage across it. The PROFIT system will use a spare element in the BOM probe. Heater control will remain with the BOM A/C systems.

2.9.3.2 Central Computer Bus

Thirty five data words (Table 2.9-1) are currently available on the Central Computer bus. All of these will be input to the RDC through the C/C bus I/F described below, Section 4.4.

2.9.3.3 Uplink

Specific variables for the uplink have not been defined. It is likely that it will be used primarily for gain changes and trajectory data. It is anticipated that a 24 word block containing a synch word, checksum, and 22 data words will be used. Design of the uplink system is documented in section 4.2.

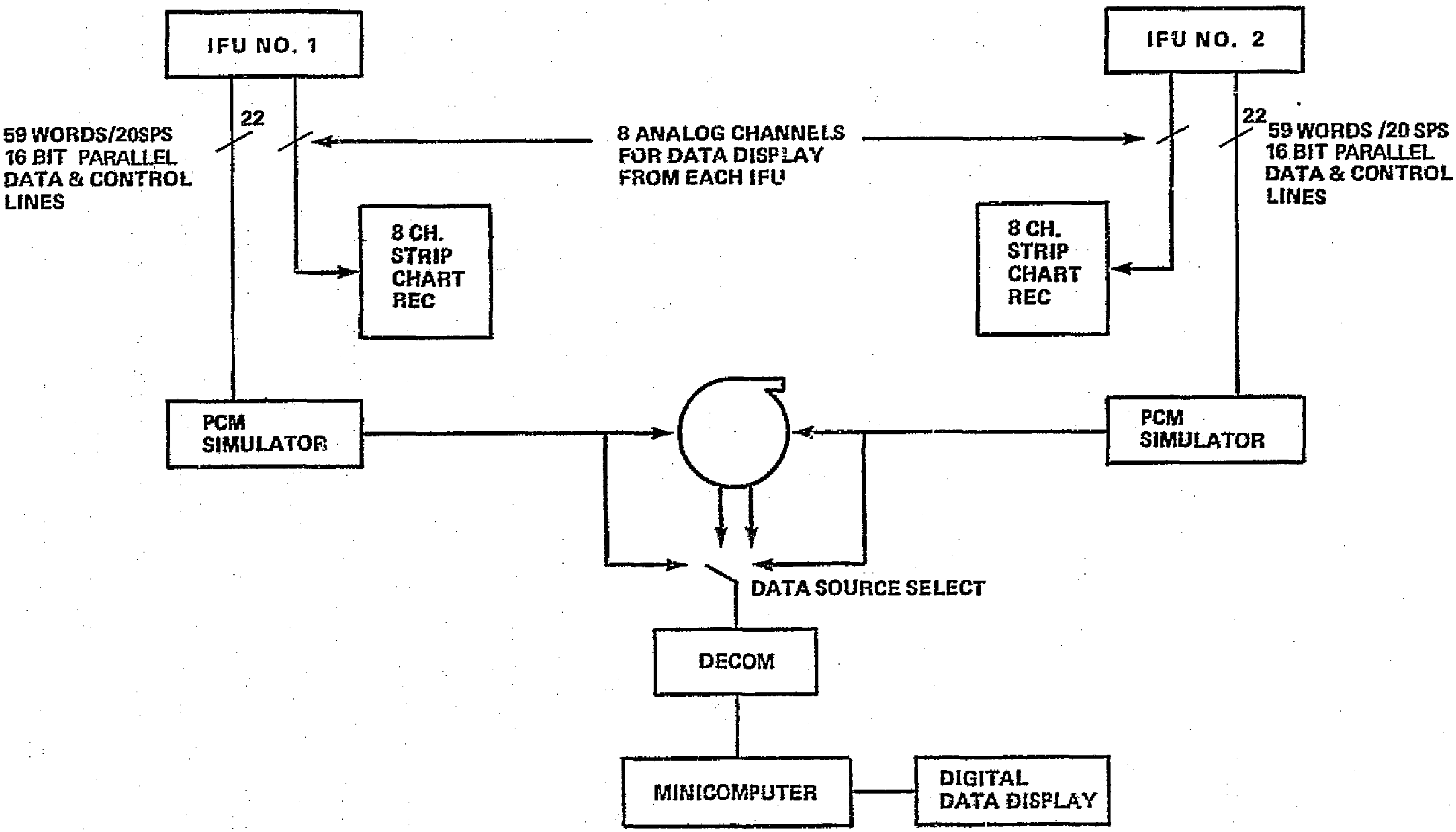

Figure 2.9-3. Ground Test Data Display

TABLE 2.9-1

CENTRAL COMPUTER BUS DATA

WORD	SIGNAL NAME	DESCRIPTION	UNITS	SCALE FACTOR
		AIR DATA COMPUTER SELECT WORD = $103A_{16}$	N/A	N/A
1	IASPDT	TRUE AIRSPEED	KNOTS	+11
	ITASPV	TRUE AIRSPEED VALIDITY (BIT 16)	0 → VALID DATA	
2	IAATKT	TRUE ANGLE OF ATTACK	SEMI CIRC.	-02
	IAATKV	TRUE ANGLE OF ATTACK VALIDITY (BIT 16)	0 → VALID DATA	
3	IHHALT	PRESSURE ALTITUDE +UP: DATA ARE ACT. ALT -39,390 FT -1570 ACT. ALT → INVALID DATA	10. FEET	+10
4	IASPOI	INDICATED AIRSPEED	KNOTS	+10
	IIASPV	INDICATED AIRSPEED VALIDITY BIT 16 (0 → VALID)		
5	ILAOAD	LOCAL ANGLE OF ATTACK	SEMI CIRC.	-02
	ILAOAV	LOCAL AOA VALIDITY BIT 16		
6	IMACHN	MACH NUMBER	ND	+02
	IMCHNV	MACH NUMBER VALIDITY BIT 16 (0 → VALID)		
7	IPRRAT	PRESSURE RATIO	ND	+01
	IPRRTV	PRESSURE RATIO VALIDITY BIT 16 (0 → VALID)		
8	IAIRDN	RELATIVE AIR DENSITY	ND	+01
	IAIRDV	RELATIVE AIR DENSITY VALIDITY BIT 16 (0 → VALID)		
9	ISTAOD	OPTIMUM ANGLE OF ATTACK	SEMI CIRC.	-02
	ISTAOV	OPTIMUM AOA VALIDITY BIT 16 (0 → VALID)		
10	IBCALT	BAROMETRIC CORRECTED PRESS. ALT DATA ARE ACTUAL ALT - 39,390 FT	10. FEET	12

NOTE: BIT 16 IS LSB OF 16 BIT WORD. THIS IS A CHANGE TO McAIR NOMENCLATURE WHERE LSB = BIT 15.

TABLE 2.9-1

CENTRAL COMPUTER BUS DATA (CONT.)

WORD	SIGNAL NAME	DESCRIPTION	UNITS	SCALE FACTOR
		AHRS SELECT WORD = 2053_{16}		
11	IPTCHA	PITCH ANGLE (AHRS) + NOSE UP	SEMI CIRCLE	+00
12	IROLLA	ROLL ANGLE (AHRS) + LEFT WING UP	SEMI CIRCLE	+00
13	IMAGHD	MAGNETIC HEADING (AHRS) + EAST, MAG. NORTH = 0.	SEMI CIRCLE	+00
		HSI SELECT WORD = 4057_{16}		
14	IHSICS	COURSE SET	SEMI CIRCLE	+00
15	IHSIMS	HEADING SET	SEMI CIRCLE	+00
16	IHSTCN	TACAN DISTANCE	N.MI	TBD
17	IBRTCN	TACAN BEARING	SEMI CIRCLE	+00
18	IMSIXI	BIT 1 BEARING REL. ALARM		
		BIT 2 DISTANCE REL. ALARM		
		BIT 3 LOCALIZER REL. ALARM		
		BIT 4 GLIDESLOPE REL. ALARM		
		BIT 5 MIDDLE/OUTER MARKER		
19	ILSLVD	LOCALIZER DEVIATION	ND	+00
20	ILSGSD	GLIDESLOPE DEVIATION	ND	+00

TABLE 2.9-1

CENTRAL COMPUTER BUS DATA (CONT.)

WORD	SIGNAL NAME	DESCRIPTION	UNITS	SCALE FACTOR
		INS SELECT WORD = 5056_{16}	N/A	N/A
21	IINSVL	INS VALIDITY (BIT 1)	1 → INS VALID	
	IATTVI	INS ATTITUDE VALIDITY (BIT 2)	1 → ATTITUDE VALID	
22	IBIALT	INERTIAL ALTITUDE DATA ARE ACT. ALT. -32768 FT.	FEET	16
23	IPPLAT	PRESENT POSITION LATITUDE (WORD 1)	SEMI CIRCLE	00
24	IPPLAT	2 LSB'S IN BIT 1, 2 (WORD 2)		
25	IPPLON	PRESENT POSITION LONGITUDE (WORD 1)	SEMI CIRCLE	00
26	IPPLON	2 LSB'S IN BIT 1, 2 (WORD 2)		
27	IPTCHI	PITCH + UP (BITS 15 & 16 ARE RANDOM GARBAGE)	SEMI CIRCLE	+00
28	IROLLI	ROLL + LEFT W. UP (B 15, 16 GARBAGE)	SEMI CIRCLE	+00
29	ITUHDI	TRUE HEADING + EAST, TRUE NORTH = 0. (B 15, 16 GARBAGE)	SEMI CIRCLE	+00
30	IVELNS	NORTH - SOUTH VELOCITY + NORTH	FPS	+12
31	IVELEW	EAST - WEST VELOCITY + EAST	FPS	+12
32	IVELVT	VERTICAL VELOCITY + UP	FPS	+11
		INS SELECT WORD = 5053_{16}		
33	IACCNS	NORTH - SOUTH ACCELERATION + NORTH	FPS^2	+08
34	IACCEW	EAST - WEST ACCELERATION + EAST	FPS^2	+08
35	IACCVE	VERTICAL ACCELERATION + UP	FPS^2	+09

2.9.4 Output Data (Development Phase)

Control data are output to the CAS (normal acceleration, roll rate) and to the cockpit thrust request display and/or autothrottle (PLA error). Analysis data are output to the PCM system (59 16 bit words at 20 SPS from each RDC) and to strip chart recorders (8 analog channels/12 bit resolution). Analysis data base is not yet formally defined but will include all input data, the control outputs and selected intermediate control variables. Variable data menus will be provided for both PCM and analog output data.

2.9.5 Control Data (Development Phase)

The table below summarizes features of the control data.

SIGNAL	NOMENCLATURE	FORMAT	SIGN	RANGE	SF
$\dot{\phi}_c$	ROLL RATE CMD	400 hz	IN PHASE WITH REF. IS +	0-4.81 VAC	(2 LINE SEGMENT)
nz_c	NORMAL ACCEL CMD	400 hz	IN PHASE WITH REF IS +	0-5.5 VAC	
PLAERR	PLA ERROR (THRUST REQUEST DISPLAY)	D.C.	+ VOLTAGE IMPLIES CMD>ACTUAL	±10V	(LINEAR)
	(AUTOTHROTTLE)	400 hz	IN PHASE WITH REF. IS + TORQUE	0-16.5 VAC	(LINEAR)

The CAS and autothrottle interface designs are documented in section 4.13 and 4.15 respectively.

2.10 SYSTEM B (PROPULSION CONTROL PHASE)

In the propulsion control phase the system is expanded, Figure 2.10-1, through the incorporation of a MIL-1553 bus port and perhaps by utilizing existing IFU/DCU processing capability to encompass the inlet control in a manner similar to the arrangement described in System A. The key feature of this arrangement is the flexibility and growth potential afforded by the MIL-1553 bus as depicted in figure 2.10-2.

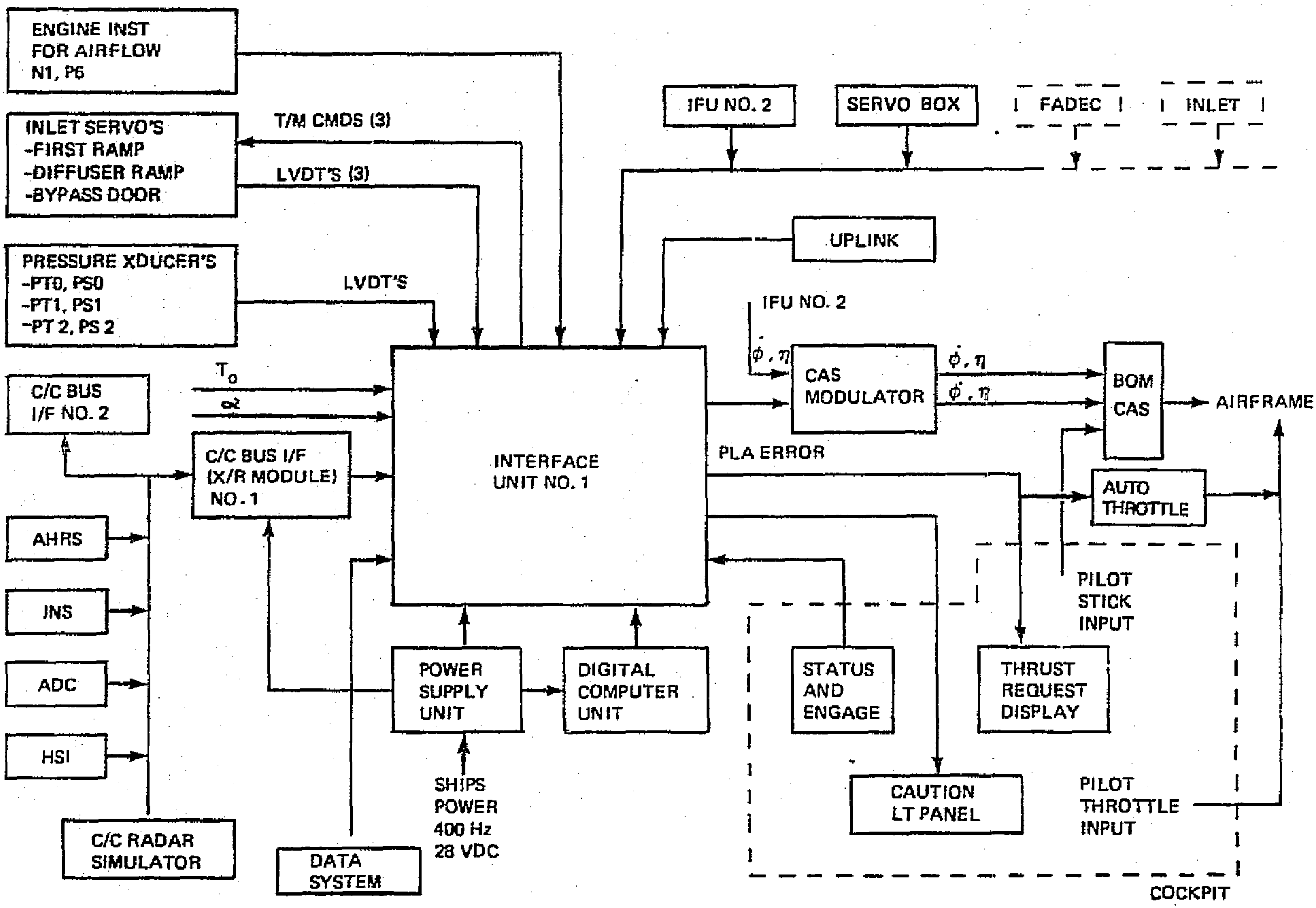

Figure 2.10-1. PROFIT Propulsion Control Phase Configuration–System B

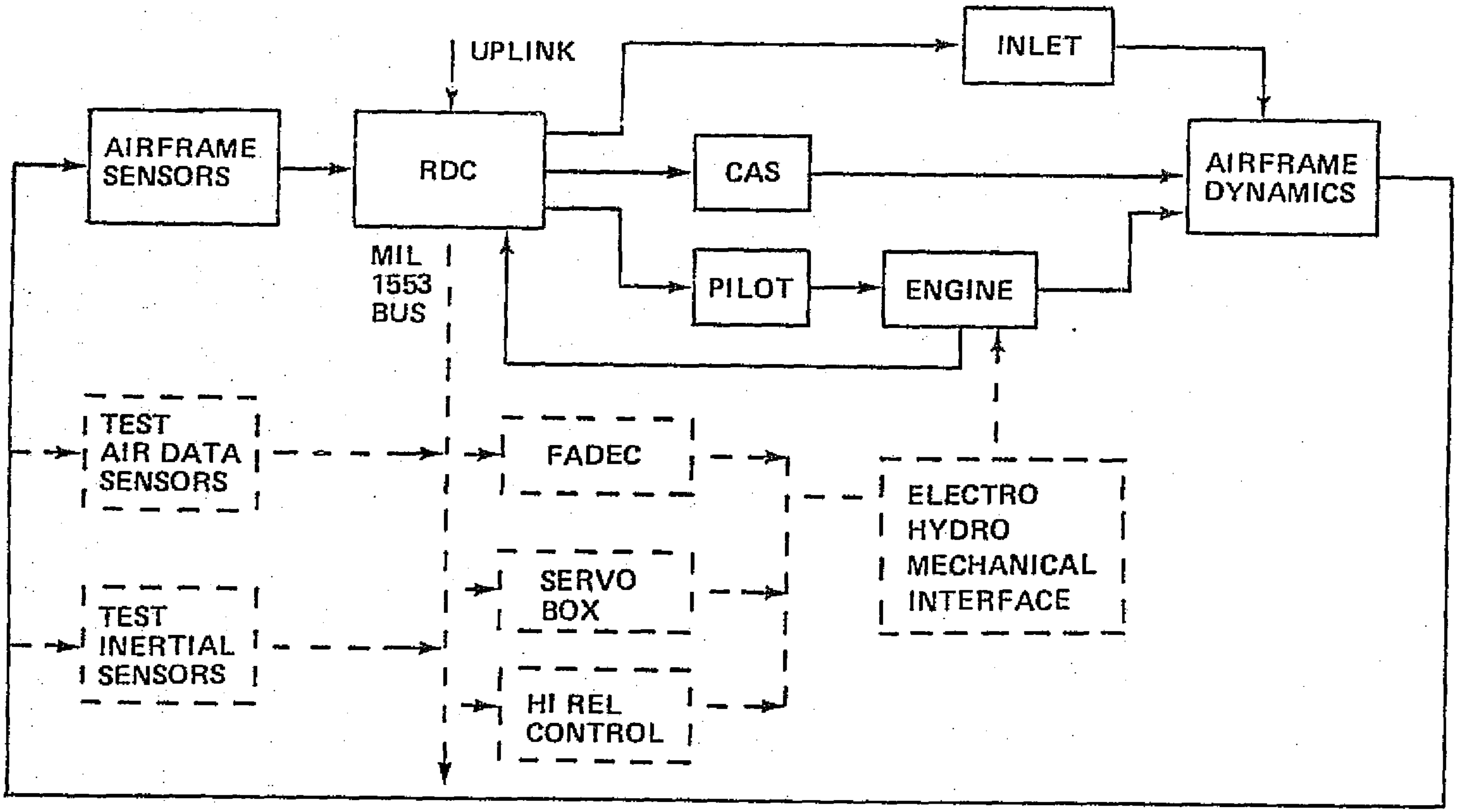

Figure 2.10-2. PROFIT System Growth Potential

3.0 CONTROL ALGORITHM ANALYSIS/RESULTS

The major activity in this area has been a study of the sample rate requirements. The overall objective of the study is to determine the computation interval necessary for satisfactory control performance.

It is divided into two phases. In the initial study, dynamic simulation CCD 1103-2.0 was used as the basis of a detailed examination of the effect of increasing calculation intervals to 60 milliseconds. This study is described in sections 3.1, 3.2, and 3.3. Later when the CCD 1103-3.0 program became available, this simulation was modified to use the PROFIT control and the anticipated PROFIT sensor and actuator dynamics. A study was conducted (section 3.4) using this simulation to verify the results obtained with the 1103-2.0 program. While differences in the programs resulted in significant changes in engine acceleration time, the comparison between the BOM and PROFIT control performance was similar. The memory and calculation time results presented in section 3.3 are not affected by the choice of engine simulation.

3.1 BILL-OF-MATERIALS CONTROL DEFINITION AND SIMULATION

The BOM control was defined as part of the software specification, reference 2. This control was included in the modified dynamic simulation used for the calculation rate study.

3.1.1 Control Definition

Technical Order 6J3-4-102-3, Engine Electronic Control, formed the basis for the definition of the EEC. The unified fuel control (UFC) definition was derived from the dynamic simulation and the data from references 3, 4, and 5. The UFC documented is the Lot VII control used on the F100 (3) engines. The BOM control specification was reviewed by $P\&WA_{TM}$ prior to its release.

3.1.2 Dynamic Simulation

The P&WA digital dynamic simulation of the F100(3) engine (CCD 1103-2.0) was used in the study described in section 3.2. The simulation was modified for the study in the following manner:

1) A new control package, programmed from the draft software specification, replaced the existing control routine for the transient calculations. The new control was designed with an executive and a series of control subroutines to facilitate variation in computation rate.

2) The logic of the initialization portion of the program was unmodified except for control logic necessary to match the initialization and transient portions of the program.

3) Schedules and constants from the specification were used in both the transient and initialization portions of the program.

The new control routine was programmed directly from the software specification with subroutines corresponding to the subparagraphs in the spec. The engine simulation calculations are exercised every 0.0025 seconds to provide calculation intervals that are multiples of the 0.005 second minor cycle for the HDC-601 computer. The executive subroutine controls both the order of execution and the rate of execution of the control subroutines.

Two different control calculation intervals are used in the study. The first is representative of the existing bill of materials system. The performance of the BOM calculation interval, referred to as BOM DT in section 3.2, is used as the standard of comparison for the PROFIT control. Figure 3.1-1 presents the timing diagram for the BOM DT. Sensor and actuator dynamics are unchanged from the basic CCD 1103-2.0 program. The hydromechanical UFC which operates continuously is computed at the same 2.5

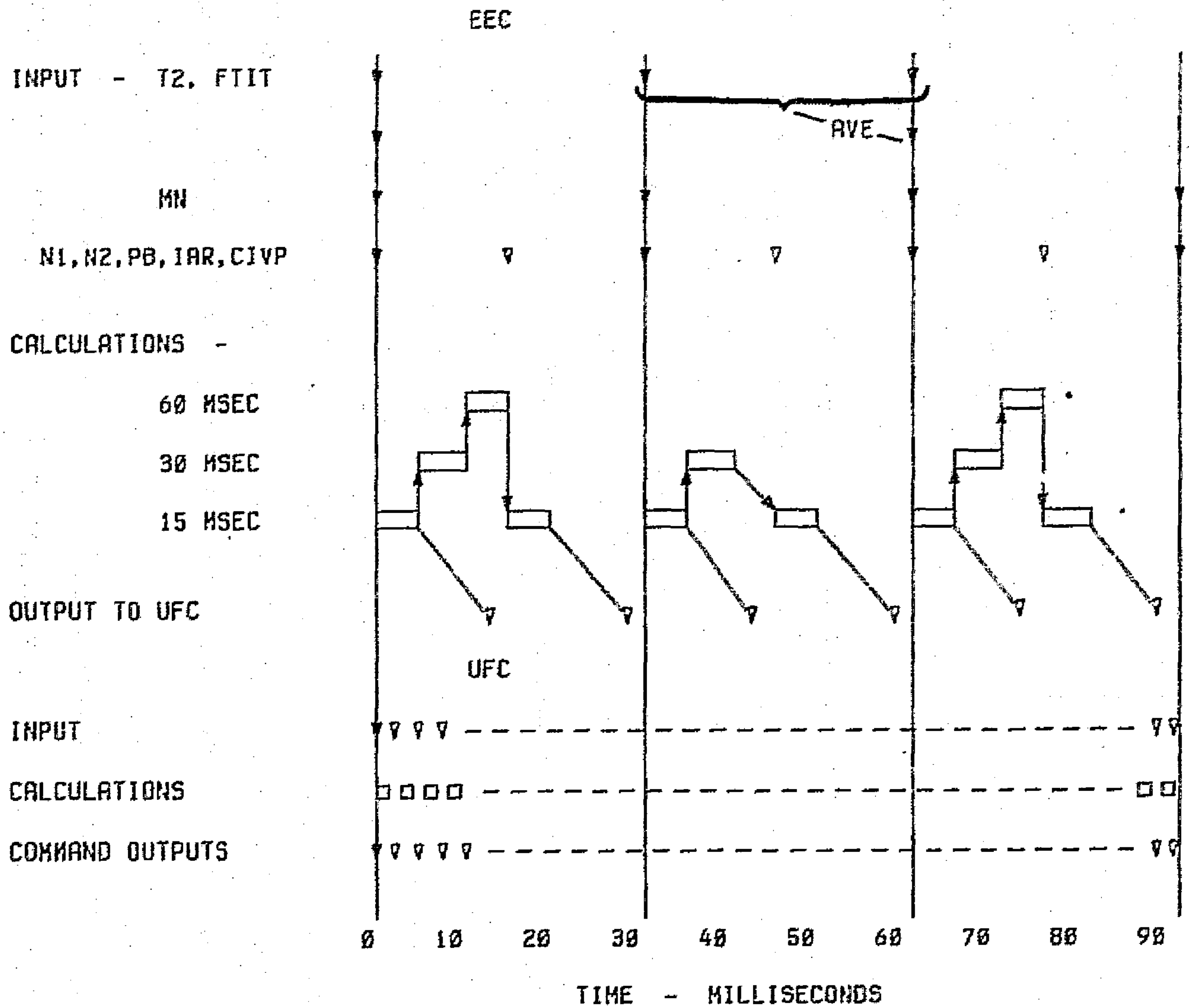

Figure 3.1-1. PROFIT Simulation Timing - BOM Interval

millisecond interval as the engine dynamics. Portions of the EEC are computed at 15, 30, and 60 millisecond intervals. Output to the engine is every 2.5 milliseconds.

The other calculation interval is for the PROFIT system. The intent was to perform all the control computations at the same rate. Exceptions to this are identified in section 3.2. Sample delay and averaging effects have been included in the sensors and actuators. Figure 3.1-2 shows the timing. As in IPCS the rotor speeds are sampled every 5 milliseconds. The frequency to digital conversion is represented by averaging two inputs 2.5 milliseconds apart. The samples input at the 5 millisecond rate are averaged over the control major cycle. The lags used in the BOM to represent speed sensor dynamics were removed for the PROFIT configuration. Low level analog inputs (T_2, T2.5, FTIT, and Pb) are sampled every 30 milliseconds and averaged over the previous control computation interval. Representative delay times are included in data input and command output to the engine actuator dynamics.

Both the BOM and PROFIT rates are included in the same simulation program with the control executive determining the sampling interval. The same engine and control computations are used for both.

3.2 COMPUTATION RATE STUDY

The study consisted of an evaluation of the PROFIT mode at a 60 millisecond control computation interval after preliminary studies indicated this was feasible.

3.2.1 Evaluation Procedure

Four flight conditions were selected (figure 3.2-1) to provide a range of engine operating conditions: 1) Sea level static, 2) Mach 1.2 at sea level for high burner pressure, 3) Mach 0.9 at 45,000 ft. for reduced

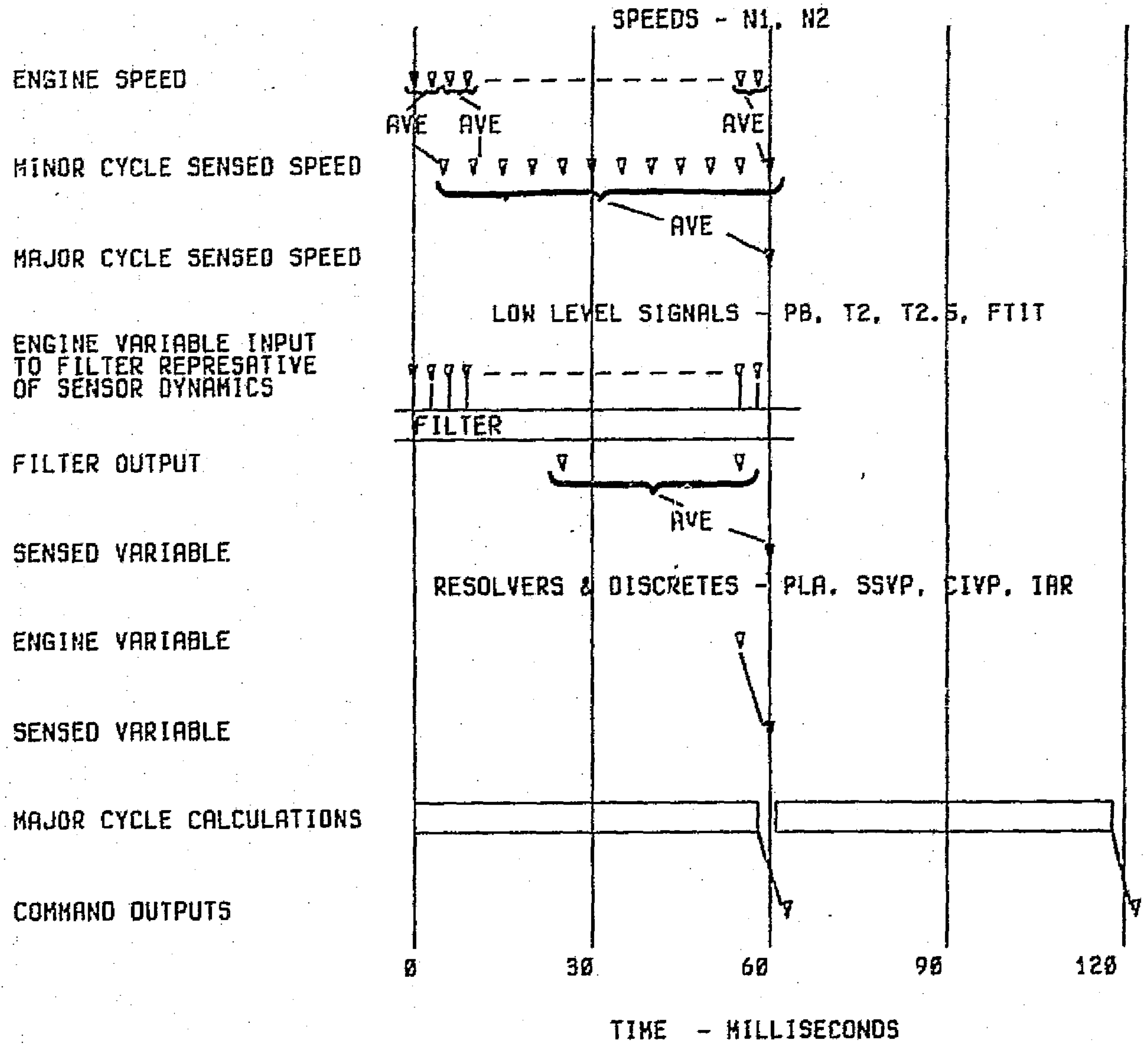

Figure 3.1-2. PROFIT Simulation Timing - 60 Msec Interval

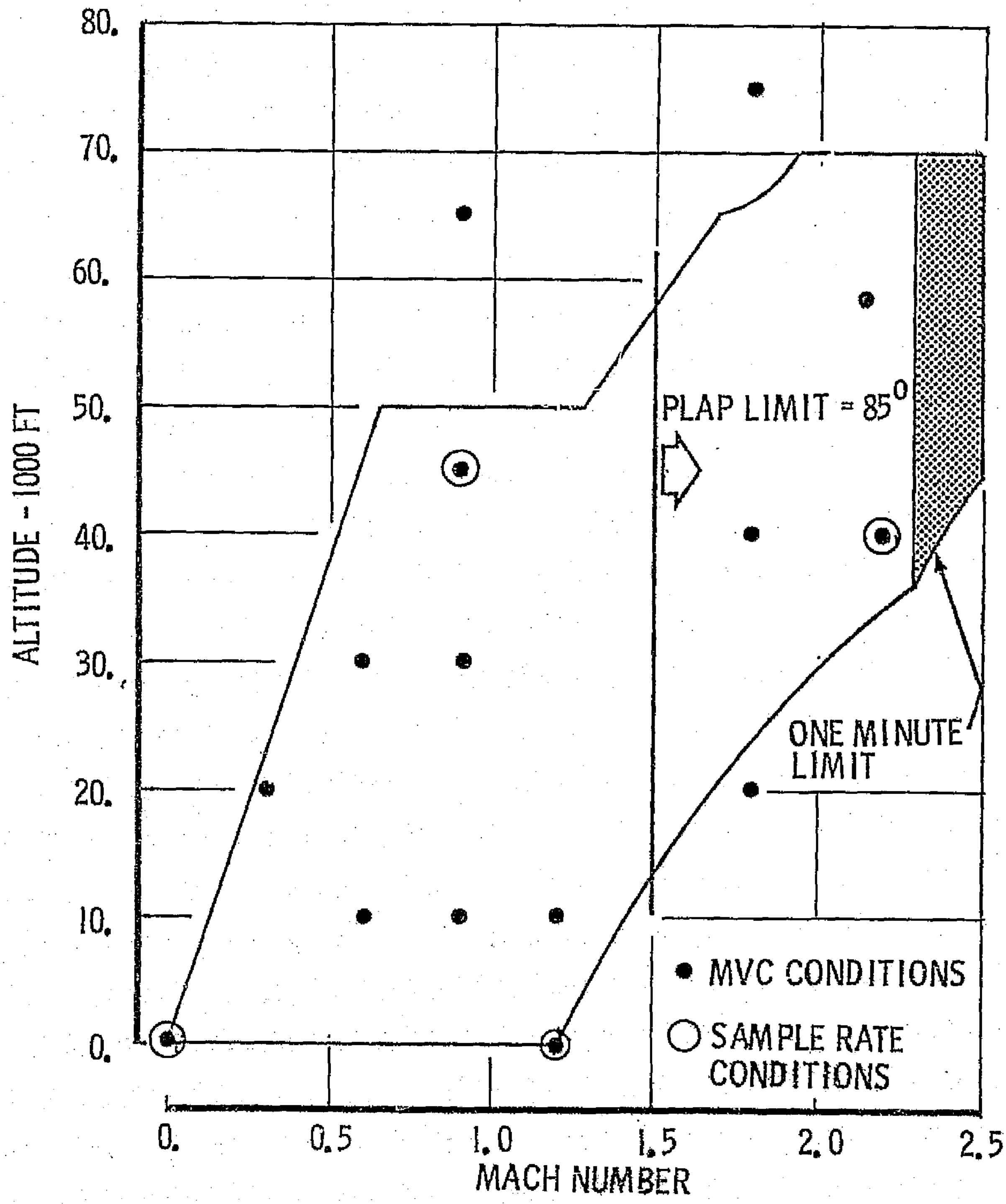

Figure 3.2-1. Flight Conditions Used for Sample Rate Study

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pressures, and 4) Mach 2.2 at 40,000 ft. for supersonic conditions. These conditions match points selected for work on the MVC, reference 6. Several throttle transients were run at each flight condition to compare different calculation rates. Table 3.2-1 identifies the throttle transients conducted.

Four parameters were used to evaluate control performance: transient time, thrust stability, and surge margin in the fan and high compressor. In addition the plots were examined to insure that speed, burner pressure, and compensated FTIT transients were not more severe than for the BOM rate. The definitions of the four evaluation parameters are as follows:

- Transient time
  Gas Generator - Time required to reach 90% and 98% of the change in net thrust.
  Afterburner
  Acceleration - time to maximum thrust.
  Deceleration Time to the A/B fuel shutoff as indicated by segment sequence value position.

- Stall Margin - Minimum value of stall margin occuring during the transient.

- Thrust stability - Does the thrust increase or decrease montinically during the transient.

Table 3.2-1 THROTTLE TRANSIENTS USED IN SAMPLE RATE STUDY

- SEA LEVEL STATIC
  Idle - Intermediate
  Intermediate - Idle
  Intermediate - Max
  Max - Intermediate
  65^{o} - 60^{o} PLA
  Bodie

- MACH 1.2, SEA LEVEL
  Idle - Intermediate
  Intermediate - Idle
  Intermediate - Max
  Max - Intermediate
  65^{o} - 60^{o} PLA
  Bodie

- MACH 0.9, 45000 FT
  Idle - Intermediate
  Intermediate - Idle
  Intermediate - Max
  Max - Intermediate

- MACH 2.2, 40000 FT
  Intermediate - Max
  Max - Intermediate

3.2.2 Results

This paragraph describes the results of the evaluation of the 60 millisecond computation interval and identifies those modifications required for this interval. Generally the 60 millisecond computation interval provided satisfactory performance. Appendix A contains plots of all the transients identified in Table 3.2-1 for both intervals. Table 3.2-2 presents a comparison of the evaluation parameters for the gas generator transients. With the exception of a small increase in acceleration time the performance is comparable. Figure 3.2-2 shows a SLS acceleration comparison that is typical of all flight conditions. In all cases except Mach 1.2, sea level the thrust transients were monotonic.

An oscillation is present at the Mach 1.2, sea level condition. The small oscillation in the intermediate to idle transient at the BOM interval is increased for long calculation times (Figure 3.2-3). This clearly must be corrected for satisfactory operation at the 60 millisecond interval. A similiar, but less severe, situation exists for the idle to intermediate transient at this flight condition resulting in a loss in high compressor surge margin.

TABLE 3.2-2
GAS GENERATOR TRANSIENT COMPARISON

Condition	Transient	DT	Transient Time 90% FN	Transient Time 98% FN	Minimum Surge Margin Fan	Minimum Surge Margin HPC
SLS IAR = 1	INT - IDLE	BOM	3.80	[1]	.079	.176
		.06	3.80	[1]	.080	.176
	IDLE - INT	BOM	2.68	3.99	.103	.098
		.06	3.12	4.55	.099	.115
SLS IAR = 0	INT - IDLE	BOM	2.51	[1]	.114	.176
		.06	2.60	[1]	.118	.176
	IDLE - INT	BOM	2.66	3.95	.097	.100
		.06	3.10	4.54	.100	.119
M = 1.2 Sea Level	INT - IDLE	BOM	.58	.64	.208	.124
		.06	.66	.70	.209	.067
	Minor Cycle Rcvv	.06	.65	.69	.204	.132
	IDLE - INT	BOM	1.49	1.85	.245	.102
		.06	1.61	1.75	.245	.089
M = 0.9 45,000 FT	INT - IDLE [2]	BOM	1.98	9.48	.193	.101
		.06	2.02	9.54	.193	.099
	IDLE - INT	BOM	1.63	2.13	.213	.029
		.06	1.87	2.46	.213	.034

[1] Not achieved in 6 second run.

[2] 11500 and 11000 N_2 used rather than 90% and 98% FN.

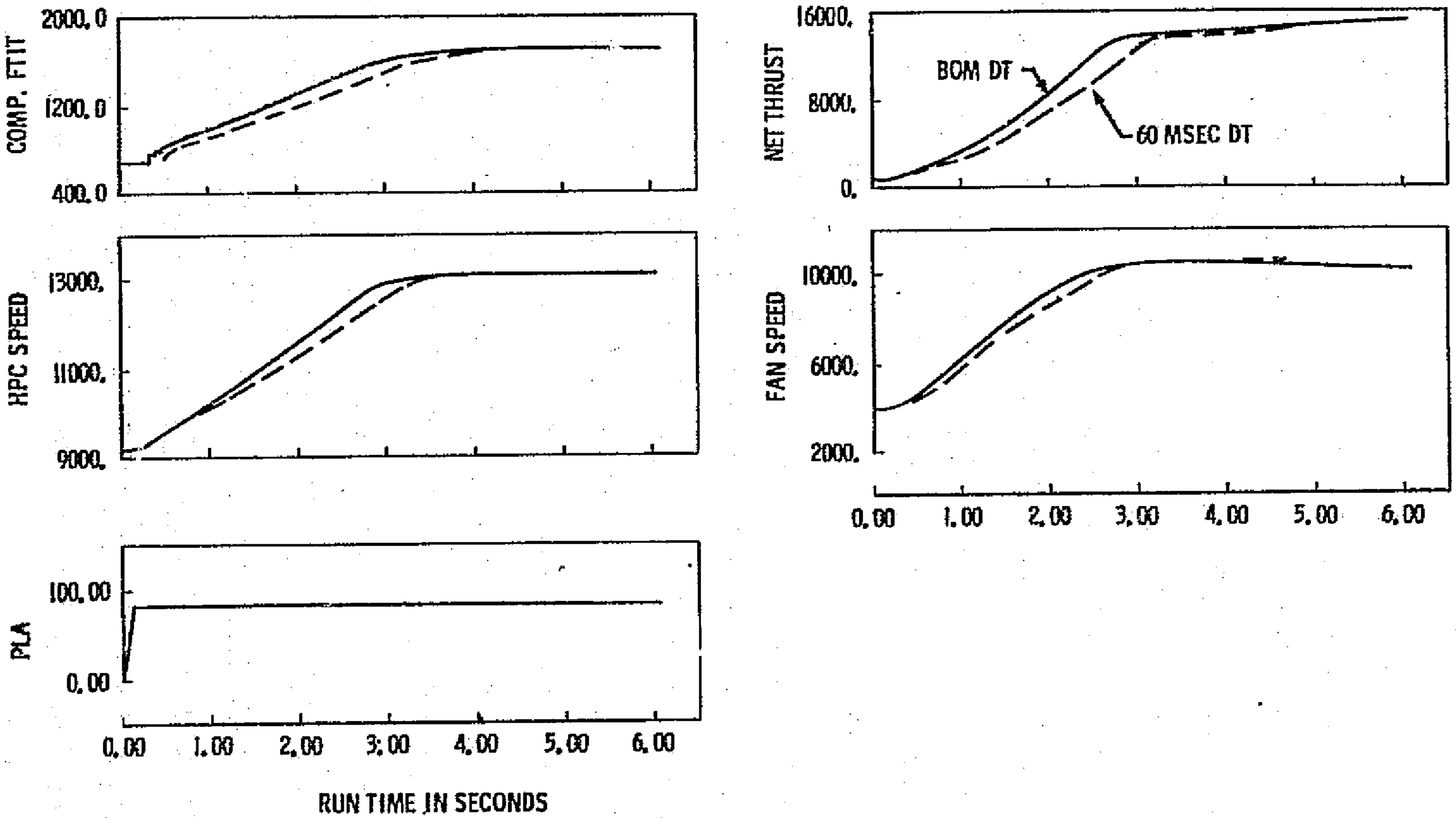

Figure 3.2-2. BOM Time Response Comparison

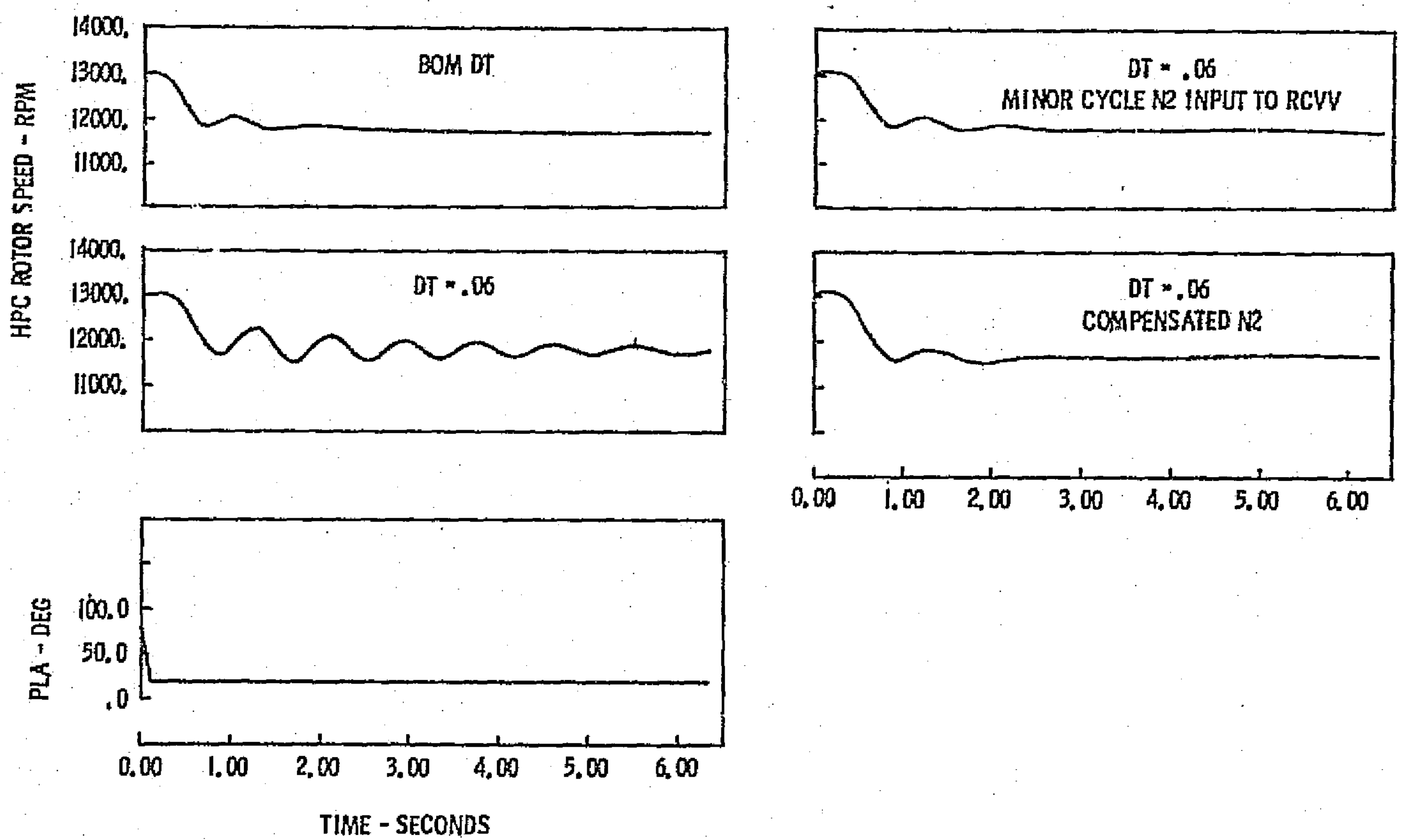

Figure 3.2-3. Mach 1.2, Sea Level Oscillations

These oscillations occur only for high Mach number, low altitude flight conditions. The results of two approaches to solving this problem are shown in figure 3.2-3. One is lead-lag compensation of the sensed N_2 input to the fuel flow command computation. The compensation results in a small overshoot during an acceleration. This tendency is much more pronounced at sea level static. Therefore, the compensation would have to be phased out as a function of flight condition. It appears more promising to compute a portion of the control at a higher rate.

As shown on the figure, computing the RCVV command every minor cycle (5 msec) provides an adequate solution. Figure 3.2-4 illustrates the computation. The schedule (figure 3.2-5) is a function of N_2 and $T_{2.5}$ which consists of two straight line segments at each temperature. The two slopes and the breakpoint are computed as a function of $T_{2.5}$ during the major cycle. These are used with N_2 to compute the command during the minor cycle.

Table 3.2-3 presents the transient time comparisons for afterburner operation. The Mach 0.9, 45,000 FT. acceleration is faster because PLAP limiting prevents segment 5 operation at this flight condition. Afterburner timing is controlled by the rate limited PLA (PLAP) and the time to fill the five segment manifolds. When the PLAP moves above a segment threshold, the corresponding manifold is filled using a high flow rate. PLAP is held at the minimum level for that segment until filling is complete as indicated by a fill switch in the fuel system.

In the PROFIT system the IFU will generate a priority interrupt when fill is completed. In response to the interrupt the executive records the value of the minor cycle counter, advances the segment sequence value (SSV) command to the operating position for the segment just filled, and outputs the SSV command. In the next major cycle, PLAP hold is released prior to the computation of PLAP for that cycle. The PLAP rate limit is adjusted to correspond to one major cycle plus the fraction of a cycle between the

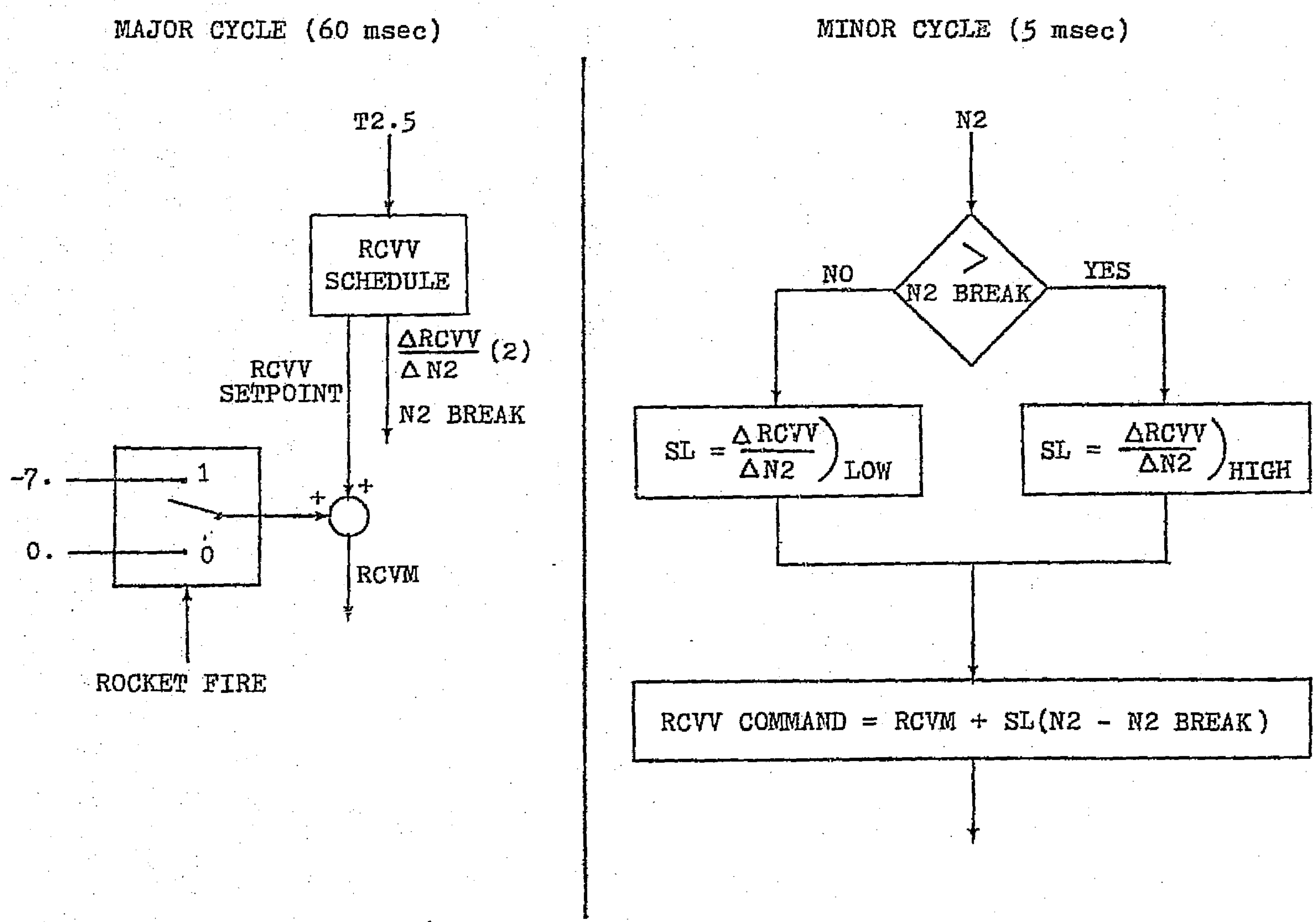

Figure 3.2-4. RCVV Command Computation with Minor Cycle N_2 Input

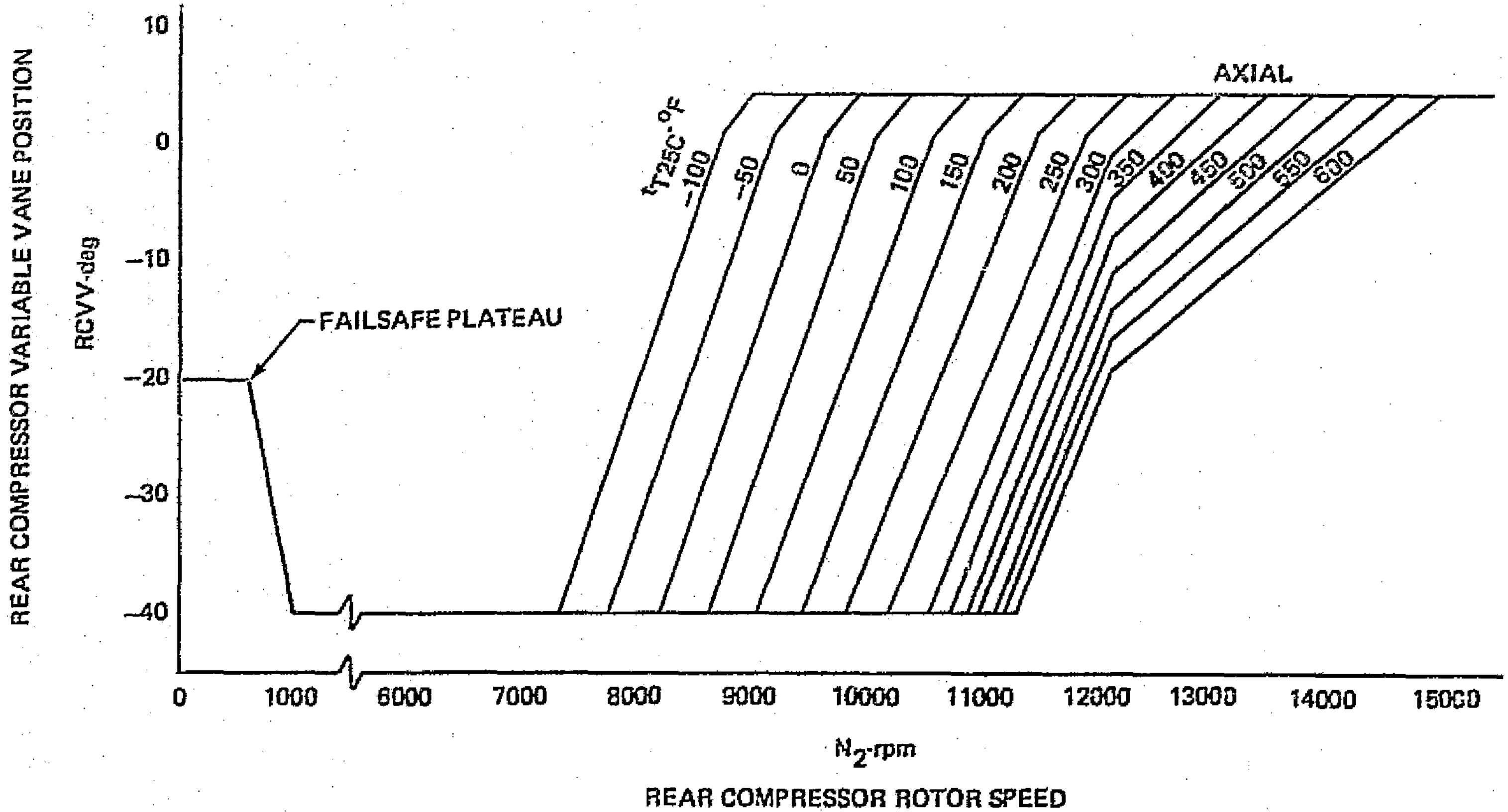

Figure 3.2-5. Rear Compressor Variable Vane Schedule

TABLE 3.2-3

AFTERBURNER TRANSIENT COMPARISON

Condition	Transient	DT	Transient Time	Minimum Surge Margin Fan	Minimum Surge Margin HPC
SLS	INT - MAX	BOM	3.84	.201	.176
		.06	4.08	.203	.176
	MAX - INT	BOM	.96	.228	.177
		.06	1.08	.228	.177
M = 1.2 Sea Level	INT - MAX	BOM	3.78	.275	.130
		.06	4.02	.275	.126
	MAX - INT	BOM	.96	.284	.127
		.06	1.08	.282	.122
M = 0.9 45,000 FT	INT - MAX	BOM	3.36	.134	.126
		.06	3.48	.134	.126
	MAX - INT	BOM	.72	.147	.124
		.06	.84	.147	.123
M = 2.2 40,000 FT	INT - MAX	BOM	3.78	.252	.097
		.06	4.02	.252	.096
	MAX - INT	BOM	.96	.249	.086
		.06	1.08	.247	.085

interrupt and the end of the major cycle. The ignition timer is computed in a similiar manner for segment 1. This prevents operation of the afterburner at the high fuel flow rate used to fill the manifold and reduces the acceleration time. The data presented in table 3.2-3 are for this configuration.

3.2.3 Conclusions

The following conclusions can be drawn from the results of the initial study:

1. The computation interval can be extended to 60 milliseconds

2. Satisfactory performance was achieved at SLS, Mach 0.9, 45,000 FT., and Mach 2.2, 40,000 FT. without any modifications to the control

3. The oscillations present in the BOM control at Mach 1.2, sea level are significantly worse with the 60 millisecond interval. Several possible fixes have been considered including: partial minor cycle calculation, compensation of the N_2 signal, and reduced droop slope.

3.3 SYSTEM MEMORY AND CYCLE TIME

Memory and cycle time requirements have been estimated for the PROFIT system software. The BOM control is sufficiently well defined to permit a line by line evaluation. The engine control definition is discussed in section 3.1. The inlet control is defined in references 7, 8, and 9. Tables 3.3-1, 3.3-2, and 3.3-3 list the estimates for the EEC, UFC, and inlet control.

TABLE 3.3-1

EEC MEMORY AND CYCLE TIME

FUNCTION	MEMORY	CYCLE TIME (μ SEC)
Speed input filters and normalization	43	174.4
T2 filter and table lookups	465	758.4
PB filter and derivative gain bias	20	86.4
VMAX	42	40.8
PLAP limiting	76	73.2
N2 high rate solenoid	85	124.8
Stall recovery	70	111.6
Minimum PLAP loop	610	1560.4
ΔPLA loop	542	1482.2
Nozzle area trim loop	629	1725.0
CIVV	61	197.6
Unvariate table lookup	38	--
TOTAL EEC	2681	6334.8

TABLE 3.3-2

UFC MEMORY AND CYCLE TIME

FUNCTION	MEMORY	CYCLE TIME (μ SEC)
Power lever angle logic	202	319.2
T2.5 compensation	28	70.8
Gas generator fuel cmd	431	765.8
RCVV - Major Cycle	122	138.0
Minor Cycle	31	576.0
Compressor bleed	58	183.6
Nozzle area	399	657.6
Segment sequence valve	151	210.0
Afterburner fuel flow cmd	532	805.6
Bivariate table lookup	115	--
TOTAL UFC	2069	3726.6

TABLE 3.3-3

INLET CONTROL MEMORY AND CYCLE TIME

FUNCTION	MEMORY	CYCLE TIME (μ SEC)
Freestream pressure ratio calibration and filter	104	472.6
Mach block and Mach No. to EEC	31	54.8
First ramp	326	644.4
Third ramp	230	724.0
Bypass	145	274.4
BIT	55	74.4
TOTAL INLET CONTROL	891	2244.6

The HDC-601 is a sectored machine. This requires indirect addressing of any location outside the current sector (512 words). For estimating it was assumed that any variable used outside a subroutine would have to be addressed indirectly. This provides a somewhat conservative estimate in that indirect addressing requires a location for the address and 1.2 μsec additional execution time (i.e., 3.6 rather than 2.4 for an ADD). Since the specification and simulation break the engine control into 33 subroutines for convenience in performing multirate sample studies, this represents some additional memory and cycle time. Further an indirect return was assumed at the end of each subroutine.

The intent was to generate worst case estimates. In cases where parallel logic paths existed the longest execution time was used. Table look ups were based on beginning at the middle of the table and going to the end to find the correct value. It is intended that mid location addresses will be loaded for all tables in the power up routine to insure that it is not necessary to travel further than half the table.

Two concepts were examined for table look up routines: one in which only the X and Y values are stored and one in which slopes are stored along with the X and Y values. Using stored slopes is faster, but it requires more memory. In the case of univariate tables there is substantial time saving for relatively little increase in memory. However, for bivariate tables the additional memory is large relative to the time saving. In the BOM control the fast univariate saves 884 microseconds with an increase of 548 locations and the fast bivariate saves only 242 microseconds with an increase of 885 locations. As a result the fast univariate was used in the estimates while the fast bivariate was not.

The estimates for the engine control were made line-by-line from the control routines in the dynamic simulation. Previously the EEC had been estimated line-by-line from the EEC assembly language listings in the T.O. The two approaches produced consistent results. The inlet control was estimated line-by-line from the assembly language listing contained in reference 9.

Other portions of the control system were estimated based on existing IPCS code and known requirements. Control input/output is based on the conservative approach of processing all the possible I/O channels. The development plans presented in Section 5.0 are structured around the use of a co-resident BOM control to be used as a reference for advanced engine controls. The difficulty of making direct comparison between flights on different days with different ambient temperature was demonstrated on the IPCS program. Engine to engine differences make right to left engine comparisons difficult. Thus co-residence offers the best approach to establishing a consistent reference engine control.

A research configuration of interest would include a full authority BOM control co-resident with the Multi-Variable Control currently under development by AFAPL/LeRC/P&WA/SCI. In addition it might include a debugging program and ground support software with automated checkout capability. Table 3.3-4 lists the memory requirements for this system. The estimates for the MVC program were obtained form data presented at the reference 10 meeting. Table 3.3-4 presents the cycle time estimates for this system executing the BOM and MVC control laws in a 60 millisecond major cycle. As indicated there is substantial available cycle time with either control.

Another possible research system consists of a single propulsion control operating in conjunction with an on board energy management system.

Table 3.3-5 presents memory estimates for an energy management scheme presented in reference 11. Reference 12 estimates the size of an energy management system for a transport aircraft as "less than 8K'. Without a firm definition of the specific requirements it is not possible to develop a definitive core estimate for the PROFIT program, but it is likely that these estimates span the range. Thus, it appears that the energy management software will not occupy significantly more memory than the engine control it replaces.

TABLE 3.3-4

ENGINE CONTROL

	MEMORY REQUIRED	CYCLE TIME	
		BOM ENG	MVC ENG
Sector 0 (Input Data, Etc)	512	--	--
Debugging Program	1024	--	--
Ground Support Software	2500	--	--
Control I/O	565	12.8	12.8
Executive	2000	4.0	4.0
DCU Self Test	798	2.1	2.1
Up/Down Link	194	4.4	4.4
Central Computer Interface	400	1.0	1.0
Inlet Control	891	2.2	2.2
BOM Engine Control	4750	10.0	--
MVC Engine Control	7135	--	15.0
TOTAL	20769	36.5	41.5
MARGIN	11999	23.5	18.5

TABLE 3.3-5

MEMORY REQUIREMENTS FOR

ENERGY MANAGEMENT MODULE

	MEMORY REQUIRED
Full/Time Tradeoff	800
Flight Director	700
Flight Control	370
In-Flight Calibration	500
Stored Paths	630
ENERGY MANAGEMENT TOTAL	3000

Memory and cycle time estimates for a system consisting of the BOM engine and inlet controls together with the energy management system identified in Table 3.3-5 are presented in Table 3.3-6. The cycle time estimates from reference 11 were adjusted to approximate the effect of differences in computer execution time.

It can be concluded that adequate memory and cycle time are available for the anticipated systems. In addition sufficient available memory and cycle time exist to provide flexibility to incorporate future programs.

3.4 RESULTS OBTAINED WITH CCD 1103-4.0

In late 1977 P&WA updated the simulation of the F100 (3) engine and bill of materials control. The new program, CCD 1103-3.0, became operational at NASA/DFRC in February 1978. The 1103-3.0 deck was modified to include the PROFIT control operating at a 60 millisecond computation interval with the same timing as shown in figure 3.1-2. The PROFIT version of the program was also modified to include PROFIT sensor and actuator dynamics, the inclusion of PROFIT sensor and actuator dynamics had been examined on the earlier program (1103-2.0) and it showed no significant impact on control performance. As a result, it was included in the 1103-3.0 deck without a separate study. A version of the 1103-3.0 program was developed to execute the PROFIT control logic at the BOM interval similiar to the BOM DT version of the 1103-2.0 deck. The BOM DT version of the 1103-3.0 program retains the BOM sensor and actuator dynamics from the 1103-3.0 deck. The PROFIT control logic is used to provide assurance that differences are due to sample interval and sensor and actuator dynamics rather than control differences.

Two changes between the 1103-2.0 and 1103-3.0 programs significantly reduced acceleration time. The time constant of the hydromechanical burner pressure sensor in the UFC was changed from 0.35 to 0.03, and the fuel system simulation was modified. The sensed burner pressure affects acceleration

TABLE 3.3-6

ENERGY MANAGEMENT

L/H SYSTEM

	MEMORY REQUIRED	CYCLE TIME
Sector 0 (Input Data, Etc.)	512	--
Debugging Program	1024	--
Ground Support Software	2500	--
Control I/O	565	12.8
Executive	2000	4.0
DCU Self Test	798	2.1
Up/Down Link	194	4.4
Central Computer Interface	400	1.0
Inlet Control	891	2.2
BOM Engine Control	4750	10.0
Energy Management Module	3000	10.0
TOTAL	16634	46.5
MARGIN	16134	13.5

time because the fuel flow command is computed as a Wf/Pb and multiplied by sensed Pb. In the 1103-2.0 program the fuel system was simulated by a series pair of first order lags (Tau_1 = .02, Tau_2 = .1). The original 1103-3.0 deck was updated to the 1103-4.0 configuration by PWA change memo dated 5-9-78. In this version the second lag (TAU_2 = .1) is represented by a second order lag with a damping ratio of 0.9 and a natural frequency of 5 Hz. At the same time the DEEC fuel system dynamics were reviewed corresponding dynamics were included in the PROFIT actuator simulation.

These changes affect PROFIT as well as the BOM control. PROFIT contains a simulation of the hydromechanical Pb sensor lag to produce comparable control performance. Both PROFIT and the bill of materials control use the same fuel pump, hence the fuel system dynamics are similar.

Although the simulation changes affect system dynamic response, the comparison between BOM and the 60 msec PROFIT is not significantly different from the earlier study. Table 3.4-1 presents a comparison of the evaluation parameters for a sea level static acceleration.

Although the PROFIT control is slightly slower (∿ 0.4 second) both controls are well within the limits defined in reference 4 -- 4 seconds to 90% and 15 seconds to 98%. Time histories at Mach 1.2, sea level are comparable to the 1103-2.0 study, figure 3.4-1. Reduced levels of oscillations at Mach 1.2 are apparent for both controls in comparing figures 3.4-1 and 3.2-3.

It has been concluded that the results of the 60 msec to BOM interval comparison performed with CCD 1103-2.0 are not significantly altered by use of the 1103-4.0 program or the PROFIT sensor and actuator simulations.

TABLE 3.4-1

TRANSIENT COMPARISON
SEA LEVEL STATIC -- IDLE TO INTERMEDIATE
IAR = 0

	BOM CONTROL	PROFIT CONTROL
Transient Time		
90% FN	1.85	2.22
98% FN	1.96	2.34
Minimum Surge Margin		
Fan	.114	.119
HPC	.045	.055

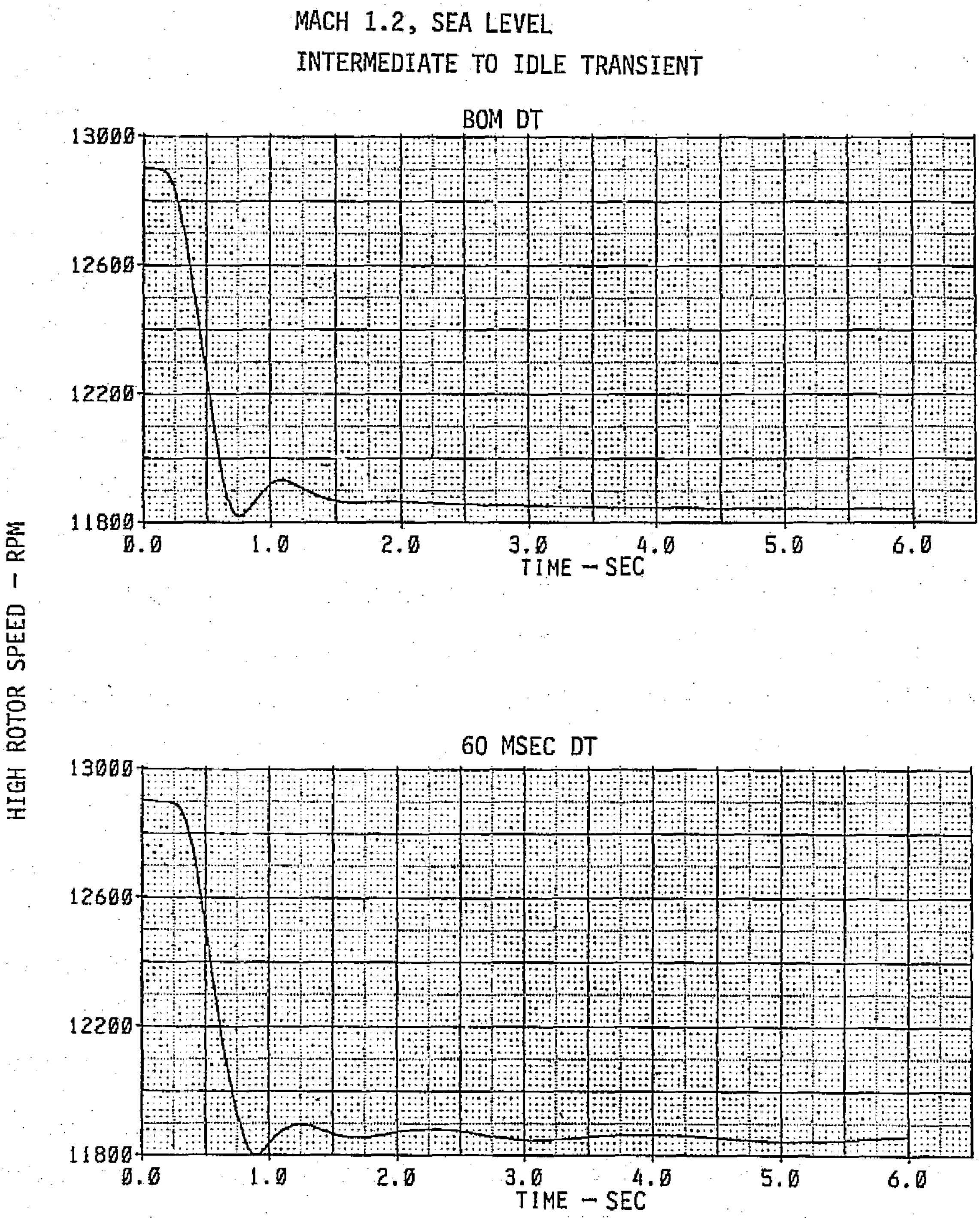

Figure 3.4-1. PROFIT CCD 1103-4.0 Deceleration Comparison

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3.5 FADEC TRADE STUDY

This study was undertaken to determine feasible and optimum alternatives for interfacing the NAVY/P&WA Full Authority Digital Electronic Control (FADEC) hardware with the PROFIT system. A large number of options were studied leading to the conclusion that there are many technically feasible alternatives. Financial constraints and organizational research objectives therefore became major factors in system configuration selection. Two configurations finally evolved, Figures 3.5-1, -2, which are acceptable on all counts. They are ranked in terms of cost benefit ratio. However, the system with the lower cost benefit ratio, Figure 3.5-2, also is lower in initial cost. Thus, final configuration selection may well depend on available funding. The following paragraphs discuss some aspects of the selection process.

3.5.1 FADEC Interfaces

FADEC is a research oriented self-contained engine mounted digital engine control, Figure 3.5-3. There are two such units with supporting hardware, one Navy owned; one Hamilton Standard owned. They will be available for research application in May 1979. Communication with these units is available through the two ports shown in Figure 3.5-3a. Both ports use similar UART chips and protocols but operate at different data rates. In the original application the high rate interface is used to pass sensor/processor information for failure mode identification and correction between the FADEC processor and a functionally identical off-engine processor. With reprogramming this interface could be used to operate FADEC either in its current mode or as a "servo box," as a controller to choose the position feedback paths on the seven engine servos. The low rate interface was originally intended for low bandpass health monitoring data but can be reprogrammed to operate FADEC in the servo box mode. The low frequency interface is not adequate to perform the data handling required for dual processor operation.

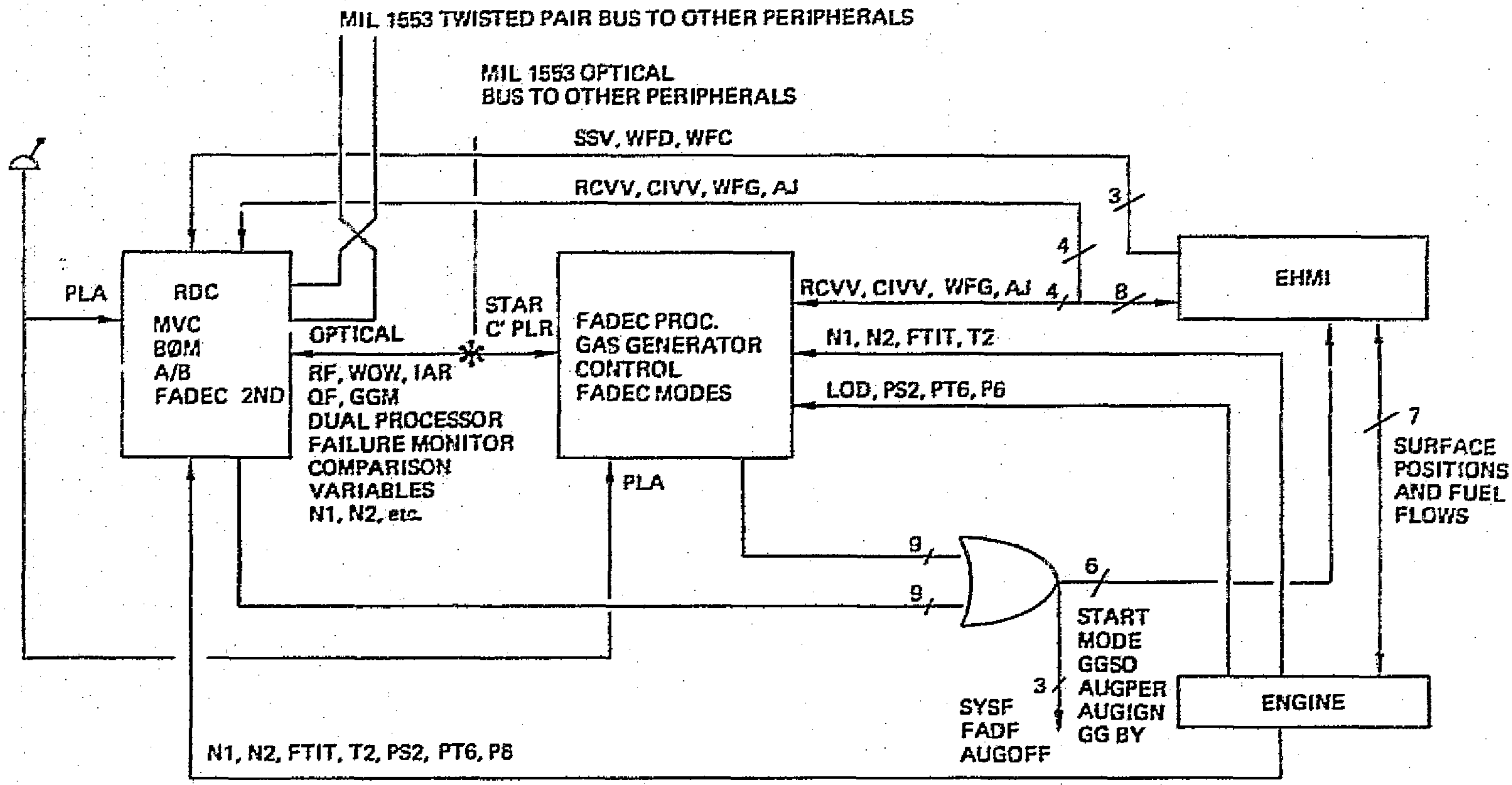


Figure 3.5-1 Proposed PROFIT/FADEC Configuration (MIL 1553)

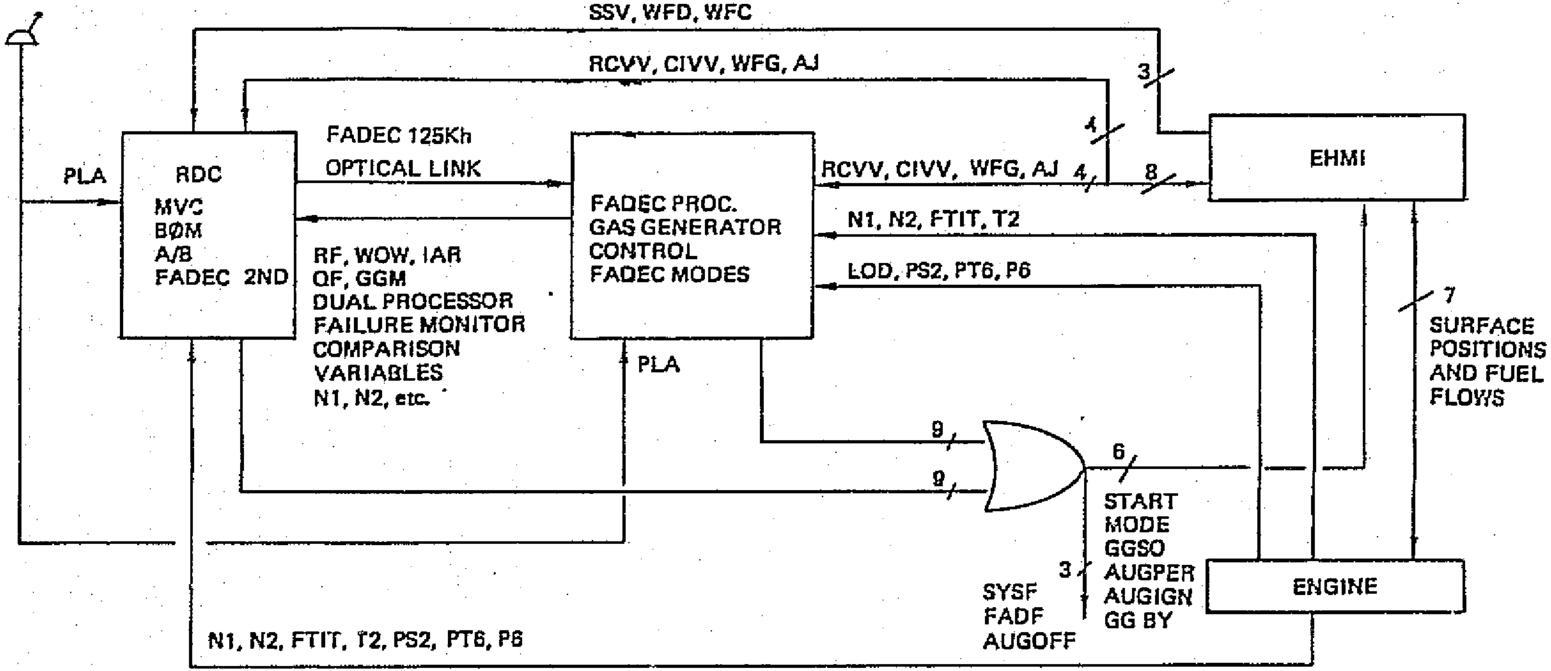


Figure 3.5-2 PROFIT/FADEC Configuration (125 khz Link)

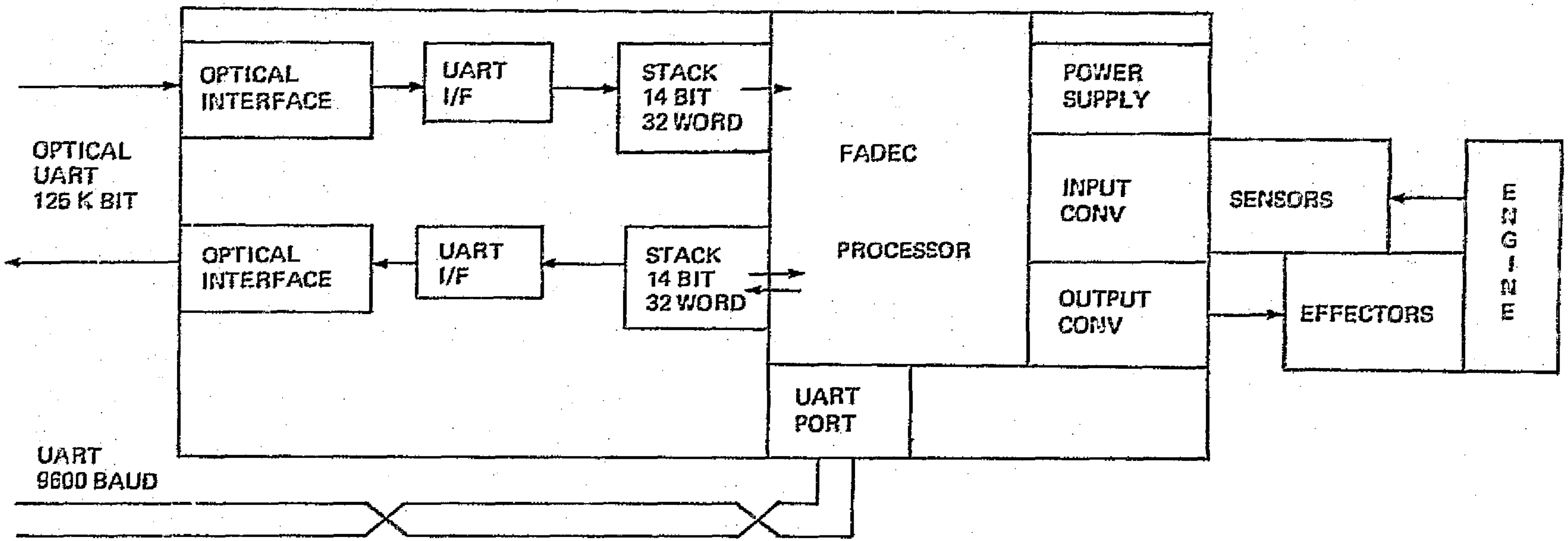


Figure 3.5-3a Current FADEC I/F

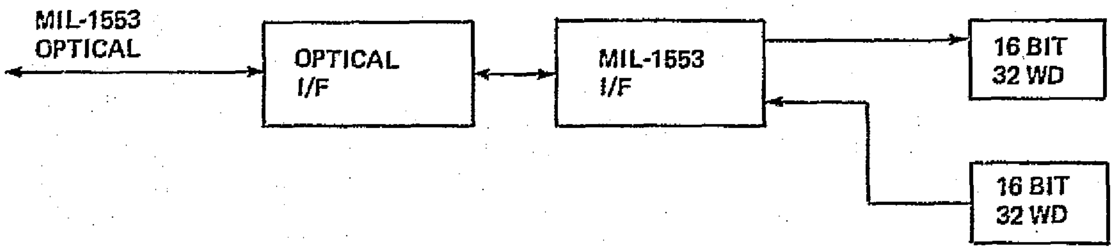


Figure 3.5-3b Eventual FADEC High Data Rate I/F

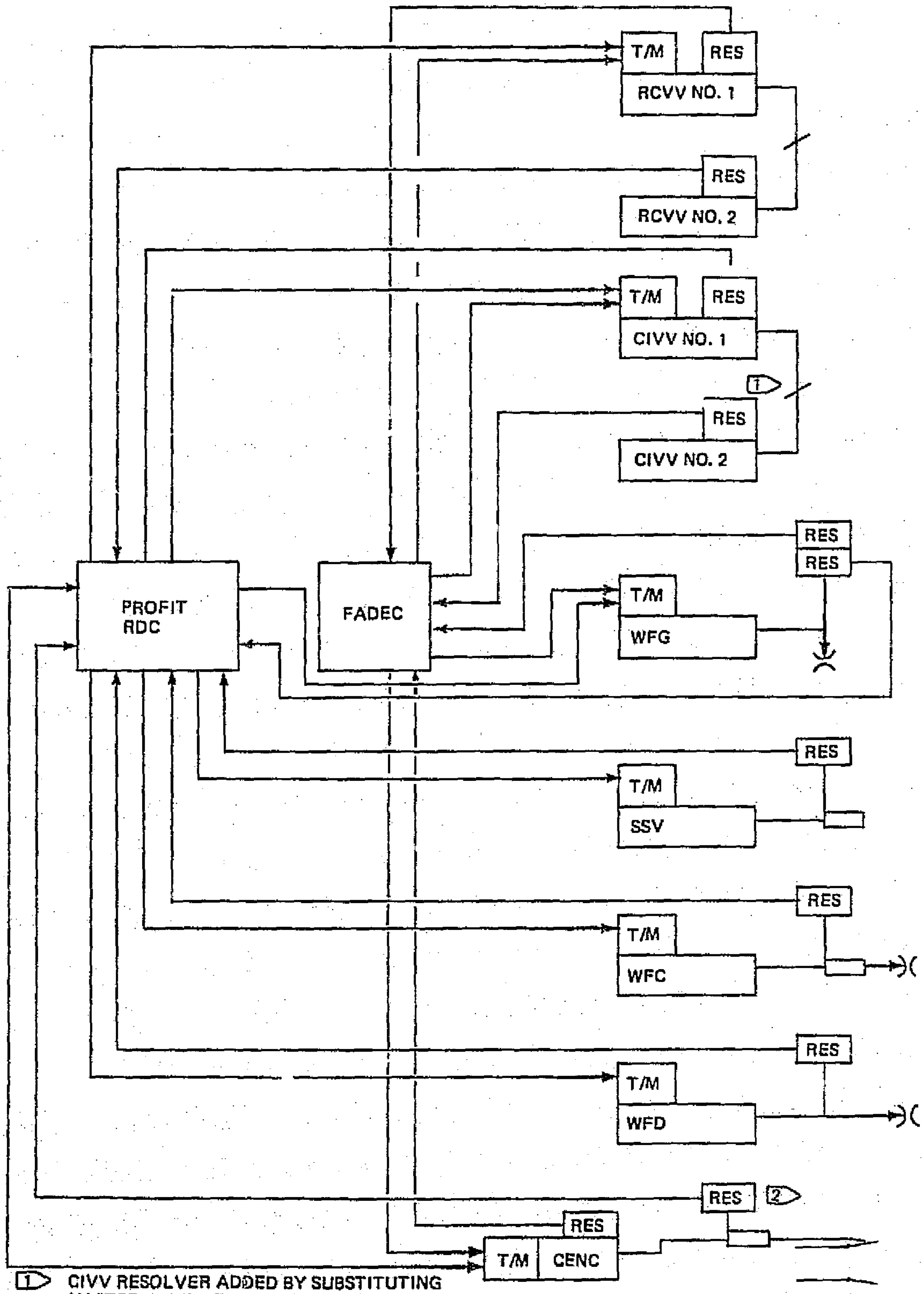
Figure 3.5-3b depicts the eventual FADEC interface-optical mil 1553A. Implementation of this interface cannot start before October 1980, due to funding, and will cost on the order of $400 K. Once implemented this interface will provide sufficient data rate capability for either servo box or dual processor information.

3.5.2 Servo System Considerations

FADEC's maximum benefit to PROFIT comes about through using FADEC as a servo box and thus reducing hardware required in PROFIT, specifically design, fabrication and test of seven demodulators and torque motor drivers. This approach, although technically feasible, is rejected because it results in an unacceptably high level of FADEC PROFIT interdependence. A requirement is established then to provide parallel servo paths to the engine from both PROFIT and FADEC. Sufficient dual resolvers exist or can be added in the electrohydromechanical interface (EHMI) to permit parallel paths for gas generator operation. Augmentor operation is implemented from PROFIT hardware only. Torque motors are dual wound. One winding is dedicated to each path, a concept proven on prior programs (EPCS, CH53). Moving the augmentor function to the PROFIT hardware implies minor changes to the FADEC software but permits full operation of the PROFIT system with FADEC removed. The resulting servo arrangement common to all systems is shown in Figure 3.5-4.

3.5.3 PROFIT Interfaces

The existing IPCS resolver-to-digital converters are compatible with the EHMI resolvers. These units convert the resolver information to a pulse whose width is proportional to resolver angle. The PWM signal is then converted to parallel digital form and passed to the DCU. The PWM signal is also available for analog demodulation. Each servo requires loop closure electronics including demodulation, see Figure 4.12-1. Seven such circuits are required, see Table 2.5-2.



1 CIVV RESOLVER ADDED BY SUBSTITUTING MASTER CYLINDER ASSY FOR SLAVE

2 AJ RESOLVER MOUNTS TO EXISTING INSTRUMENTATION PAD

Figure 3.5-4 FADEC/PROFIT Servo Arrangement

New interfaces are required to communicate with any of the FADEC data interfaces. Figure 3.5-5 depicts the electronics required for both the low and high frequency UART and mil-1553. All interfaces are operated through the HDC-601 input and output bus for simplicity. In this arrangement mil-1553 throughput will be limited to roughly 200 kbits by DCU cycle time considerations. No data transmission requirements approaching this have been identified. A DMA based mil-1553 interface would provide faster throughput but would require more design and development effort.

The circuitry of Figure 3.5-5 consists of a converter which multiplexes the HDC-601 16 bit I/O buses into an 8 bit bidirectional bus compatible with the 8 bit µprocessor and USART chip. The USART chip is available from various vendors and as indicated can be operated either at 9,600 baud or 125 KHz and either twisted pair or optical link communication can be provided.

The 8 bit bidirectional bus also communicates with a µprocessor based bus control interface unit (BCIU) which performs mil-1553 protocol and data receipt transmission tasks. This unit is currently under development for a B-52 avionics improvement program and similar ones are available from a variety of vendors and programs. Thus, the cost of this function should be low.

The hardware can be arranged in a building block manner—Card 1 implements the low frequency UART I/F. Addition of the optical elements to Card 1 and implementation of the µprocessor and buffer storage on Cards 2 and 3 provides 125 KHz capability. Finally, addition of the mil-1553A modems and fibreoptics to Cards 2 and 3 provides the mil-1553 capability. If the system is implemented sequentially significant software and interrupt structure changes are required at each step in the development process.

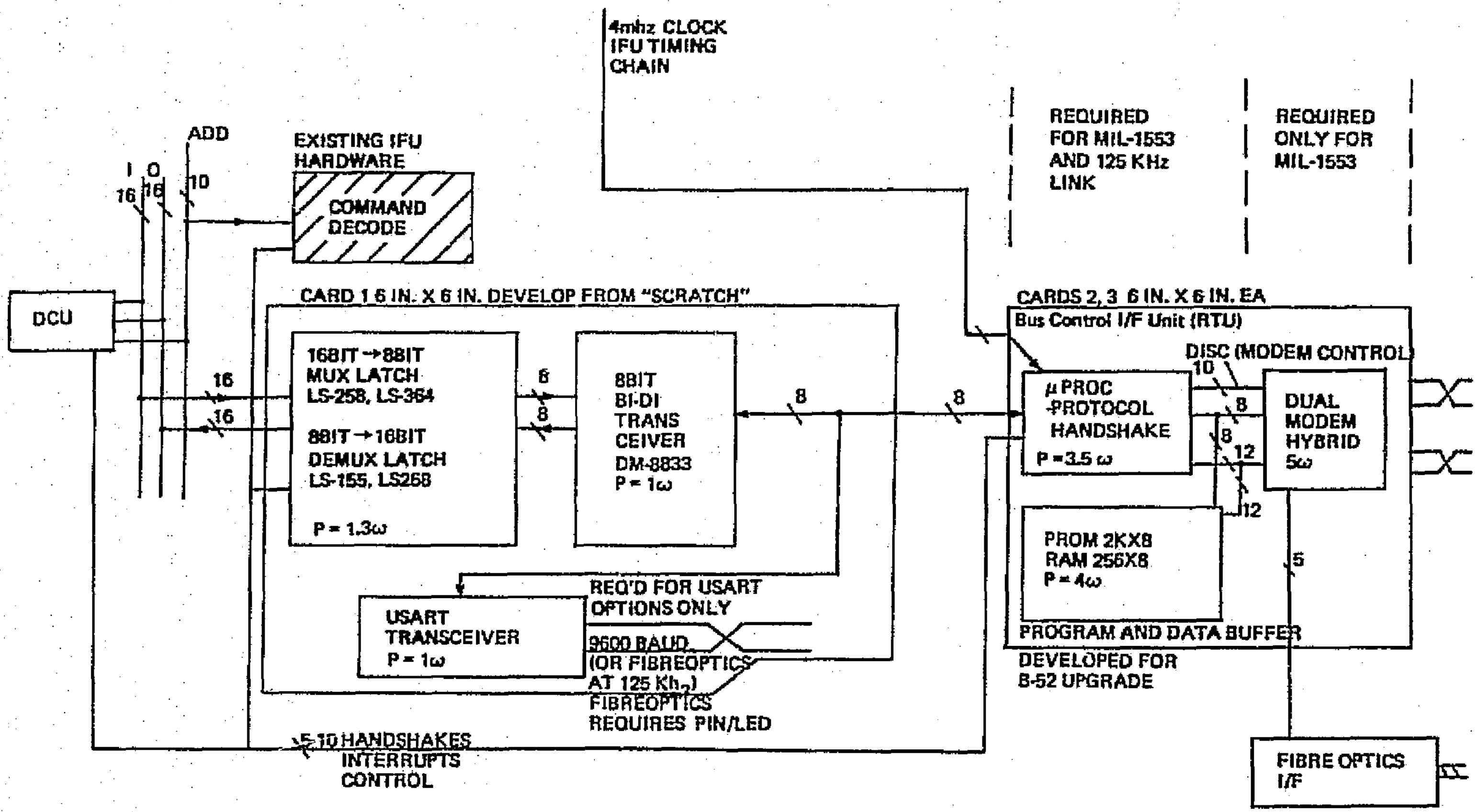


Figure 3.5-5 Serial Interface Development

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The hardware approach presented here is clearly not the only one possible. One could for example use the FADEC approach to the 125 KHz system of buffering the UART output into a dual port RAM using some minimal control logic. The μprocessor RAM approach is adopted because space and power are not severe constraints and the μprocessor design incorporating the mil-1553A interface already exists inhouse. Thus, it probably can be implemented less expensively in the small quantities involved than could a dual port ram and it grows easily into a mil-1553 interface.

System Synthesis

A matrix of possible system data links and configurations was considered. Most options were rapidly ruled out due to constraints leaving the systems of Figures 3.5-1, -2 as the viable alternatives.

The 9,600 baud UART provides a simple and convenient interface with adequate bandpass to permit FADEC to operate as a servo box or to provide engine health monitoring information. It cannot provide dual processor operation and thus limits the amount of FADEC research that can be done. As a result it is considered unacceptable.

Various alternatives to the recommended parallel servo arrangement were considered. No parallel servo path, using FADEC as a servo box, is technically practical but unacceptable because it makes PROFIT dependent on FADEC and provides no capability for dual processor operation. Since the necessary cards will fit in the IFU a peripheral servo box, considered initially as a way of offloading the IFU, has no merit. An airframe mounted high reliability research control plug compatible with FADEC was also considered as a means of both insuring against FADEC failure, providing expanded research benefits, and offloading both IFU and DCU. This approach was abandoned partially because off loading the DCU/IFU is not essential and partially because the cost and schedule requirements of such a program are not consistent with PROFIT.

The system of Figure 3.5-2 is a viable candidate because it provides dual processor operation and a parallel servo path for PROFIT operation without FADEC. The major advantage of the system is that FADEC can be used without significant hardware or software modification. The major PROFIT hardware change is the incorporation of the 125 KHz data link. PROFIT software is radically affected both by inclusion of the FADEC dual processor software and by structuring the executive to incorporate the 125 KHz data link. The major disadvantage of the system is that either it uses up IFU volume and development effort without providing inherent expansion capability or else involves building 90% of the mil-1553 interface.

The system of Figure 3.5-1 is more desirable than that of 3.5-2 since it provides long term expansion capability for PROFIT through the mil-1553 bus. From a PROFIT cost risk standpoint it is no more expensive in the near term than the 125 KHz system because most of the mil-1553 hardware is available from other programs. Long term costs are reduced because system software and hardware do not have to be redesigned and retested to accommodate 1553 at a later date. The disadvantage of the system is that FADEC rework and retest is required to implement 1553. This rework is roughly estimated to cost $400 K. Assuming an FY 80 start for this rework, a schedule as shown in Figure 3.5-6 is possible for the PROFIT program. If necessary PROFIT could proceed through the entire engine test program without FADEC. FADEC could then be incorporated onsite at DFRC using the real time simulator and local sea level facility to check out the dual processor mode. The dual processor mode would previously have been checked at bench in the current FADEC program and the modified FADEC would have been checked out in the dual processor mode at an independent bench test.

3.5.4 Recommendation

The system of Figure 3.5-1—mil-1553 data bus communications and a parallel servo path is the recommended configuration. If the Navy is unable to fund the required FADEC modifications the 125 KHz data link is a workable stop

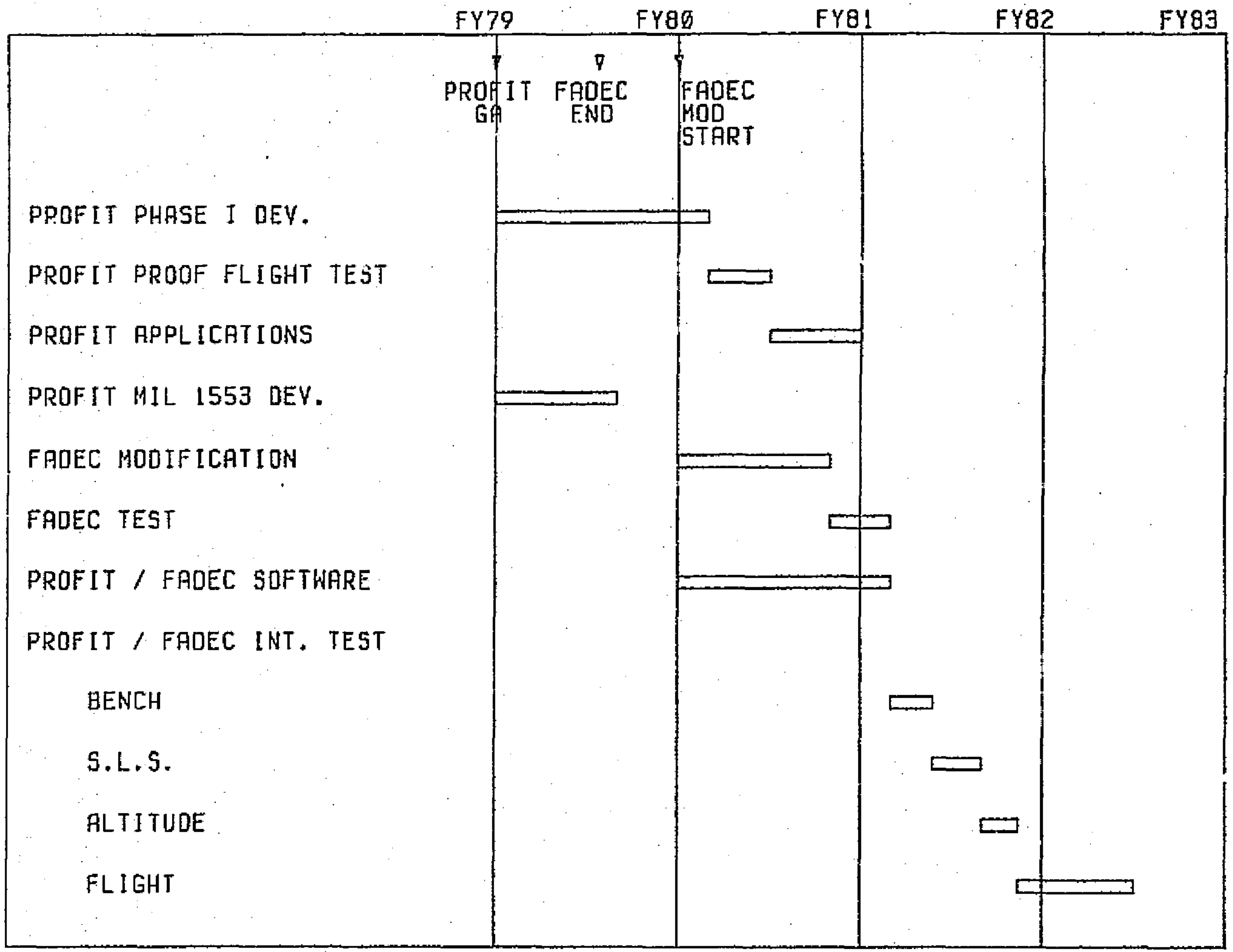


Figure 3.5-6 PROFIT/FADEC Program Schedule

gap communication link. However, its long term cost will be higher and its research experience less generally applicable than that of the preferred approach.

4.0 HARDWARE SUBSYSTEM DESIGN, ANALYSIS, & TEST

The following paragraphs document design, analysis and test of various PROFIT hardware subsystems. Because substantial portions of PROFIT hardware already exist and because the development of new subsystems is continuing the documentation presented below is, in some cases, partial. Also note that Systems A and B defined in Section 2 incorporate these subsystems in different sequence and to different degrees.

4.1 SUBSYSTEM INSTALLATION

There are six portions of the PROFIT system requiring installation, in addition to existing BOM hardware. These include cockpit hardware, PROFIT aircraft wiring, cold reference box, engine transducer box, inlet transducers and ammunition bay electronics. Each installation must consider mechanical fit, thermal environment, and vibration environment. In the following paragraphs installation requirements and preliminary designs or design concepts for each portion are presented. Based on IPCS experience all electronics components are vibration isolated and thermally protected as much as practical. Every effort is made to provide a benign environment, even if not required by component specifications, in order to enhance reliability and accuracy.

4.1.1 Cockpit Hardware

Cockpit hardware will include the BOM Caution Light Panel (CLP), a stick mounted master disengage switch, and a panel or panels fulfilling command and control functions discussed in Section 2.5.

4.1.1.1 Cockpit Hardware Environmental Requirements

Cockpit hardware assemblies shall be BOM hardware (CLP), DFRC accepted components (components already in use in similiar DFRC applications), or qualified to FRC 21-2 (Ref 13) requirements as part of PROFIT testing.

4.1.1.2 Cockpit Hardware Functional Requirements

Cockput Hardware provides the following functions:

PROFIT System Pwr off/on (Separate LH, RH),
System Status Display,
Mode Selection,
Element Engage,
Mode/Gain Adjust,
Master Disengage.

Detailed requirements in some areas are not fully established at this time. These include details of fault indication, and engage sequences. The requirements above do however define cockpit hardware necessary to provide the required functions.

4.1.1.3 Cockpit Hardware Design

Figure 4.1-1 depicts the BOM CLP and its electrical interface with the DPCU. Four lights in the caution panel are used to display DPCU mode information. Two indicate left hand and right hand DPCU power off or disengaged. The other two indicate a non-critical failure of a portion of either the left hand or right hand DPCU. The PROFIT caution lights are provided with lenses of a non-standard color, as yet unspecified, to permit rapid pilot differentiation of PROFIT and basic aircraft cautions. All PROFIT caution lights will trip the master caution light when illuminated.

Figure 4.1-2 depicts the Power Control and Engage Panel (PCEP). This is one of a series of panels associated with the cockpit hardware segregated here into functional blocks. They may eventually be merged in one panel if desired. The PCEP permits the pilot to turn the two DPCU's on or off individually and to engage or disengage various elements of the system, these elements corresponding basically to applications modules. Two of the modes - Trim

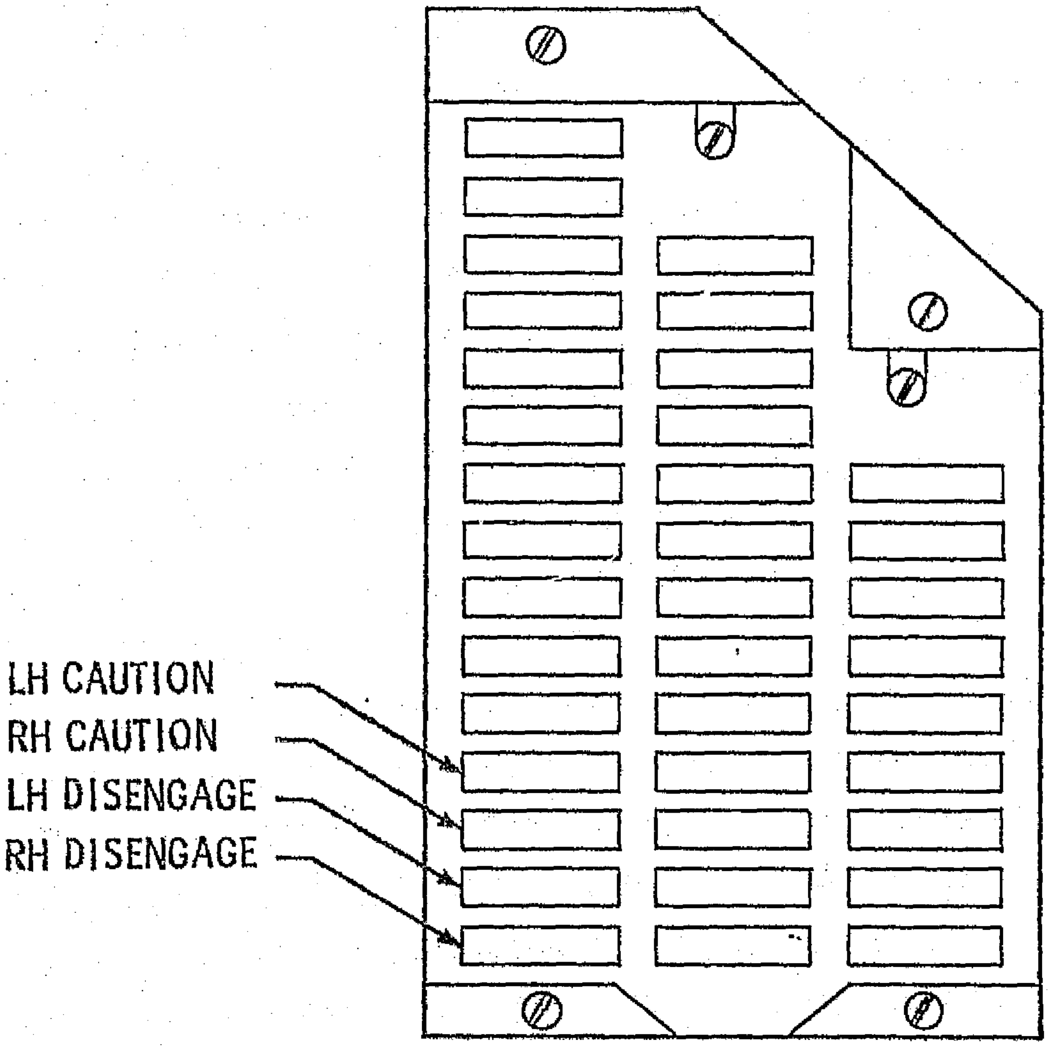


Figure 4.1-1a. Caution Light Panel

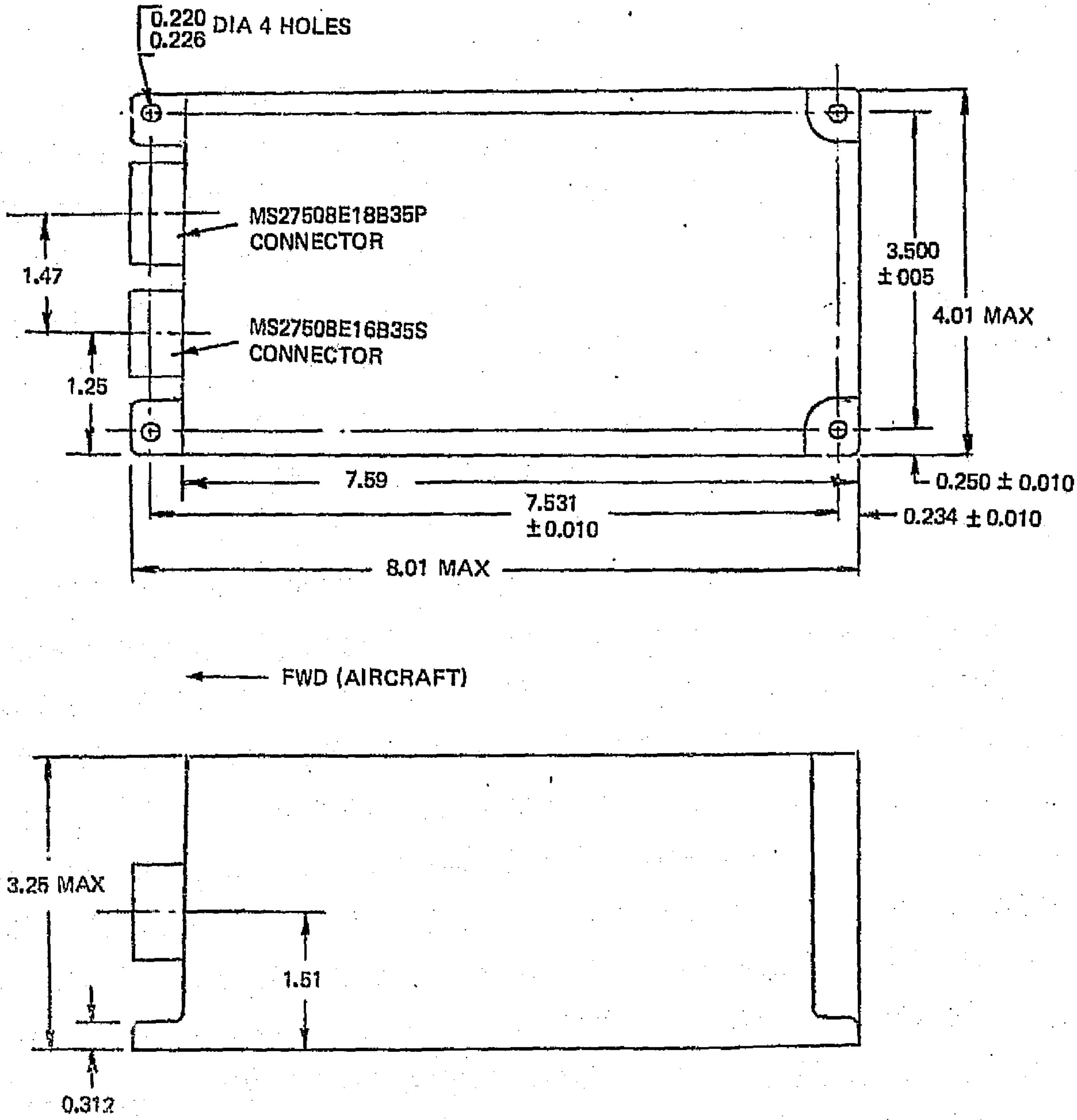
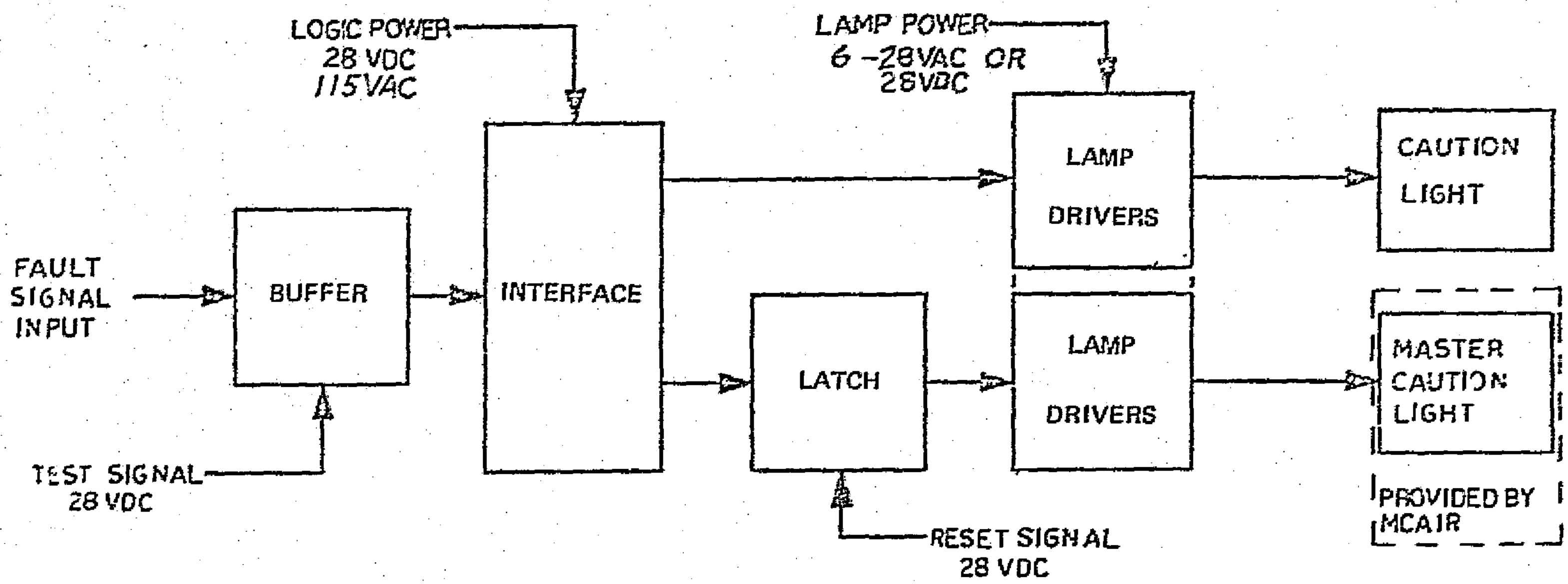


Figure 4.1-1b. Outline Dimensions for Caution Panel Logic Unit

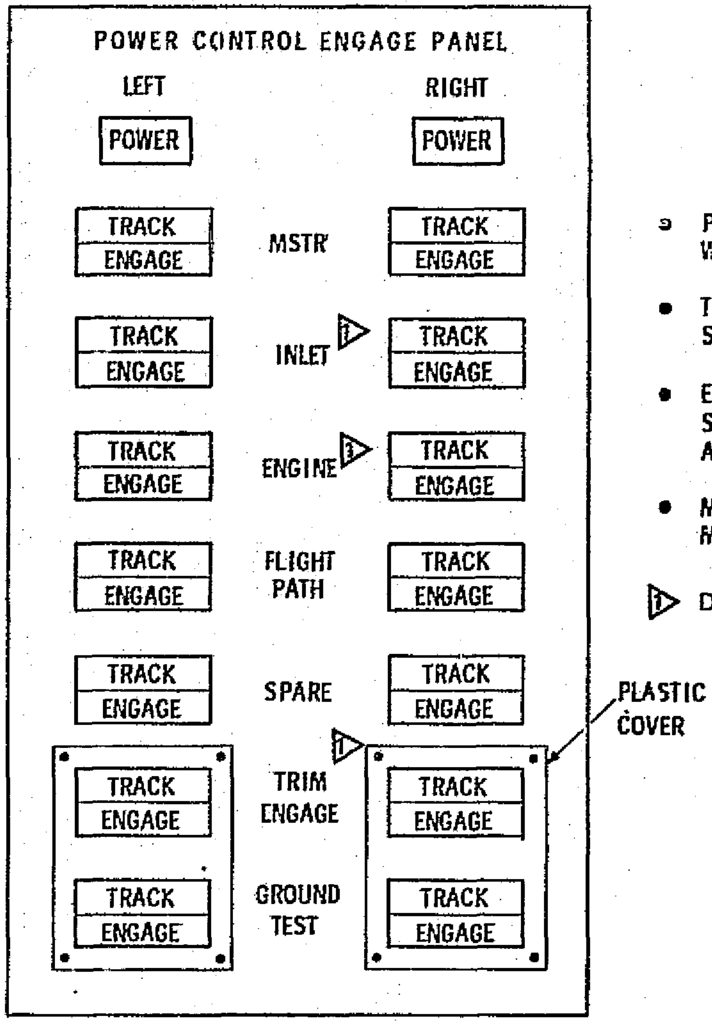


<u>Input signal</u>. The signal input shall consist of a normally grounded line. The fault signal shall consist of removing this line from ground so that it is an open circuit condition. When the input is in an open condition, the control circuit shall switch aircraft lighting power to its display element. The inputs shall draw .075 ± .025 amps when grounded. When fault is in the open condition, it shall be at a minimum voltage level of 5.0 VDC but shall not exceed the 28.0 VDC input to the unit.

<u>Input sensitivity</u>. The unit shall meet all requirements of this specification when the fault inputs are switched by "Solid State' or by mechanical switches. Fault inputs from 0 to 2.0 VDC shall be considered grounded and fault inputs passing a current of from 0 to 0.5 MA shall be considered open.

FAULT LIGHT DESIGNATIONS
FOR PROFIT
AND PIN CONNECTIONS
ARE NOT YET DEFINED

Figure 4.1-1c. Caution Light Panel Electrical Interfaces



- POWER SWITCHES LIGHT WHITE WHEN ON
- TRACK LIGHTS GREEN UNDER SOFTWARE CONTROL
- ENGAGE LIGHTS GREEN IF BOTH SOFTWARE AND HARDWARE ACKNOWLEDGE ENGAGEMENT
- MASTER DISENGAGE BY STICK MOUNTED SWITCH

1 DELETED FOR SYSTEM B

Figure 4.1-2. Power Control and Engage Panel

and Ground Test - are protected by a plastic cover and software inhibited from engagement if the airplane is airborne. Provision is made to display a track function for each mode, implying mode ready to engage, and mode engaged.

Figure 4.1-3 depicts the Mode Select Panel. Sixteen switches control the 16 bits of the DCU input discrete register. The input discrete information is decoded by the DCU software to permit selection of individual or combinations of special modes. Since these functions are under software control they are reprogrammable. Some possible modes are indicated in the sketch. Modes are entered to the computer by deliberate pilot action using the enter switch to prevent accidental mode selection. All modes can be cleared immediately through the clear switch or individually by changing the mode switch pattern and verifying data prior to entering it.

The Mode Adjustment Panel contains eight potentiometers. Four are dedicated to trimming the left hand engine through the left hand DPCU. These will not be implemented in the Development Phase of System B. The other four are available to adjust controller gains. Their function is controlled by the mode selection switches. Nominally two of the utility pots are connected to the left hand DPCU and two the right. However, the panel is arranged to permit connecting up to four pots to either DPCU.

The Cockpit Display Panel communicates DPCU information to the pilot. Six channels of analog information are provided - three from each DPCU. Four of the readouts are voltmeters - either conventional or digital - and two channels are used to operate a flight director. The panel is assembled to permit reassignment of display devices from one DPCU to the other as required by research objectives.

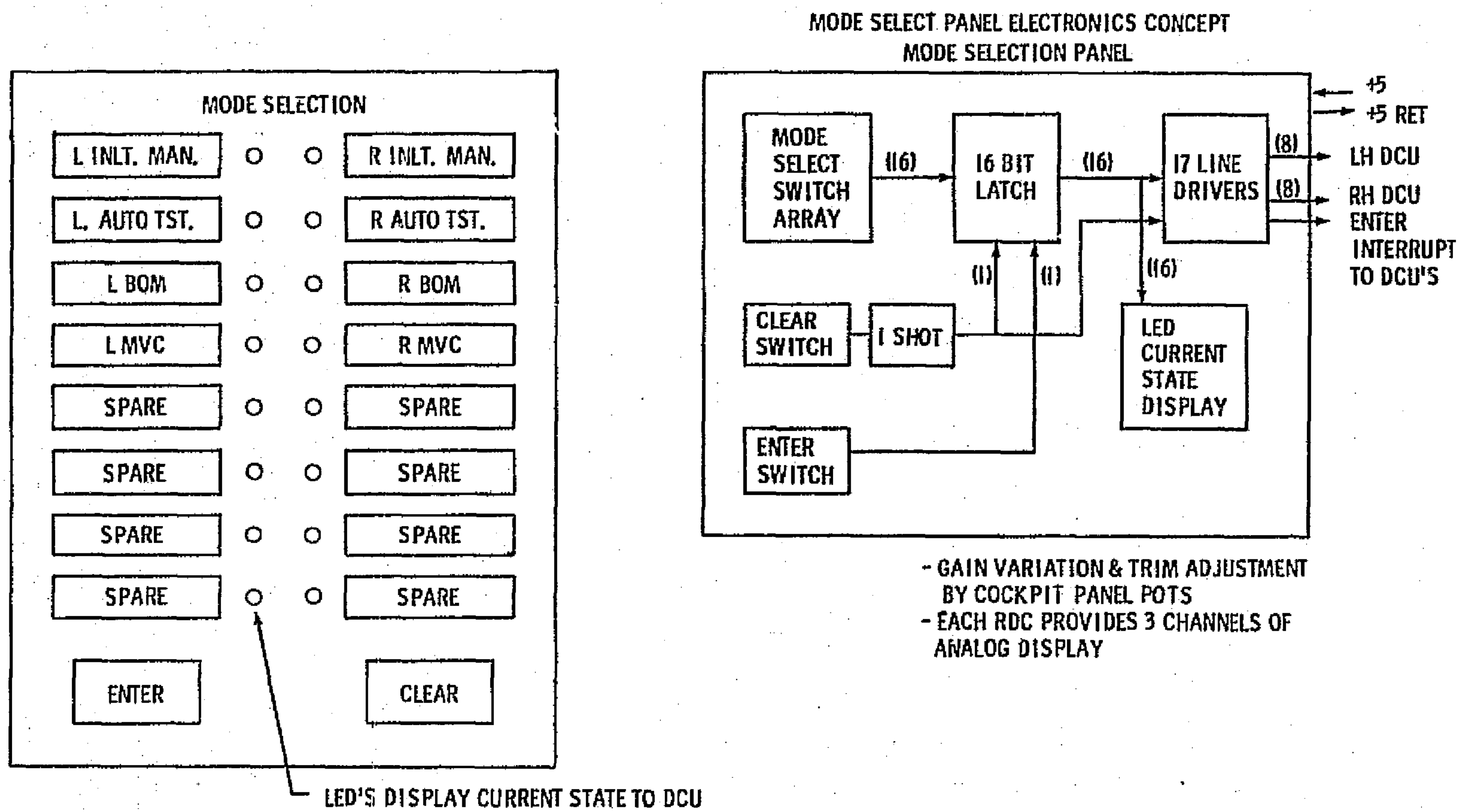


Figure 4.1-3. Mode Selection Panel

4.1.2 PROFIT Aircraft Wiring

Due to the large number of transducers and effectors involved in the PROFIT system and the central signal conditioning, as opposed to remote multiplex systems, inherent in the IFU, PROFIT wiring is a major undertaking. Because existing hardware is being installed in an existing airframe PROFIT wiring is constrained by available connectors in the IFU and available space and bulkhead locations in the F-15. Interconnect conductor requirements among system boxes were reviewed and a cabling scheme conceived which finds sufficient spare and reassignable paths to permit use of existing connectors. Figure 4.1-4 depicts on a block diagram basis the PROFIT cabling scheme. Location of wire runs on the airplane has not been established beyond the fact that all DPCU cables will terminate in DPCU connectors located at the bottom of the ammo bay. Left and right hand side wiring will be virtually identical.

Wiring practice will be based on successful IPCS experience. A single point system ground will be maintained, ample shielding will be provided, and in so far as possible noise sources and noise sensitive channels will be isolated.

4.1.3 Cold Reference Box

Location of this box has not been determined. The primary requirements is to install it in a relatively benign thermal environment (-55^{o}C. to +93^{o}C.) close to the engine bay. One box is required on each side of the airplane. All pins in intermediate connectors between sensing thermocouples and the cold reference box must be cromel or alumel as appropriate.

UNIT	ACRONYM	NOMENCLATURE
1	DCU	DIGITAL COMPUTER UNIT
2	IFU	INTERFACE UNIT
3	CCP	COCKPIT CONTROL PANEL
31	PCEP	POWER CONTROL ENGAGE PANEL
32	CLP	CAUTION LIGHT PANEL
33	CDP	CONTROL DISPLAY PANEL
34	MAP	MODE ADJUST PANEL
35	MSP	MODE SELECT PANEL
4	GSE	GROUND SUPPORT EQUIPMENT
41	CCU	COMPUTER CONTROL UNIT
42	PMP	POWER MONITOR PANEL
5	PSU	POWER SUPPLY UNIT
6	AIRFRAME	
7	MPS	MEMORY POWER SUPPLY
8	CASIF	CAS INTERFACE
9	UIU	UPLINK INTERFACE UNIT
10	BCRD	RECEIVER/DECODER
11	CCIF	CENTRAL COMPUTER I/F
12	ENGINE	
13	CRB	COLD REFERENCE BOX
14	INLET	

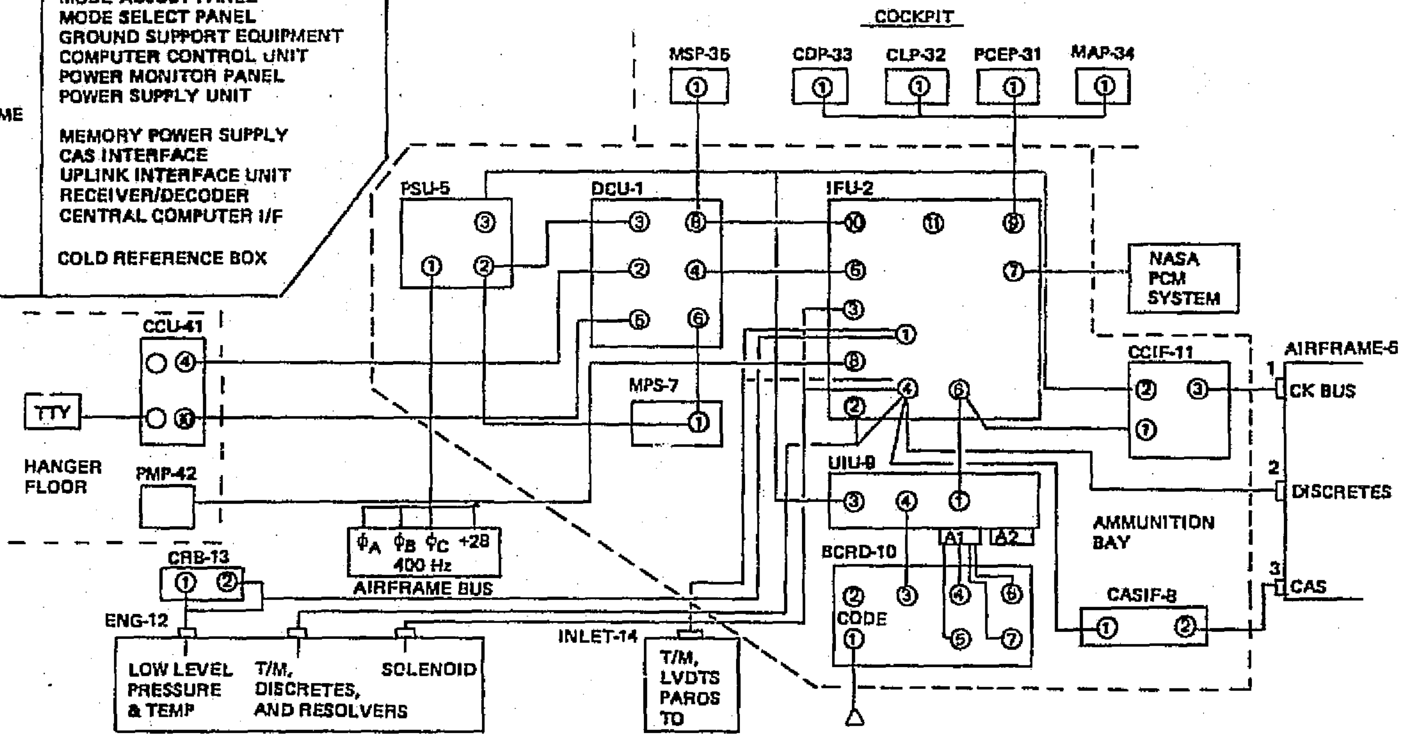


Figure 4.1-4a. Profit Cable Diagram - Left Hand Side System A

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UNIT	ACRONYM	NOMENCLATURE
1	DCU	DIGITAL COMPUTER UNIT
2	IFU	INTERFACE UNIT
3	CCP	COCKPIT CONTROL PANEL
31	PCEP	POWER CONTROL ENGAGE PANEL
32	CLP	CAUTION LIGHT PANEL
33	CDP	CONTROL DISPLAY PANEL
34	MAP	MODE ADJUST PANEL
35	MSP	MODE SELECT PANEL
4	GSE	GROUND SUPPORT EQUIPMENT
41	CCU	COMPUTER CONTROL UNIT
42	PMP	POWER MONITOR PANEL
5	PSU	POWER SUPPLY UNIT
6	AIRFRAME	
7	MPS	MEMORY POWER SUPPLY
8	CASIF	CAS INTERFACE
9	UIU	UPLINK INTERFACE UNIT
10	BCRD	RECEIVER/DECODER
11	CCIF	CENTRAL COMPUTER I/F
12	ENGINE	
13	CRB	COLD REFERENCE BOX
14	INLET	

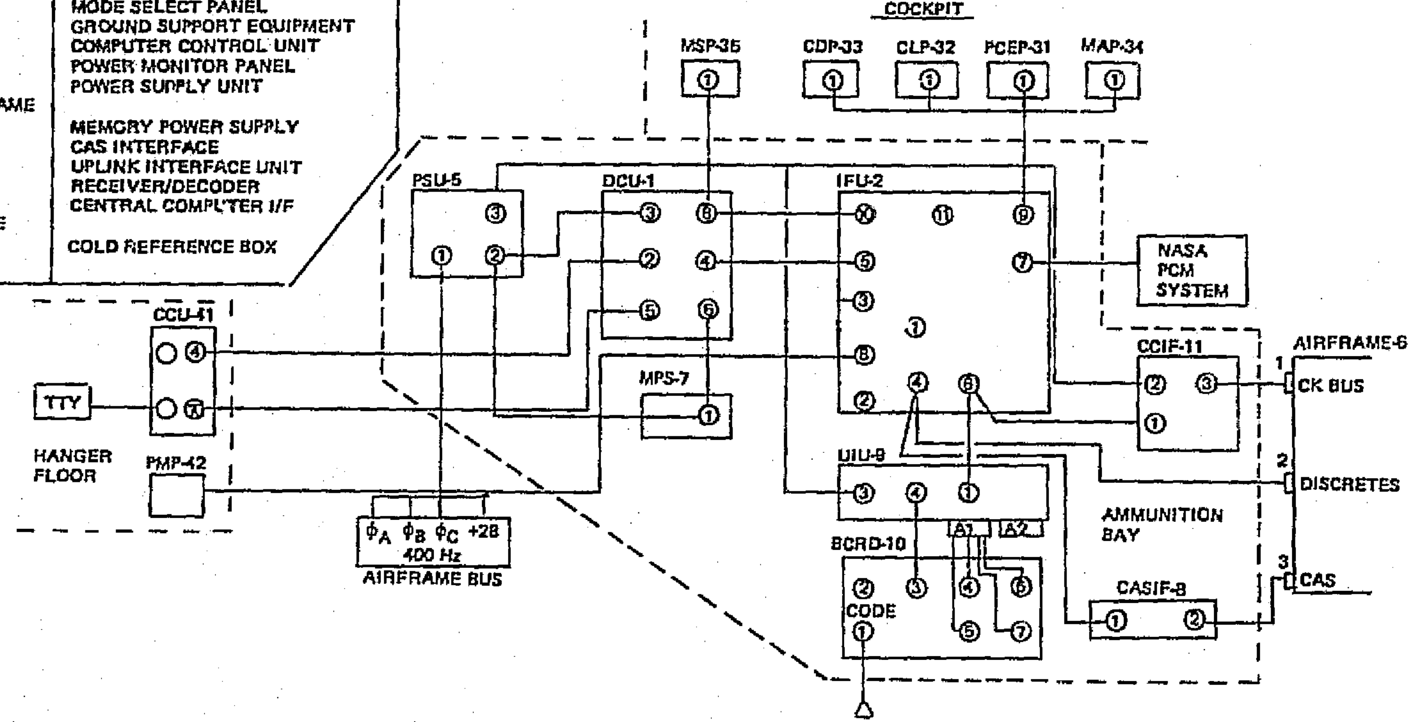

Figure 4.1-4b. PROFIT Cable Diagram - Left Hand Side System B

4.1.4 Inlet Transducer Installation

Because the probe pneumatic lines are routed to the EAIC location and the EAIC will be removed in the PROFIT system the inlet transducers are installed in place of the EAIC. The engine face pressure probe pneumatic lines are also routed to this location to permit mounting all quartz-crystal transducers in one location. The six transducers are mounted in a simple assembly, Figure 4.1-5, which provides vibration isolation and thermal conditioning to improve transducer reliability and accuracy. The protection provided is not absolutely essential since the transducer passed FRC 21-2 testing without it as part of IPCS DPCU qualification testing.

4.1.5 Ammunition Bay Installation

Figure 4.1-4, above, indicates the array of components to be installed in the ammunition bay. All elements shown are duplicated in the completed PROFIT system except the UIU which is shared by the LH and RH systems.

4.1.5.1 Ammunition Bay Environmental Requirements

The primary environmental requirement in this area is to maintain DPCU cooling air inlet temperatures and flows as indicated in Table 4.1-1 with the indicated heat load, assumed equivalent to input power. Reference 14 indicates this can be achieved within the capacity of the existing avionics cooling system by plumbing a 4.5 square inch area duct from the FCS system to the ammunition bay. The routing of this duct to the bay has not been determined but should be practical since the ECS plant is relatively close to the ammunition bay and cooling is currently provided to the area by a 1 inch diameter line.

The individual boxes installed in the bay will comply with FRC 21-2 vibration requirements. IPCS experience indicates that the electronics mounting beam will probably have a significant amplifying effect at high frequency. To

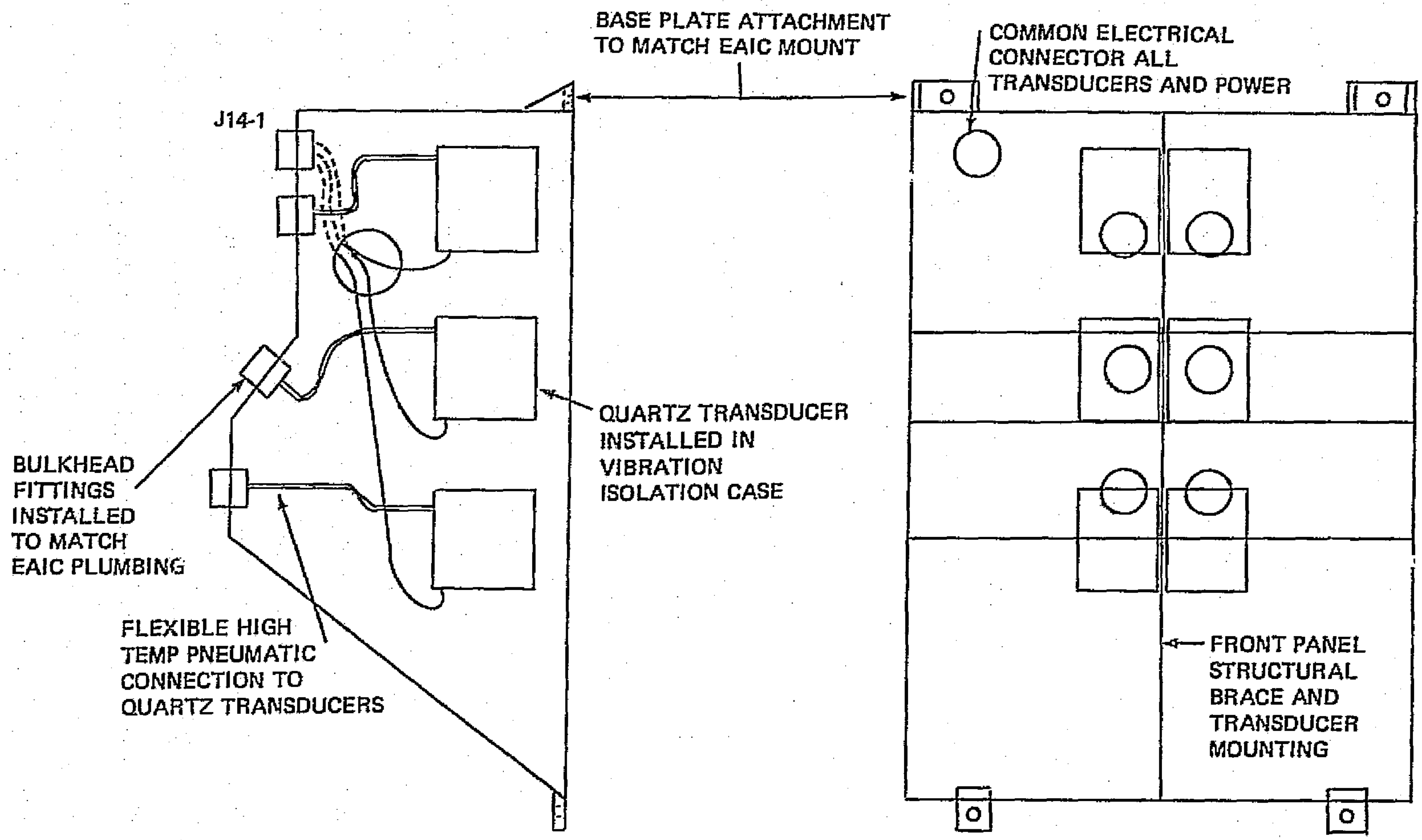

Figure 4.1-5. Inlet Transducer Installation Concept

TABLE 4.1-1

DPCU POWER AND COOLING REQUIREMENTS SUMMARY

PROFIT POWER AND COOLING REQUIREMENTS

<u>POWER</u>

115V, 3Ø, 400 hz

ØA 3.8A/DPCU

ØB 5.3A/DPCU

ØC 3.8A/DPCU

Includes .8 amp/phase for memory expansion

28 VDC @ 7.5A/DPCU

<u>MAXIMUM REQUIREMENTS</u> (2 DPCU + 20%)

115V, 3Ø, 400 hz

ØA = 9.12 A

ØB = 12.72 A

ØC = 9.12 A

28 VDC @ 18.A

Quality per MIL STD 704A

<u>COOLING</u>

3 lb/min/DPCU

1 lb/min/16k memory addition

Max inlet temp 80°F [1]

Min inlet temp 50°F

<u>MAXIMUM REQUIREMENT</u> (2 DPCU + 32k Memory Expansion + 20%)

9.6 lb/min @ 80°F max [1]

[1] Brief (15 minute) Excursion to 95°F is Acceptable

correct this the beam must be attached to the airframe through a low pass vibration isolator.

Mechanical dimensions and weights of the various units to be installed are depicted in Figure 4.1-6. Data for the CCIF, UIU, and CASIF are somewhat flexible since package design for these units is not final. The remainder of the units are existing hardware.

4.1.5.2 Ammunition Bay Installation Design

Figure 4.1-7 depicts the electronics black box installation in the ammunition bay. All components are mounted on box beams internally braced to provide rigidity. The beam is installed on the existing ammunition bay tracks. Vibration isolation is provided between the beam and the track slides to eliminate high frequency resonance of the beam. If analysis indicates it is required, the center of the beams may be sway braced to hardpoints along the side wall of the ammunition bay. The box beam, in addition to the structural function, serves as a ground plane and cold plate. Cooling air is passed down the box beams to provide memory power supply, uplink interface unit and central computer interface unit cooling. Square cooling ducts are used to conduct cooling between DPCU components in order to assure adequate space in the connector area at the bottom of the installation. An insulation blanket consisting of a thermal/acoustic outerlayer and an inner metallic layer for EMI shielding is permanently installed in the ammunition bay walls. Access to the connector area with the ammo bay access door removed is excellent and the 6 foot CCU cable requirement is relatively easy to meet.

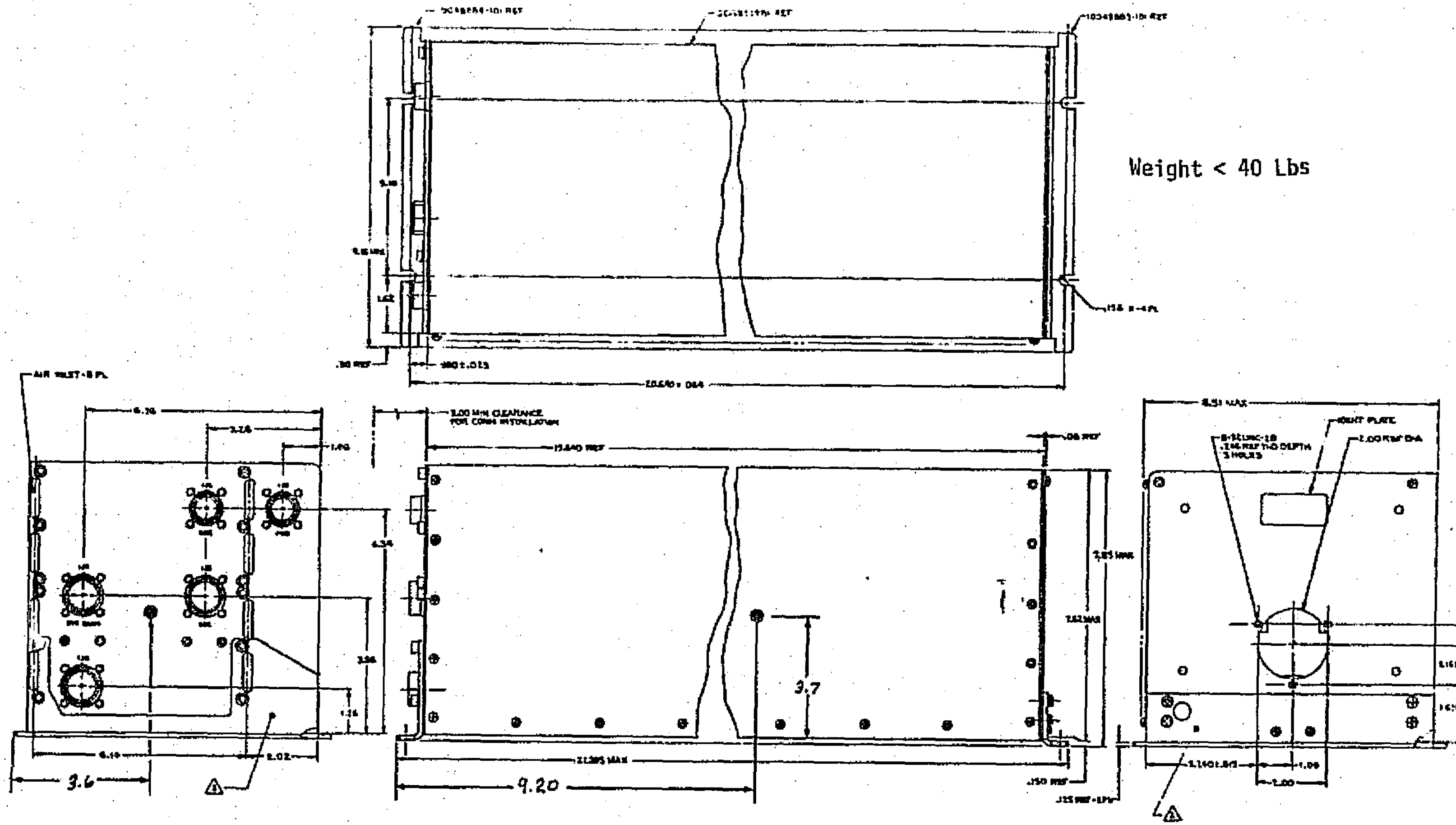

Figure 4.1-6a. Digital Computer Unit (DCU)

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Weight < 53 Lbs

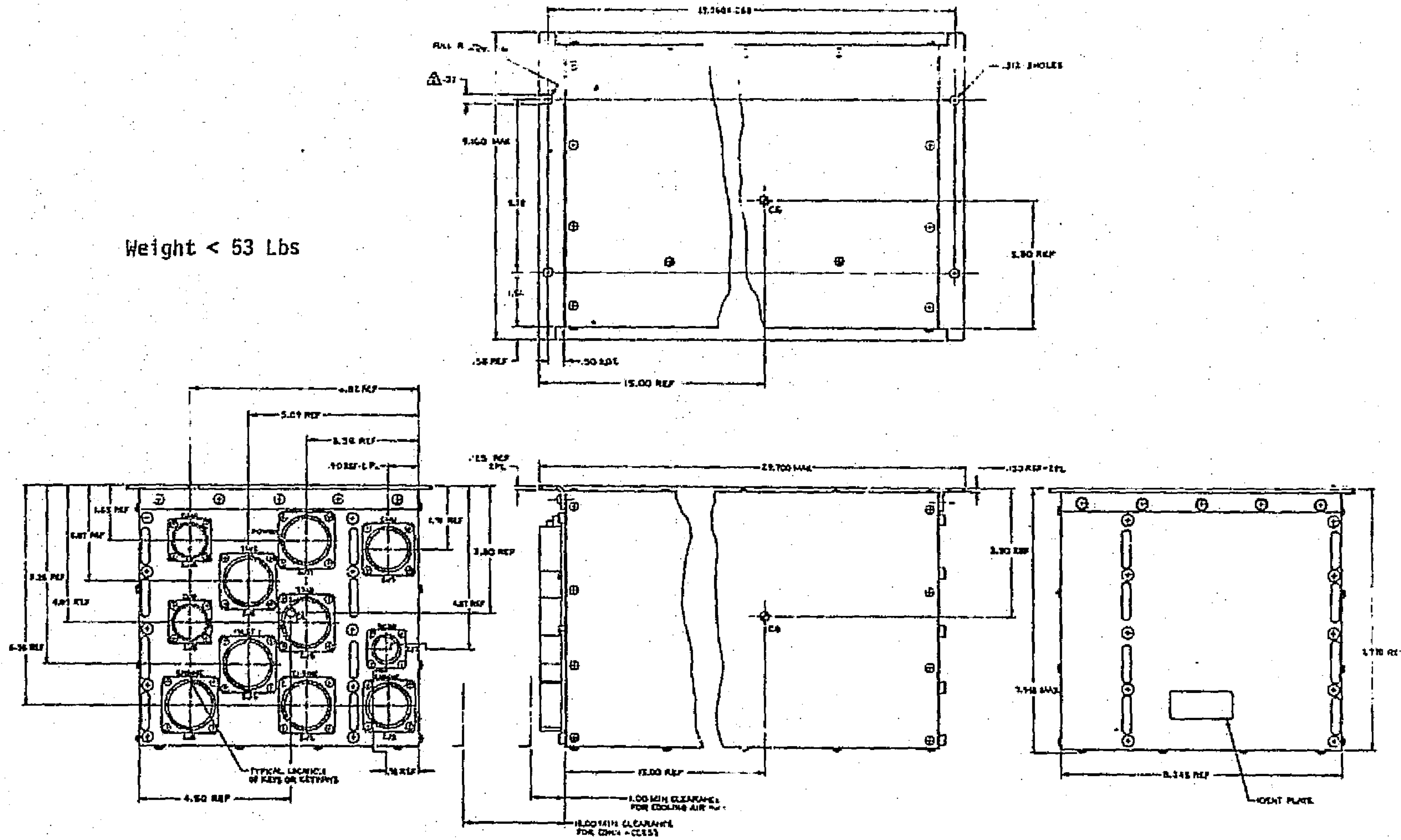
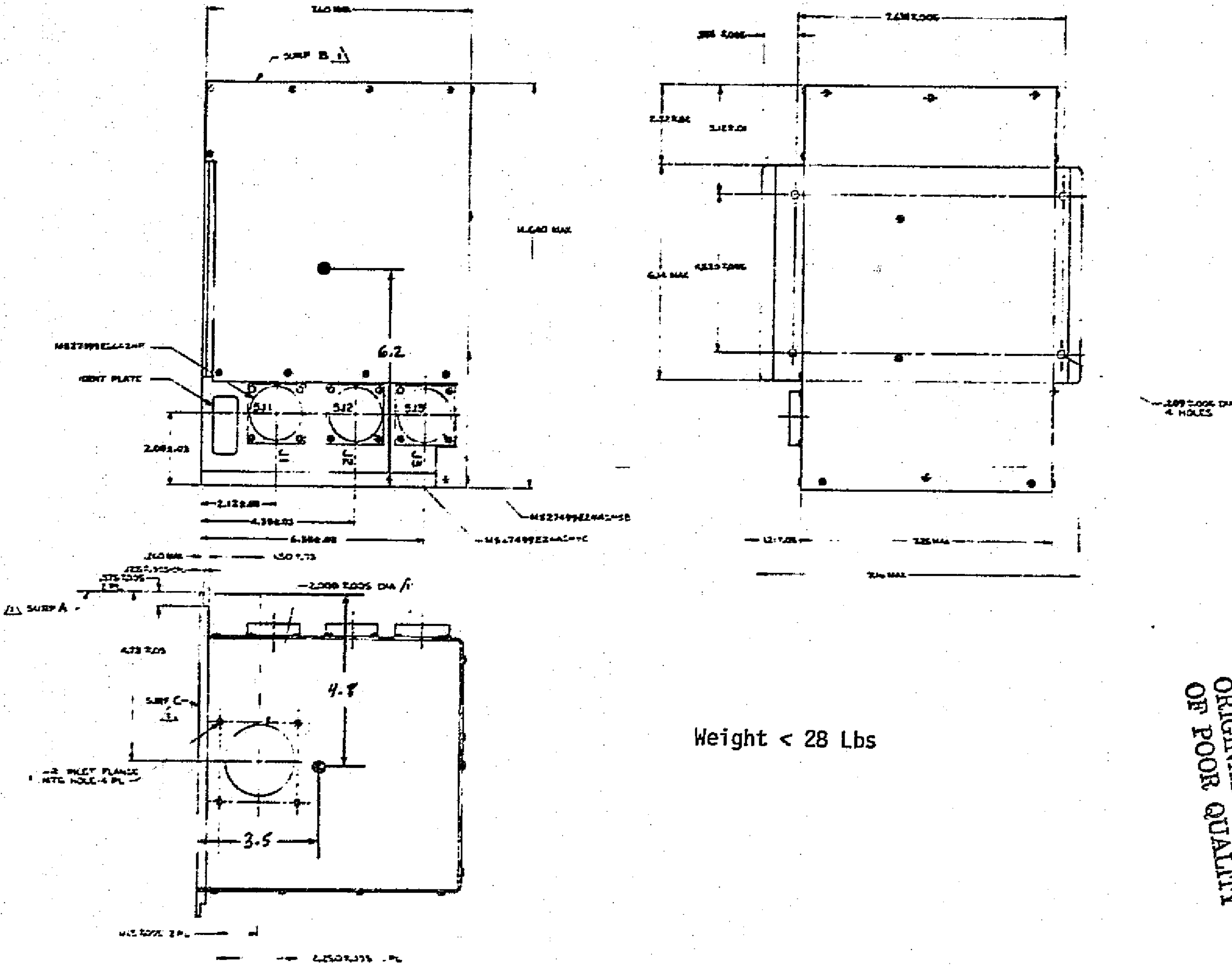


Figure 4.1-6b. Interface Unit (IFU)



Weight < 28 Lbs

Figure 4.1-6c. Power Supply Unit (PSU)

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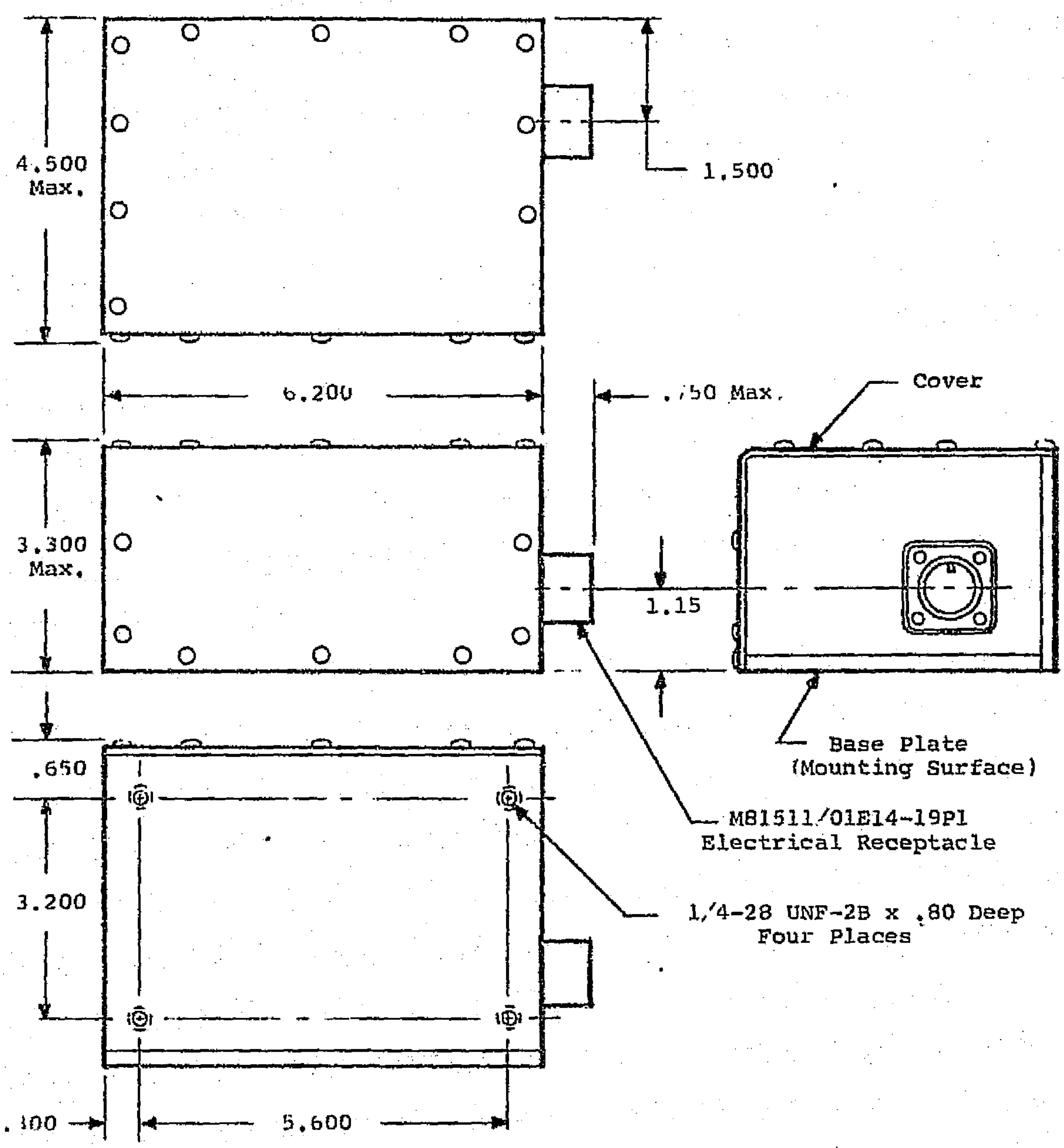

Figure 4.1-6d Memory Power Supply SEPS-8 Installation Details

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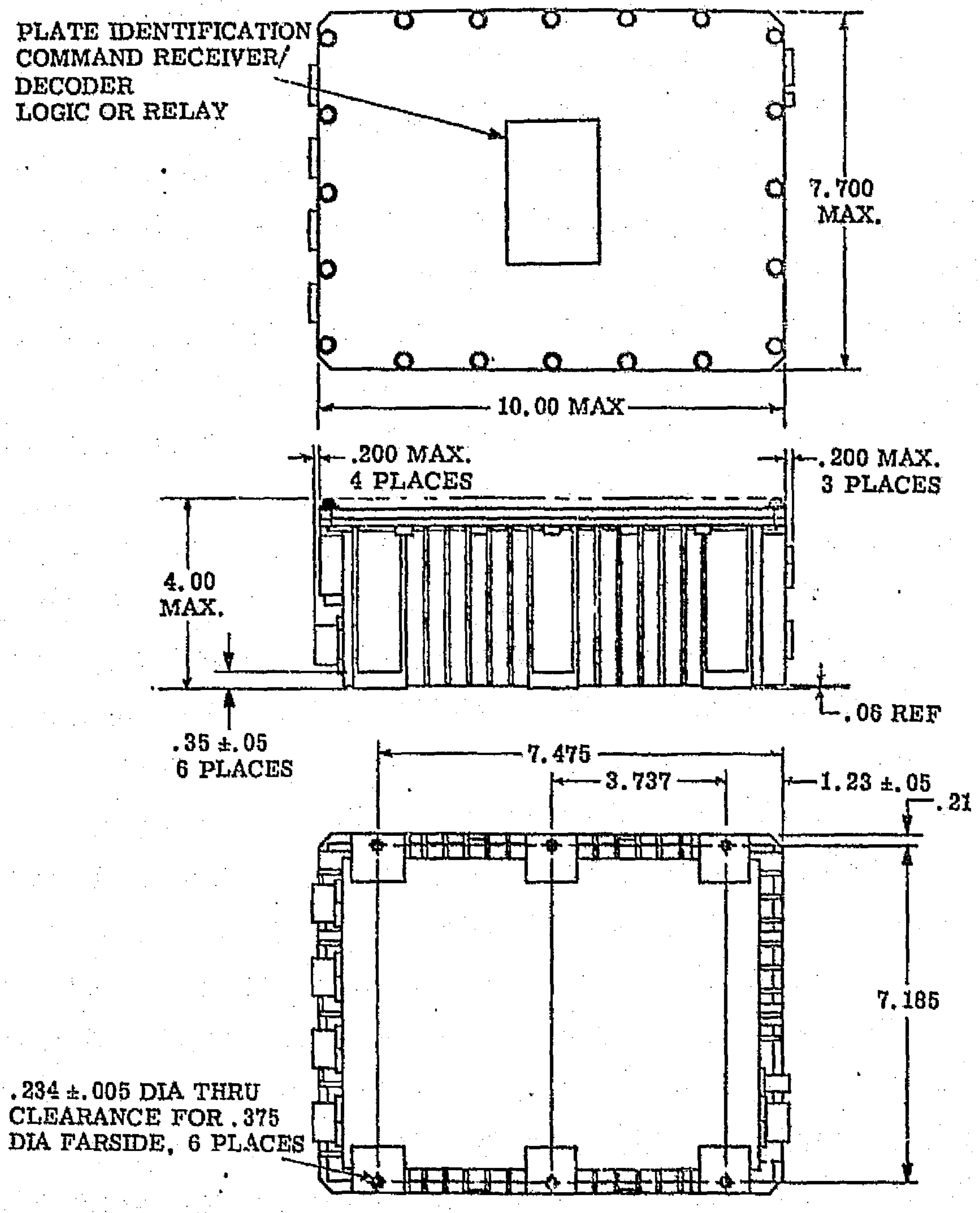
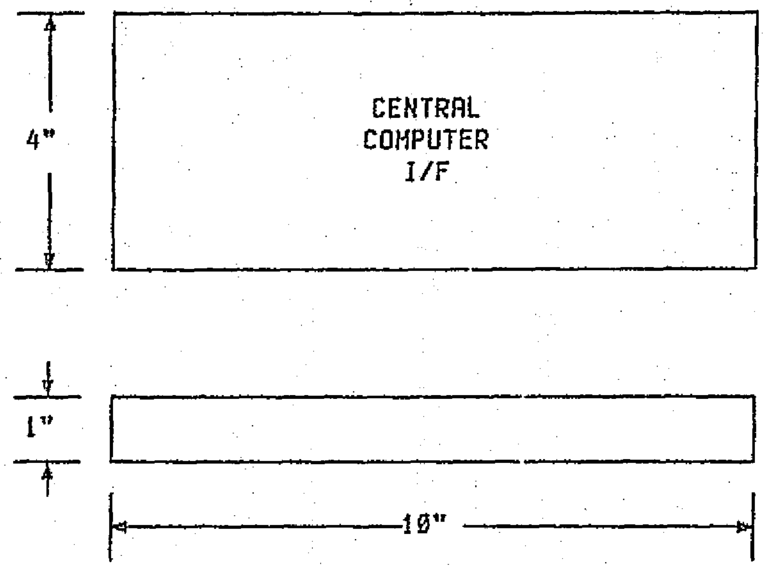


Figure 4.1-6e. Uplink Interface Unit (UIU) Envelope



NOTE: DIMENSIONS ARE FOR SINGLE I/F PAGE
2 PAGES + POWER SUPPLY ARE
REQUIRED PER DPCU

Figure 4.1-6f. Central Computer I/F Envelope

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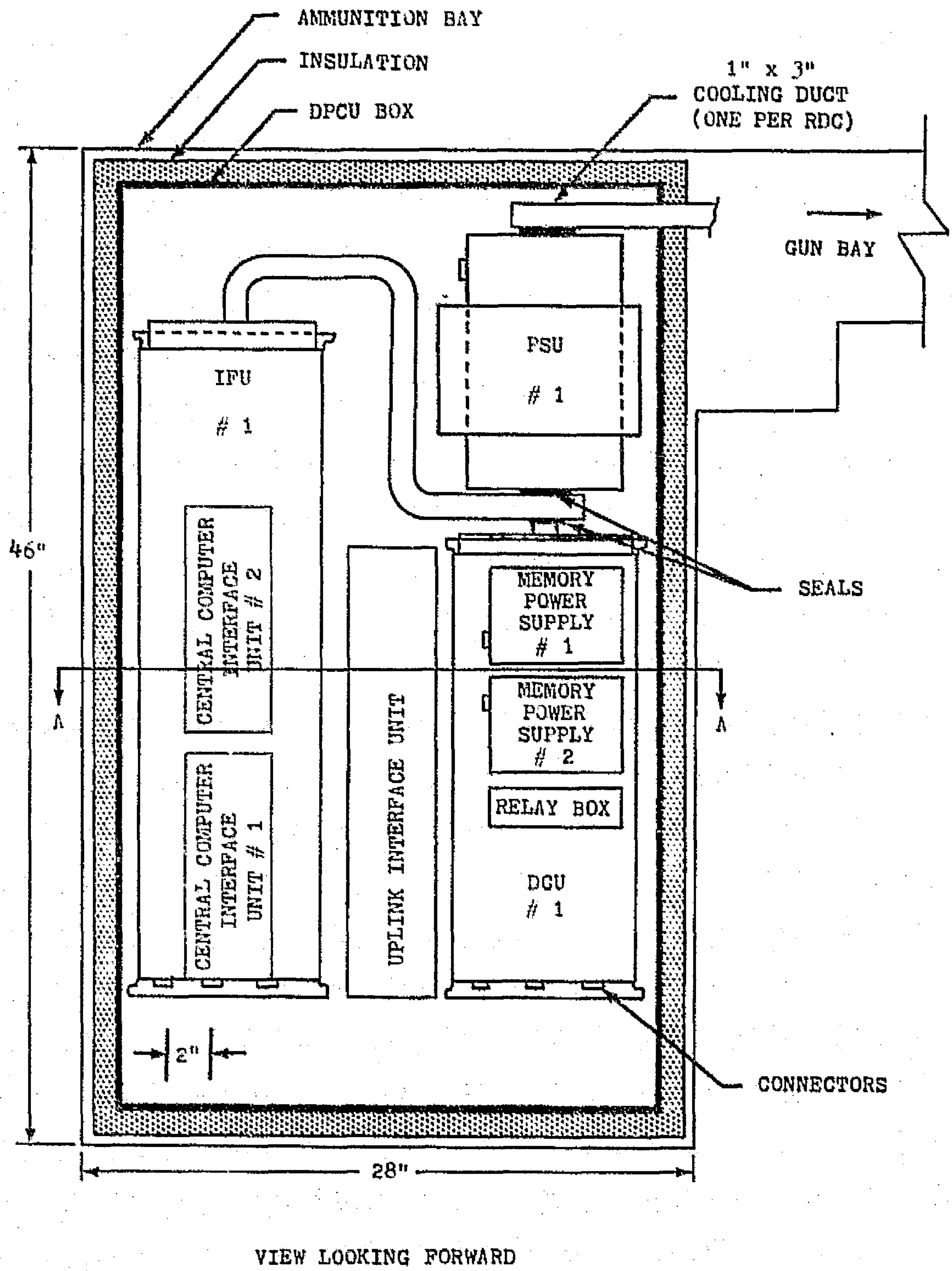


Figure 4.1-7. Installation in Ammunition Bay

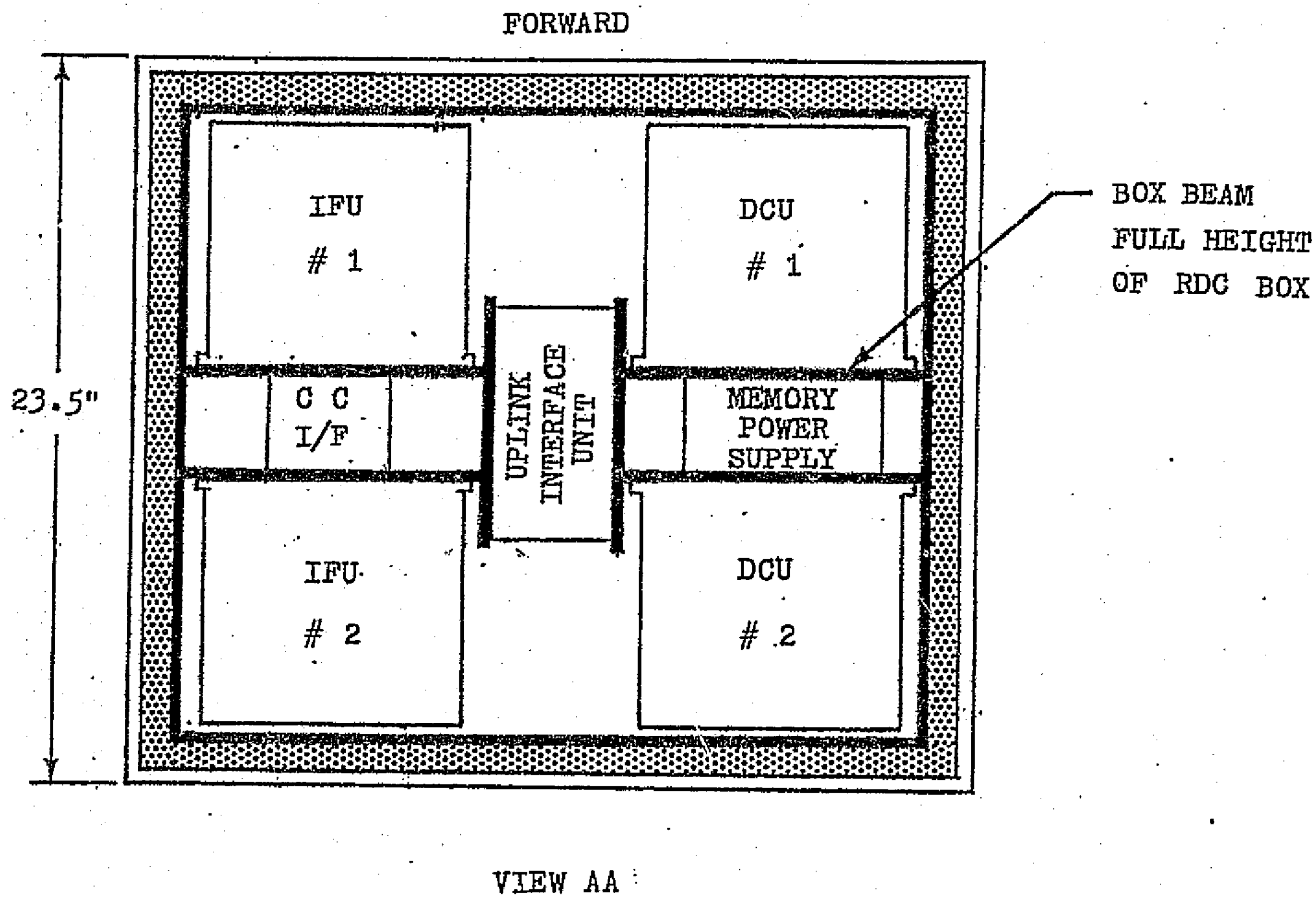


Figure 4.1-7. (Cont.)

4.2 UPLINK INTERFACE

The purpose of the uplink interface is to provide a means to transfer ground computed data to the PROFIT system in flight. Consistent with the philosophy of PROFIT this is to be done with existing hardware and provide flexibility for as yet undefined applications. Figure 4.2-1 depicts the hardware elements of the system. Data to be uplinked are generated in the RAV facility, if flight safety restricted, and in other facilities if not flight safety restricted. The RAV facility formats the data and outputs it to the Babcock encoder/ transmitter which serializes it and transmits it to the Babcock BCRD-31 receiver decoder on the airplane. This unit, whose output is 4 parallel 16 bit words, is interfaced to the DCU input bus and interrupt structure by a digital multiplexer (Uplink Interface) whose design and test is discussed below.

4.2.1 Uplink Interface Design Requirements

The Babcock uplink system is bit rate limited by hardware and link design. Within that restriction the uplink interface system is required to transmit a message of from four to an unlimited number of words selected by changes to ground and flight software. For safety purposes messages shall be transmitted including a checksum which can be verified by the receiving software. A hardware element shall be built to provide an interface between the BCRD-31 output and the HDC-601 input bus. BCRD-31 interfaces are defined by Figure 4.2-2.

NASA DFRC currently uses both the Babcock BCRD-31A and -31B Receiver/Decoders, hence their use in the PROFIT system is assumed. The 16 bit parallel output of this unit is input to the DCU through a new IFU interface card. The maximum uplink data rate (-31B) is 9600 bits per second and for preliminary analysis a 24 word uplink message is assumed.

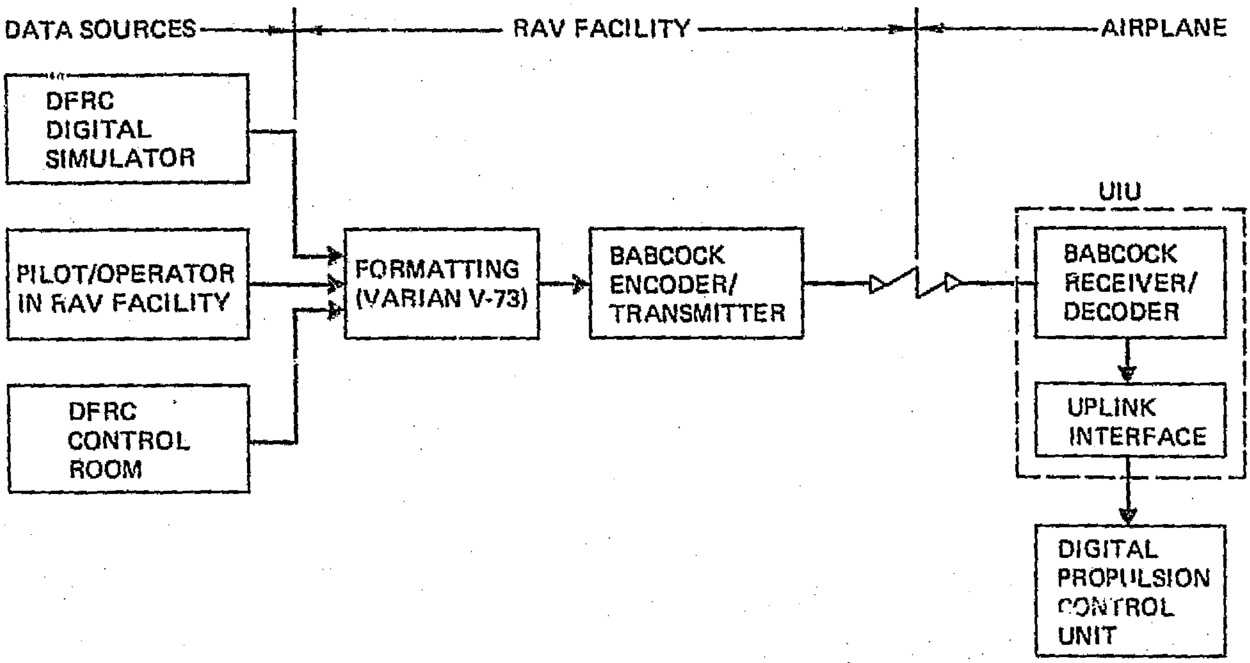


Figure 4.2-1. PROFIT Uplink Data System

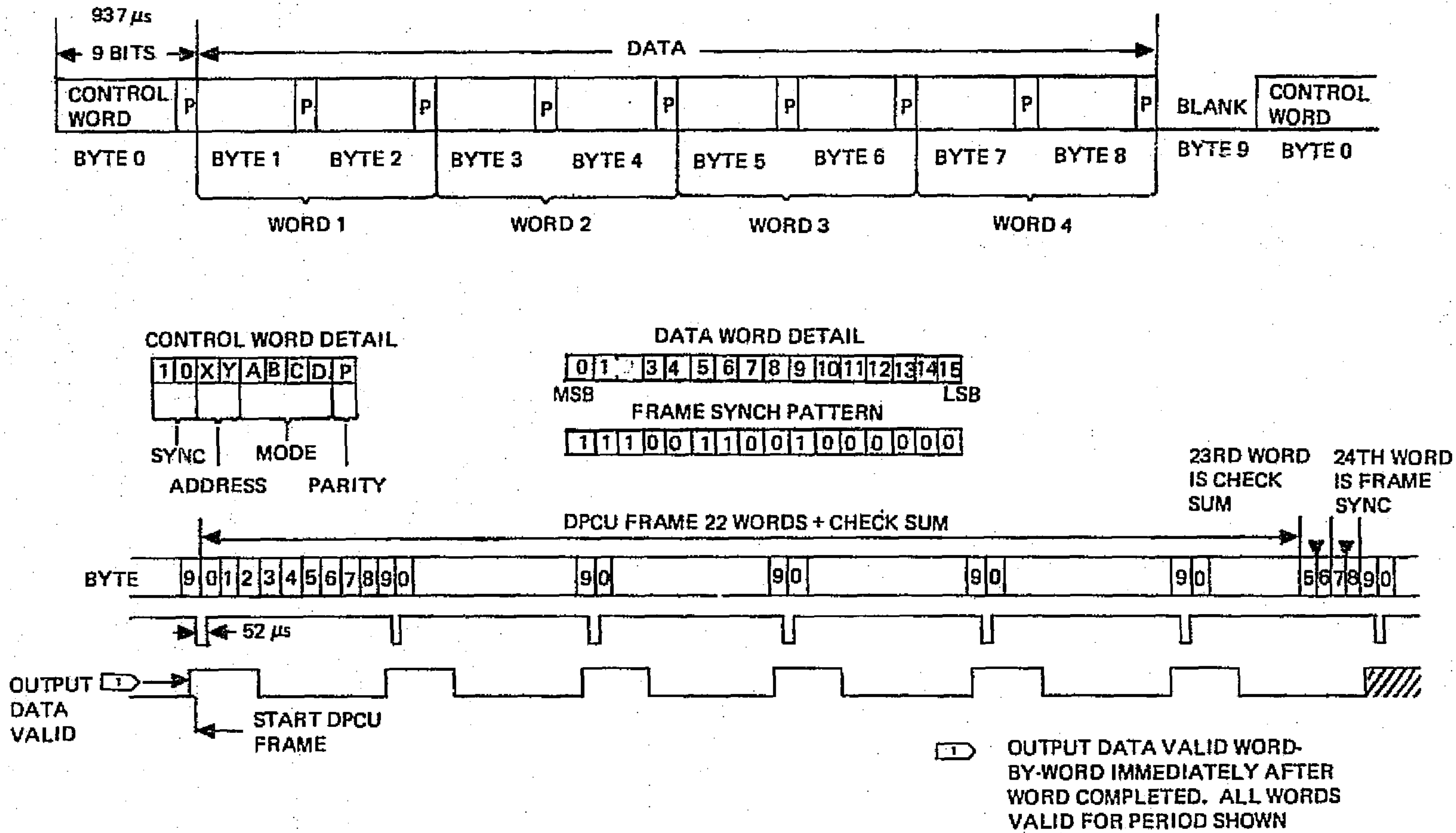


Figure 4.2-2a. Receiver/Decoder Data Format

FIGURE 4.2-2b

RECEIVER/DECODER (BCRD-31) SPECIFICATIONS

a.	Input Voltage:	28 ± Vdc
b.	Power Consumption (Maximum):	35W Maximum (8 relay boards and 32 Vdc power supply)
c.	Sensivitity:	7 μV minimum rf signal
d.	Maximum undetected error rate at any carrier level or fade condition:	Less than 6-bit errors/hour with 64-bit frame
e.	Modulation Bandpass:	Logical 0 = 57.6 kHz ±2% Logical 1 = 43.2 kHz ±2%
f.	Information Loss Relay:	0.5 Seconds
g.	Bit Rate:	4800 Hz ±0.1% - 31A [1] 9600 Hz - 31B
h.	Frame Length:	0 to 64 data bits, 8-bit increments
i.	Rf Characteristics:	406 to 549.5 MHz, fm
j.	Deviation:	±120 kHz
k.	LO Stability:	±0.01%
l.	RF Input Impedance:	50 ohms
m.	Rf vswr:	3.0
n.	Weight	10.5 pounds
o.	Temperature:	-54° to +71° C operating
p.	Altitude:	70,000 feet MSL
q.	Vibration:	2 g's 5 to 500 Hz, 15 g's 11 milliseconds
r.	Outputs:	64 data bits TTL compatible pin connections per reference 15. Frame rate pulse J3-12. 1KΩ output impedance, TTL compatible,

[1] DPCU design to be compatible either bit rate.

Since the -31B unit has the higher bit rate of the two, and thus imposes the most severe requirements, it is used to define interface requirements. Figure 4.1-6f defines the mechanical interface. Figure 4.2-2 defines the basic electrical interface.

4.2.2 Uplink Interface Design

Figure 4.2-3 is a block diagram of the interface between the Babcock BCRD-31 and the DCU. A possible mechanical layout for the system is shown in Figure 4.2-4. Spare card slots are shown to permit use of separate interfaces to the two DPCU's.

The Babcock's four output words are stable for 3 byte times after the frame synch pulse (FRPS), see Figure 4.2-2a.

Data timing and organization are defined by Figure 4.2-2a. After the decoder is synched, the frame rate pulse precedes the control word, which is not available to the DCU. Output data are stable on the output registers for 2.86 milliseconds following the frame rate pulse. For preliminary purposes six receiver/decoder frames will constitute one DPCU frame. The 23rd word in a DPCU frame will be the checksum of the previous 22 words. The 24th word of the frame is dedicated to the frame synch function. The frame synch word used on IPCS (Barker Code) is shown although alternatives are possible.

System operation is initiated by DCU software unmasking the two uplink interrupts (data = 10, frame synch = 11) when the receiver decoder is in operation. The frame rate pulse (FRPSO), see Figure 4.2-5, is used to generate the PIL 100 data interrupt. If the Babcock word four is a synch word, SNWD1, see Figure 4.2-6, enables the PIL110 frame synch interrupt.

PIL101 clears the word select counter, Figure 4.2-7. Software then generates an INA 1424 command which enables the 153 mux to the DCU input bus through

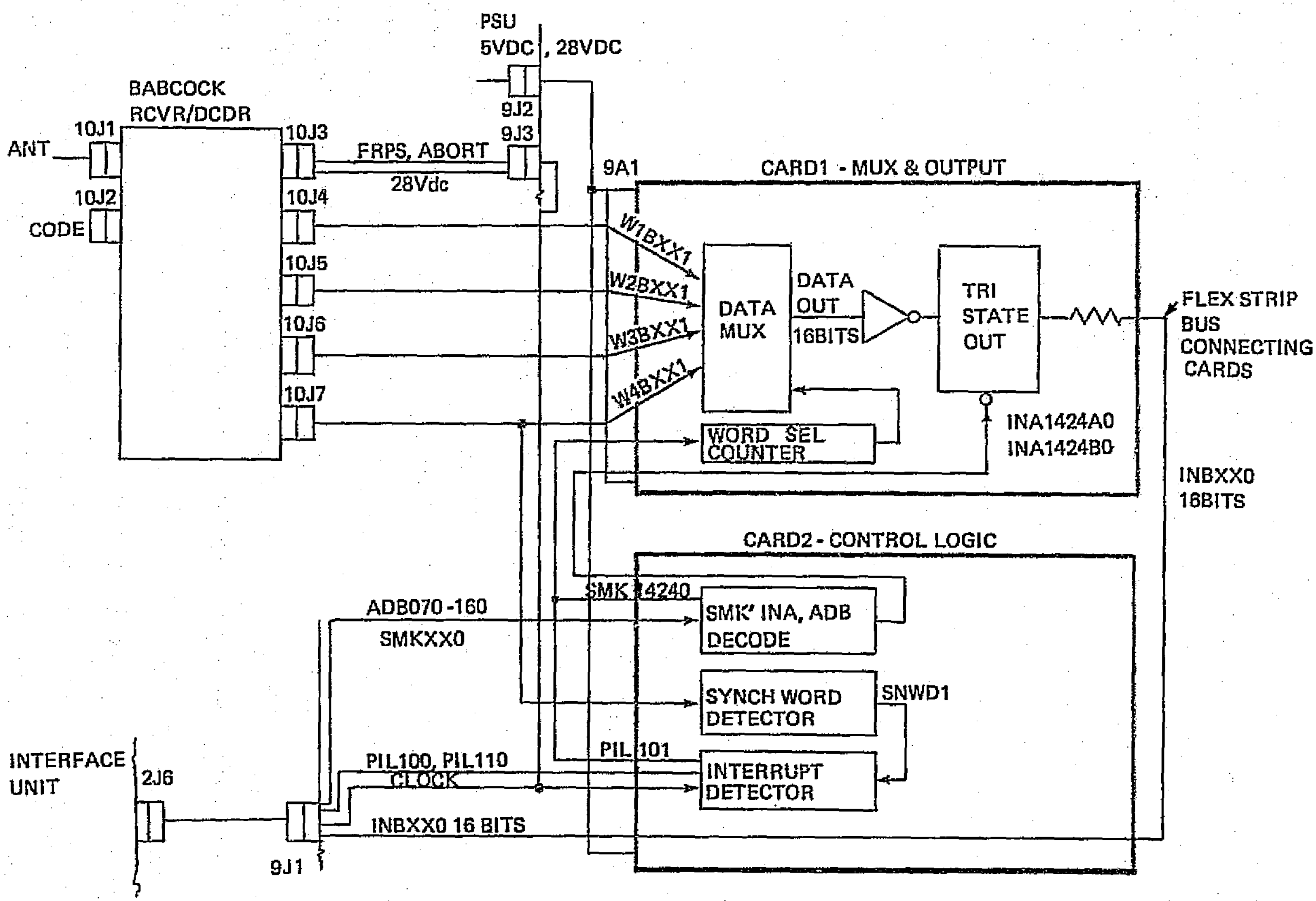
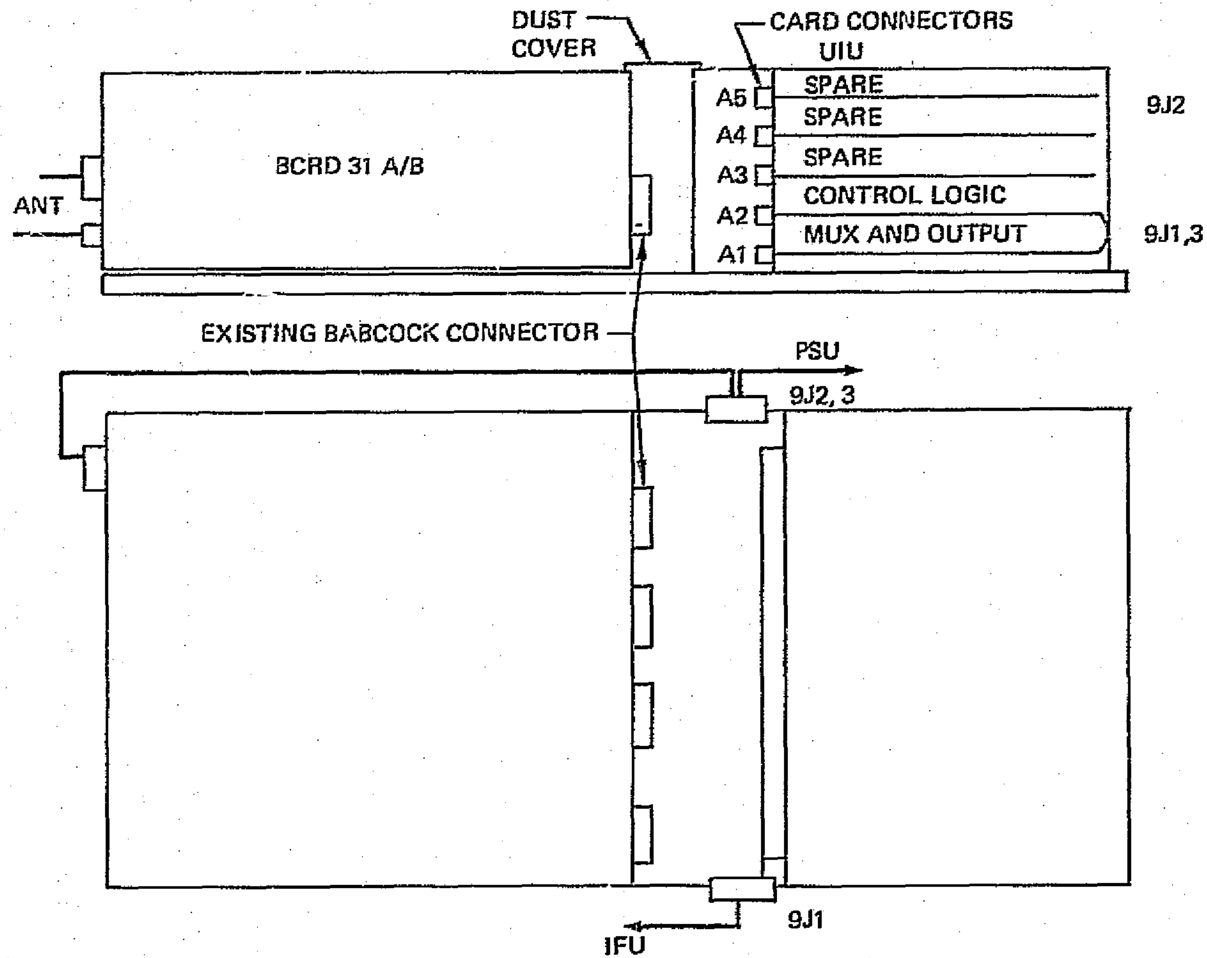


Figure 4.2-3. Uplink Interface Unit (UIU) Block Diagram



UNIT NAME: UPLINK INTERFACE UNIT
UNIT NUMBER= 9, BCRD 31 UNIT NUMBER IS 10
BABCOCK RCVR/DCDR BCRD31 A/B IS COMPATIBLE

Figure 4.2-4. PROFIT Uplink Interface Unit Mechanical Arrangement

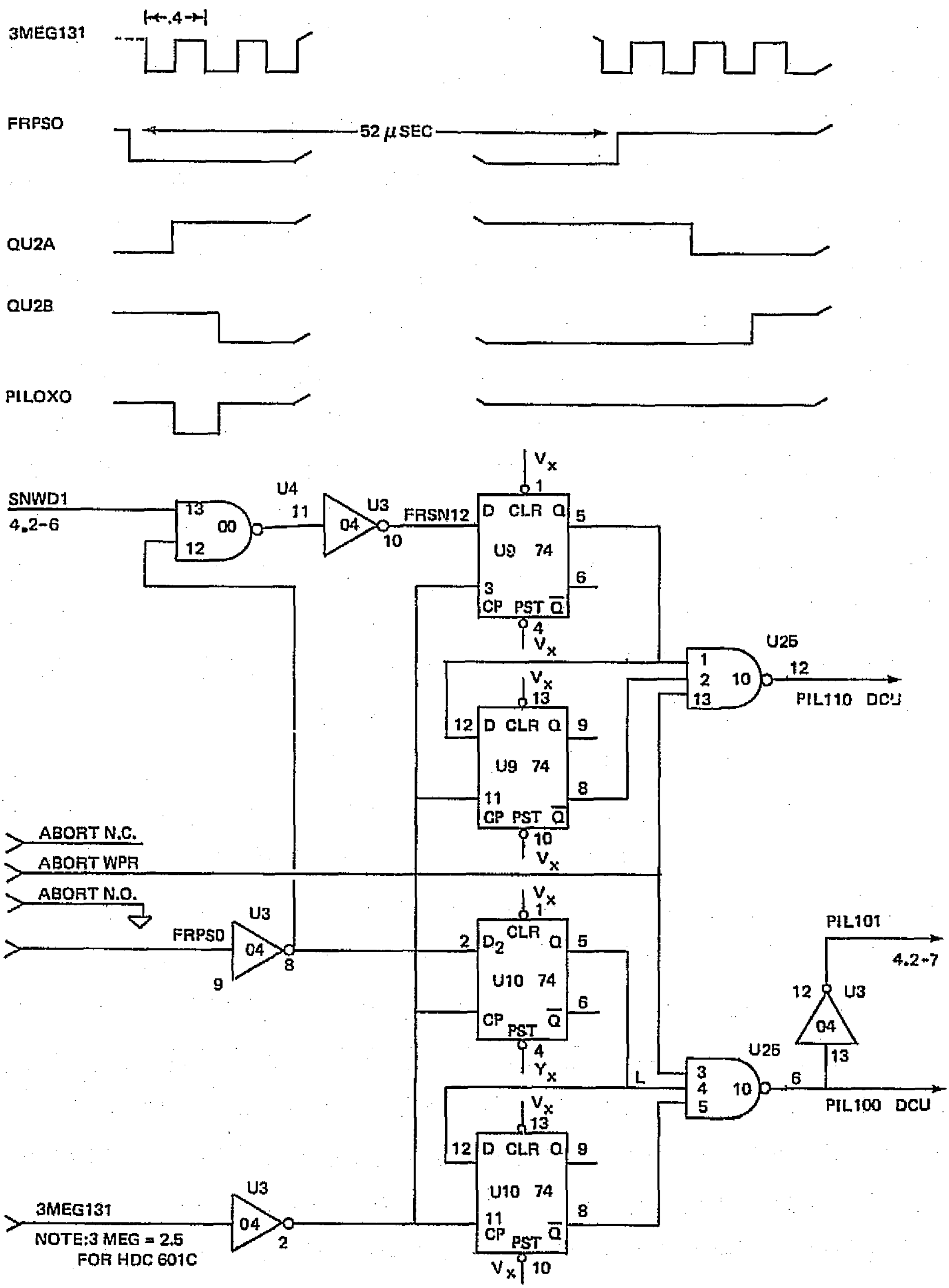
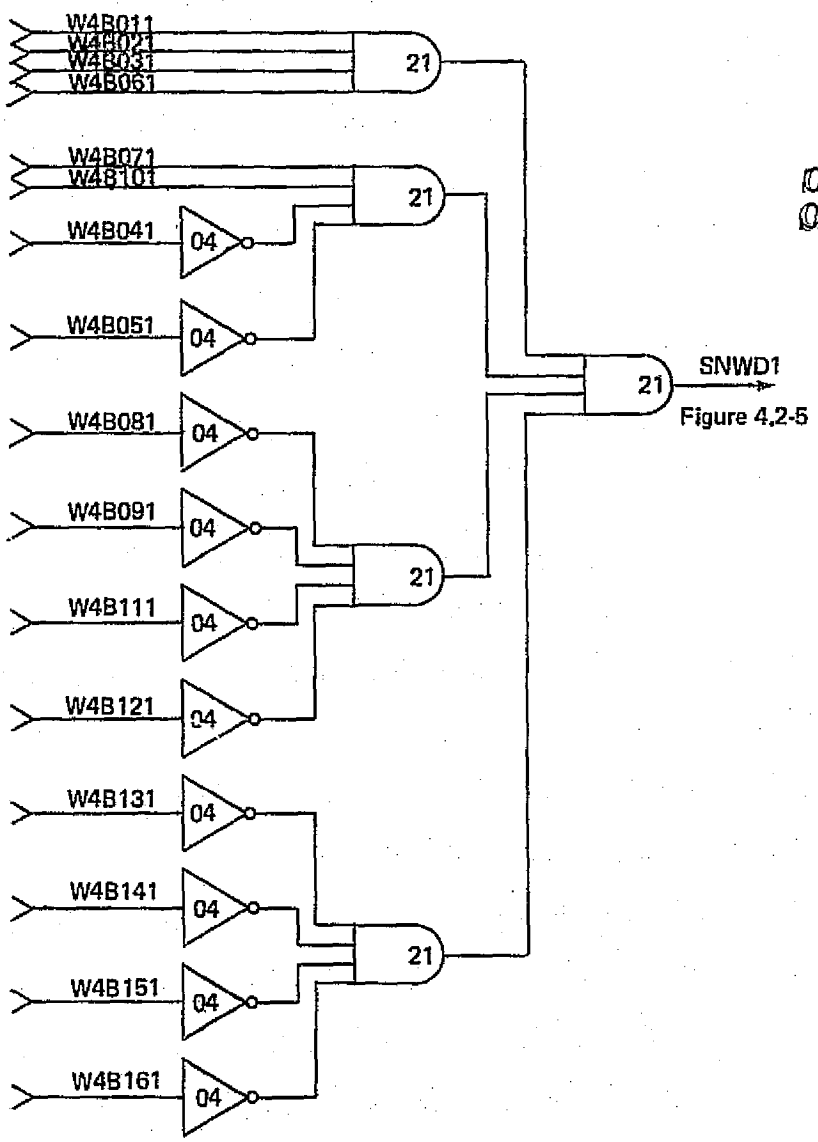


Figure 4.2-5. PROFIT Uplink Interrupt Generator

SYNCH WORD IS

	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0
BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

MSB LSB



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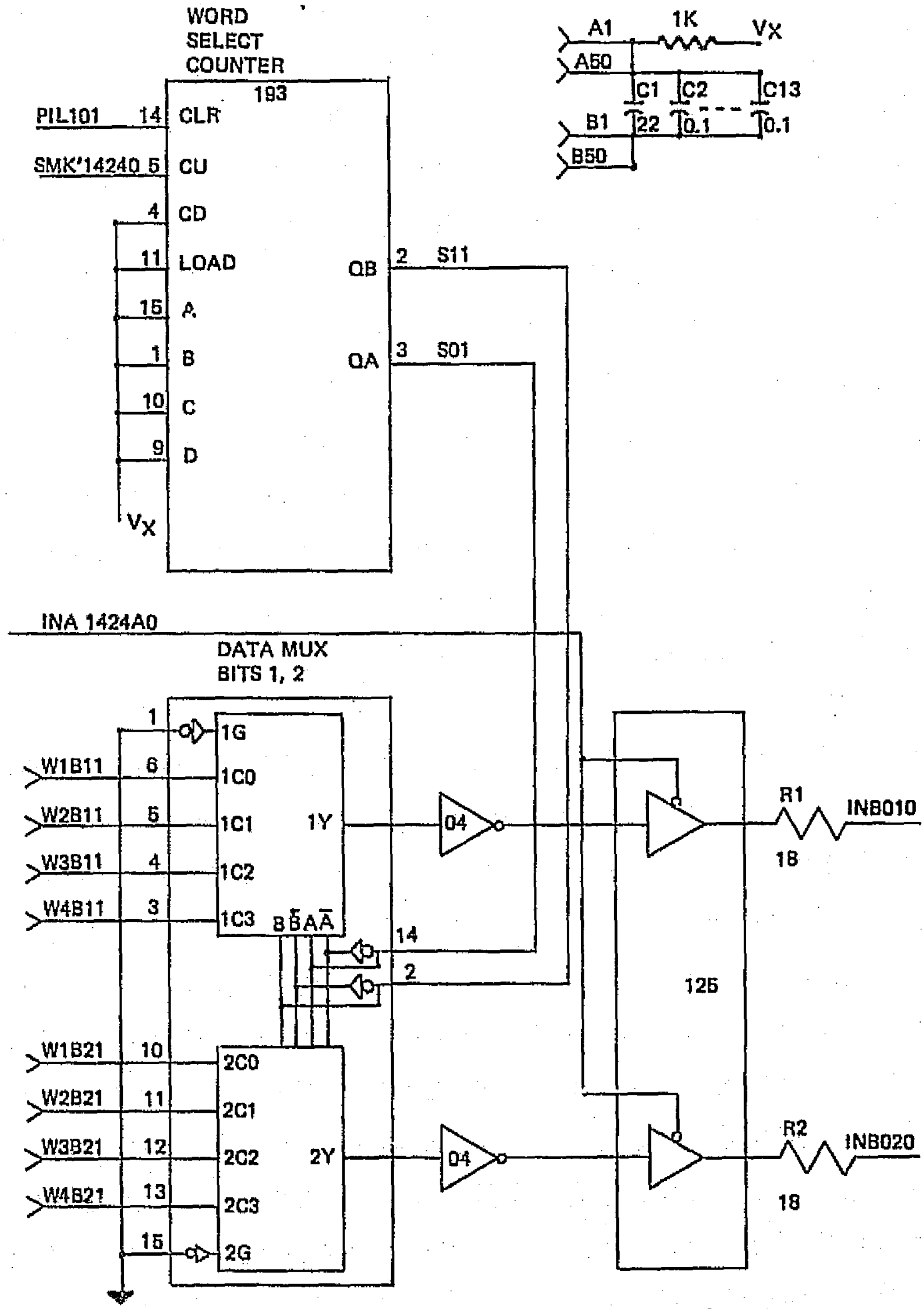
NOMENCLATURE:
W4B161 WORD 4, BIT 16, ACTIVE HIGH

Figure 4.2-6. PROFIT Synch Word Generation



1 MUX CHIP, DATA INVERTER, AND TRI-STATE OUTPUT GATE OF 8 SHOWN. 7 OTHERS ARE IDENTICAL EXCEPT WIRED FOR BIT PAIRS 3,4: 5,6: 7,8: 9,10: 11,12: 13,14: 15,16 USE INA 1424A0 FOR BITS 1-8, INA1424B0 FOR BITS 9-16.

Figure 4.2-7. PROFIT Uplink Word Select and Mux

the 125 buffers. The INA 1424 also generates a hand shake, DRLINØ, see Figure 4.2-8, for the DCU. The software next generates a SMK 1424 which increments the word select counter and the next word of the block is input. This process continues until all four words are input. From a hardware standpoint there is no difference between a 4 word data block containing a frame synch word and one that doesn't. The required 601 processing software is defined in Reference 2.

Although the above design is presented as a baseline, two variations of it are worth considering:

1. Multiplex Packaged in IFU
2. Uplink Interface Output Connected Direct to DCU

Note that the design above contains a number of unnecessary components because in the breadboard setup the IFU was not used, only the DCU, see Figure 4.2-9, and available components were used. The following simplifications are possible. In Figure 4.2-5 only one 5474 is required to generate the two interrupts since PIL110 is simply PIL100 gated by SNWD1. In Figure 4.2-6 a 5404 is eliminated by using a 5425 in place of the 5404/5421 combination. In Figure 4.2-7 the 54153/ 54125 can be replaced by the 54LS253. If a data inversion is accepted, not recommended since it creates a potential error source in software design, the 5404 inverters can be eliminated. In Figure 4.2-8 the address bus decode and DRLINØ function already exists in the IFU 710 card so it too can be eliminated when the IFU is available. By making all these parts reductions the interface part count permits building it on one IFU card. Thus it becomes attractive to place these electronics in the IFU. This however implies running 64 data lines plus returns and shields from the receiver/decoder into the IFU. The most plausible way to do this is to replace the T/M downlink connector, 2J7 (22 pins), with a 100 pin connector to serve both uplink and downlink requirements. The implications of doing this require both a review of IFU assembly detail and other contemplated IFU modifications.

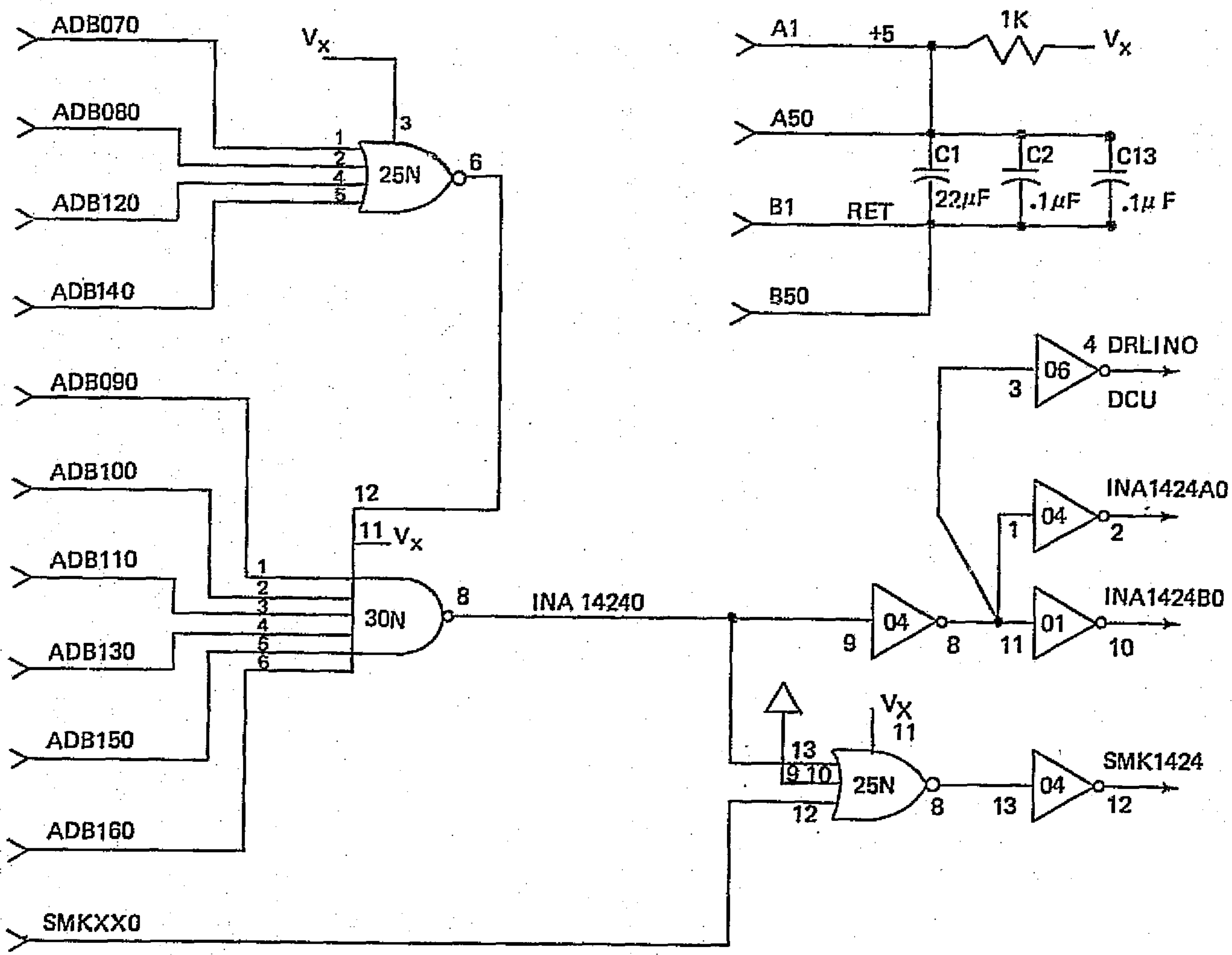


Figure 4.2-8. PROFIT Uplink SMK, INA 1424

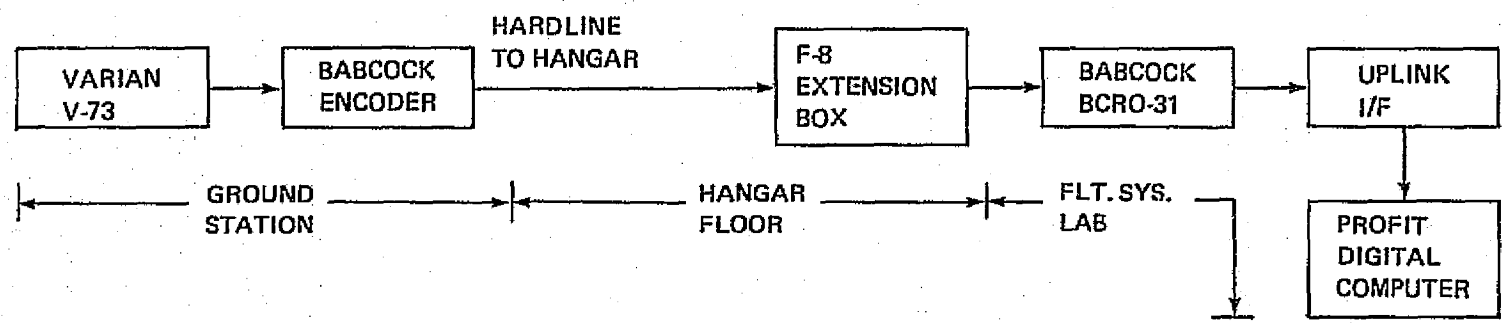


Figure 4.2-9. PROFIT Uplink Test Hardware Elements

Another approach to the problem is to run UIU data output to the DCU GSE connectors, 1J2 and 1J5, and obtain the signals not available there, INA 1424, for example, from the IFU. This would minimize IFU modifications but requires use of a nonconventional (teed) cable to GSE (CCU) if CCU operation is desired with the UIU connected.

A detailed IFU design definition is required to make a final decision in this area.

4.2.3 Uplink Interface Test

The uplink interface was assembled on a breadboard basis and the system was tested on an end to end basis with the equipment indicated in Figure 4.2-9. Varian V-73 and 601 software was developed to transmit three bit patterns over the system, Figure 4.2-10. The intention of these patterns was to generate two patterns which would cause frequent bit transitions. The third pattern generates random patterns which in combination with the software checksum permitted running a long term check for transmission errors. The system ran for four hours without a bit error in ambient lab conditions. No attempt was made to run the system at extreme temperatures although, properly packaged, no problems are anticipated.

4.3 DCU MEMORY EXPANSION

In order to provide adequate core memory for PROFIT applications all four HDC-601 DCU memories must be expanded to 32K 16 bit words (System A). See remarks in Section 5.2 with regard to System B requirements. Two different configurations of computers are available for the PROFIT program. Two were used for IPCS and have 16K of memory installed, and two were used on a Naval Weapons Center (NWC) program and have 8K of memory installed. For simplicity in the following discussion, they are referenced by serial number, NWC machines are S/N 3, 4, IPCS machines are S/N 5, 6.

BABCOCK WORD	DPCU WORD (W)	TEST PATTERN		
		1	2	3
1	1	000001	000030	000060
2	2	052525	111111	w_i = EQ.1
3	3	125252	022222	
4	4	052525	133333	
1	5	125252	044444	
2	6	052525	155555	
3	7	125252	066666	
4	8	052525	177777	
1	9	125252	011111	
2	10	052525	122222	
3	11	125252	033333	
4	12	052525	144444	
1	13	125252	055555	
2	14	052525	166666	
3	15	125252	077777	
4	16	052525	111111	
1	17	125252	022222	
2	18	052525	133333	
3	19	125252	044444	
4	20	052525	155555	
1	21	125252	066666	
2	22	052525	177777	W_{22} = N/21
3	23	$W_{23} = \sum_{1}^{22} W_i$	$W_{23} = \sum_{1}^{22} W_i$	$W_{23} = \sum_{1}^{22} W_i$
4	24	163100	163100	163100

EQ. 1. Compute w_i as follows
- a. Exclusive or '000001 with current w.
- b. Save resulting LSB
- c. Right shift current w 1.
- d. Stuff LSB 1 or 0 from Step b into MSB of of Step c result.
- e. Result of Step d becomes new w.
- f. Iterate

- Initial w is 125252
- N is a counter incremented on every iteration.
- W23 is checksum of 22 DATA words in all three patterns.

Figure 4.2-10 PROFIT Uplink Test Patterns

4.3.1 DCU Memory Expansion Requirements

The requirement is to expand all four machines to 32K words without violating their flight qualified status.

4.3.2 DCU Memory Expansion Design

The design work to meet the requirement of 4.3.1 was mostly done by Honeywell in the basic HDC-601 design. A connector is provided for a second memory module and the wire lists for the 32K machine are in the Honeywell Operations and Maintenance Manual, Reference 16.

The modification is a two step process. First the S/N 3, 4 machines are upgraded to S/N 5, 6 configuration by reworking cards and adding wires, see Table 4.3-1.

The 8K memory modules are replaced by 16K memory modules. All four computers are then upgraded to 32K by implementing FRC Work Order Numbers 33-1-305, 33-1-385. These add a second 16K memory, adapt the DCU end plate to attach the memory module, see Figure 4.3-1, add memory bus wiring, and modify the A12 interrupt card to accommodate two memories. An external power supply is required to power the second memory module. This is installed mechanically as shown in Figure 4.1-6, 7 and electrically as shown in Figure 4.3-2. Alternative approaches to this power supply arrangement may be considered during procurement of the modifications. The alternatives in general involve either building a new power supply capable of handling the full 32K load and/or using a more densely packaged memory module to eliminate some of the difficulties associated with two separate memory modules.

4.3.3 Memory Expansion Test

As an interim test to demonstrate the wiring and logic changes required for the 32K memory computer configuration a 24K machine was assembled by implementing the 32K logic and wiring changes on S/N 5 - DFRC Work Order numbers

CARD SLOT	DCU S/N 3 CARDS	DCU S/N4 CARDS	DCU S/N 5 (V-1) CARDS	DCU S/N 6(V-2) CARDS
A1	467-001 Rev H	467-001 Rev H	467-001 Rev H	
A2	469-001 Rev E	469-001 Rev E	709-001 Rev A	1 Should be same as S/N5 but physical inspection not made to date
A3	471-001 Rev G	471-001 Rev G	471-001 Rev G	
A4	473-001 Rev F	473-001 Rev F	473-001 Rev F	
A5	475-001 Rev G	475-001 Rev G	475-001 Rev G	
A6	477-001 Rev G	477-001 Rev G	477-001 Rev G	
A7	479-001 Rev E	479-001 Rev F	479-001 Rev F	1
A8	481-001 Rev E	481-001 Rev E	481-001 Rev E	
A9	483-001 Rev E	483-001 Rev E	483-001 Rev E	
A10	485-001 Rev E	485-001 Rev E	485-991 Rev E	
A11	487-002 Rev K	487-002 Rev L	487-002 Rev L	1
A12	489-002 Rev H	489-001 Rev J	20195-001 Rev A	1 2
A13	491-001 Rev F	491-001 Rev F	491-001 Rev F	
A14	Empty	Empty	Empty	
A15	Empty	Empty	Empty	
A16	Empty	Empty	Empty	
A17	Empty	Empty	Empty	
A18	Empty	Empty	Empty	

NOTE: Part numbers are abbreviated to last three digits for convenience.

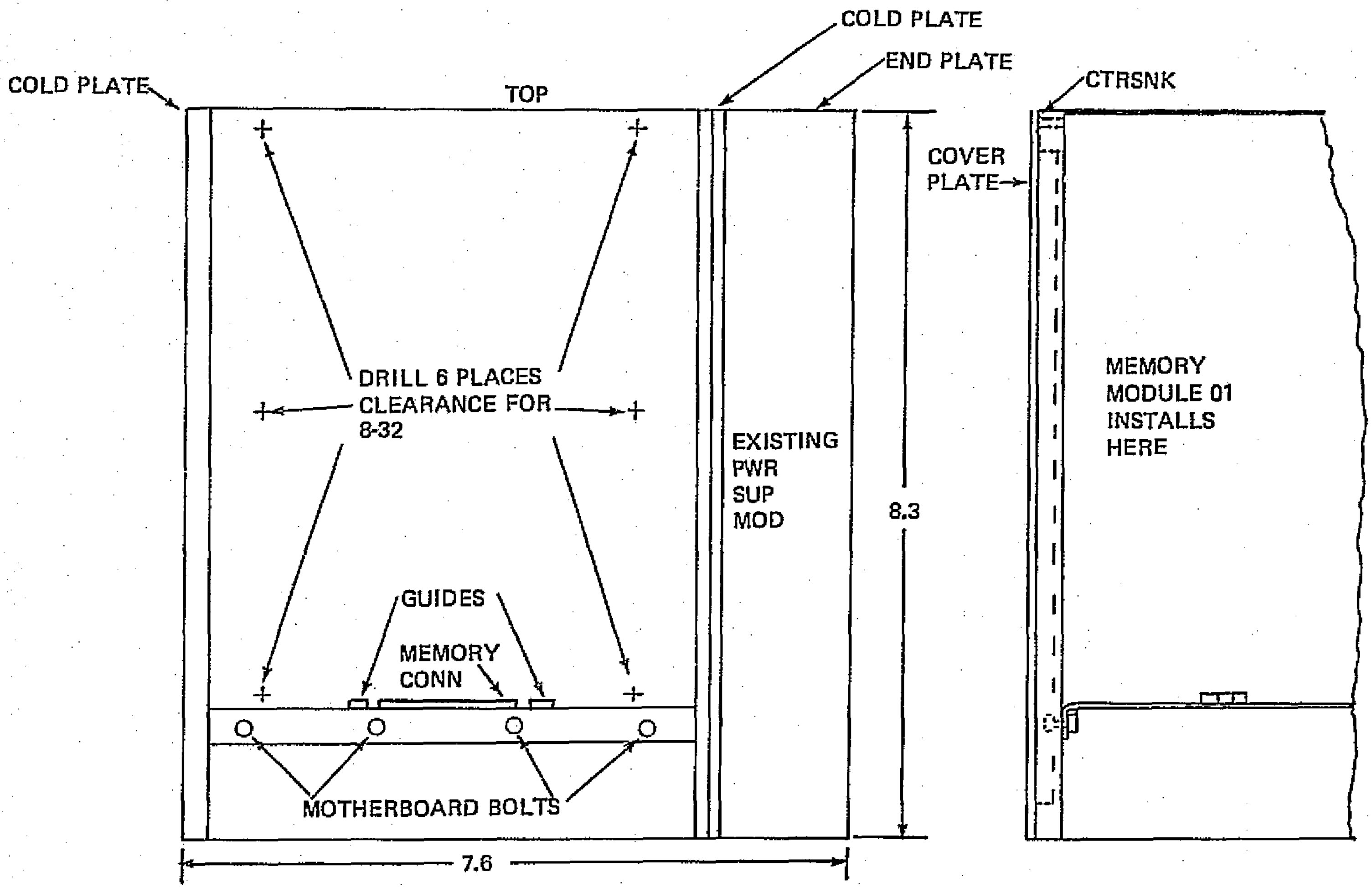
1 S/N3, S/N4 require update to S/N5 configuration. Revision letter difference implies added wire. Part number change implies board rework required.

2 A12, Interrupt Logic Card, is further updated by DFRC FSL W.O. #33-1-385, dated 5/11/77

Motherboard wire wrap changes are as follows:

1. Update S/N 3,4 to wirelist in Honeywell operations and maintenance manual for DBG-82339 B1 from that in DBG 82339A1 manual.
2. Implement FS-B-437 on S/N 3, 4, 5, 6 DCU's

DCU MODIFICATION REQUIREMENTS
TABLE 4.3-1



NOTE: SKETCH FOR FUNCTIONAL
REF ONLY

Figure 4.3-1. Memory Installation

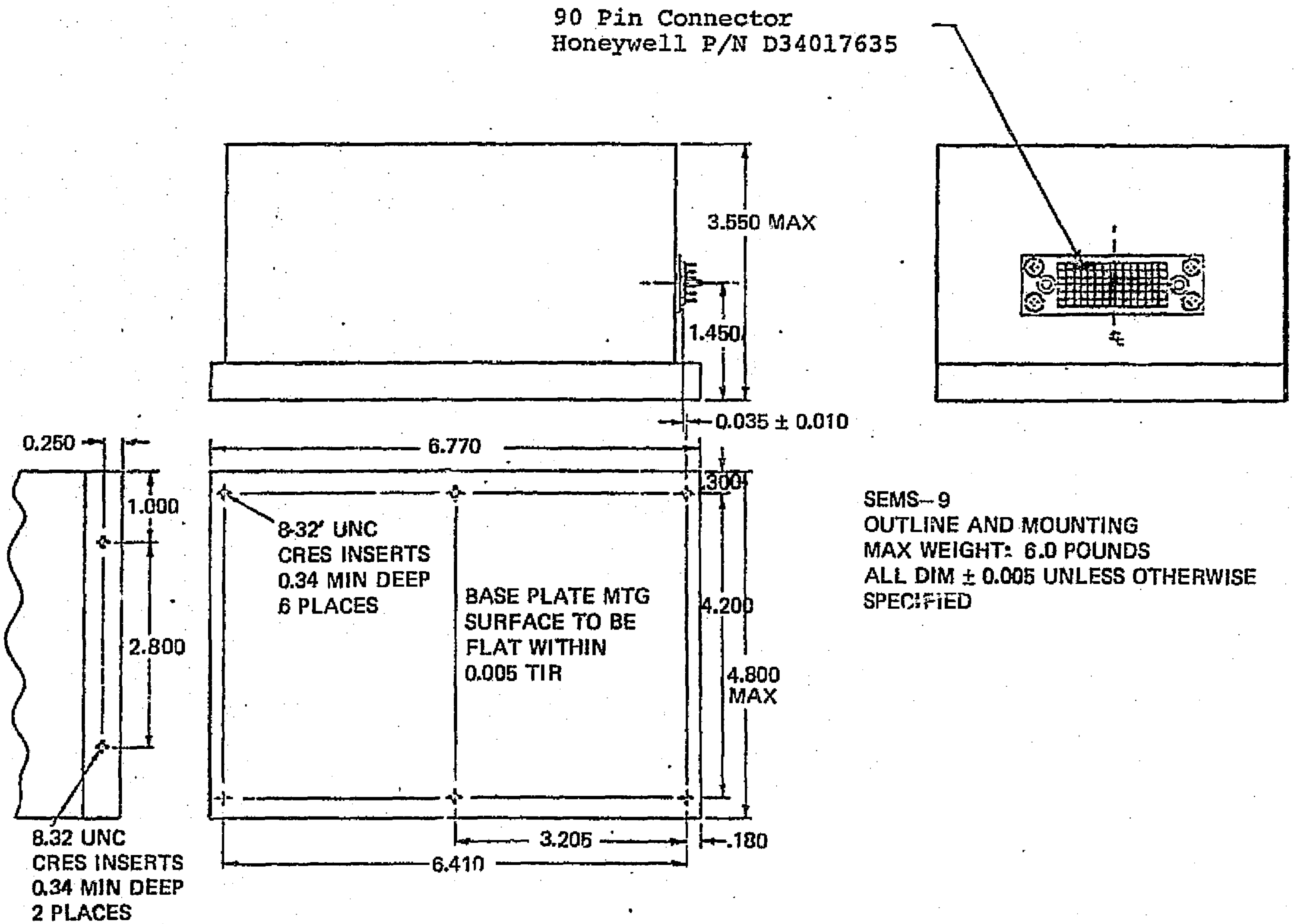


Figure 4.3-1. (cont.)

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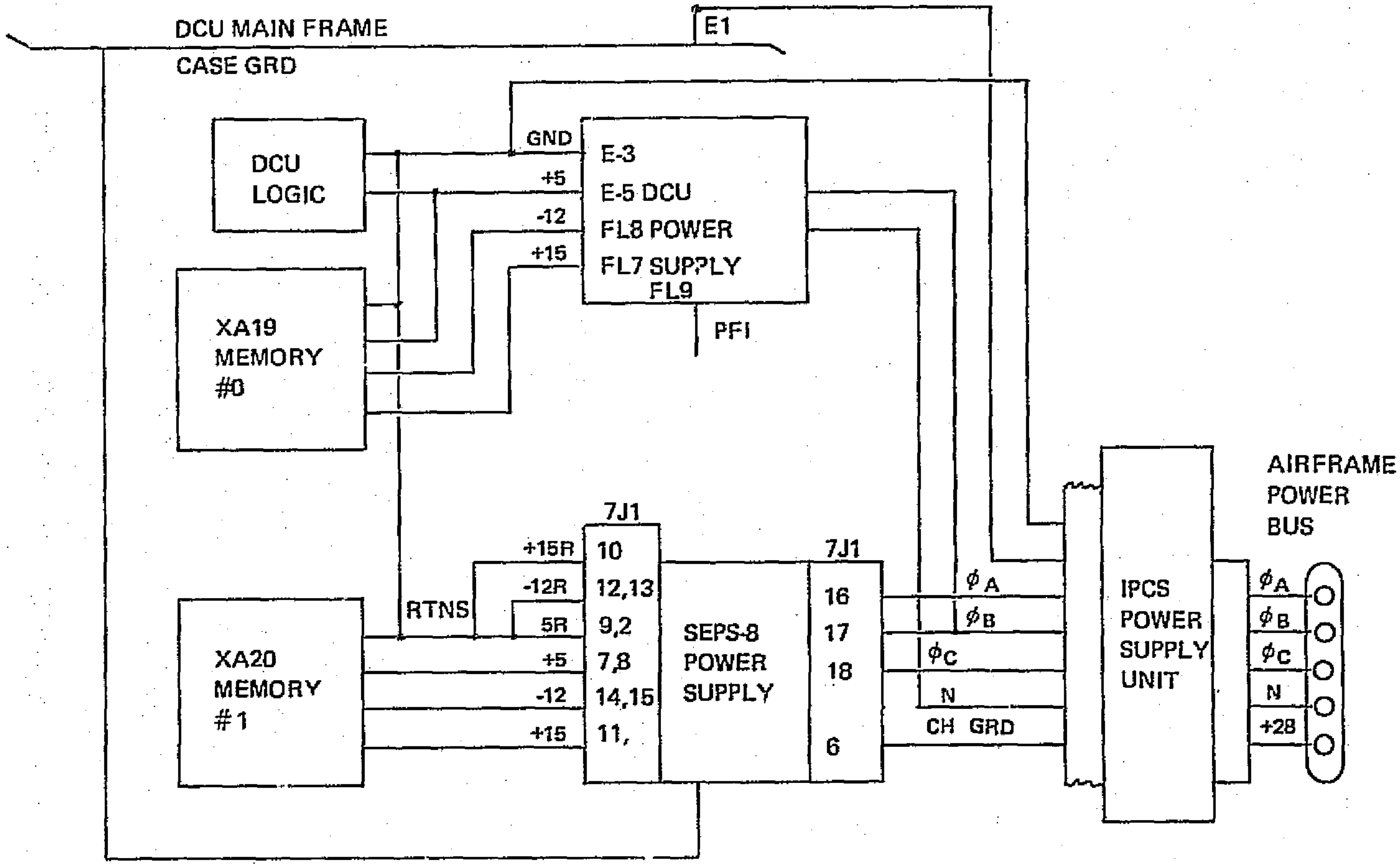

Figure 4.3-2. DCU Power Distribution

33-1-305 and 33-1-385 and installing the 8K word memory module from DCU S/N 3 in DCU S/N 5. Power for the added memory module was obtained by wiring the DCU S/N 3 power buses to the DCU S/N 5 XA20 connector. The resulting system configuration is shown in Figure 4.3-3.

Testing of this configuration led to a number of results.

The data bus noise level of this configuration is higher than the single memory module configuration. Most of this noise is the result of switching loads on the negative memory supply. Various grounding configurations were tried to resolve this and the one that seemed best is shown in Figure 4.3-3. The primary test tool was the memory verification program DQG813741. This loads and verifies various bit patterns into the memory. Intermittent errors were encountered in the extended memory module. After changing grounds, looking for glitches, etc. the 8K memory module from DCU S/N 4 was used to replace the one from S/N 3. This unit successfully passed the test consistently. The two units are different part numbers and may have significantly different I/O circuitry and power supply bypassing. This activity demonstrated the validity of the basic logic implemented but indicates the existence of a potential noise problem. When the system was tested at room temperature in the proposed flight configuration using the SEPS-8 power supply and SEMS-9 memory, it passed all tests successfully.

A peculiarity of the loader--it won't work--was encountered when operating in extended mode. The problem was corrected by inserting a patch in location 17 of the bootstrap which moved the OCP 101 to location 300 and returned.

The power supply interrupt was checked in extended mode by verifying that loss of power to either memory would result in a power supply failure interrupt and that program execution--power on interrupt--did not occur until both memories were on. It was noted during this testing that the standard power supply interrupt test which uses a time out to verify that the DCU power supply remains on for a substantial length of time after prime power

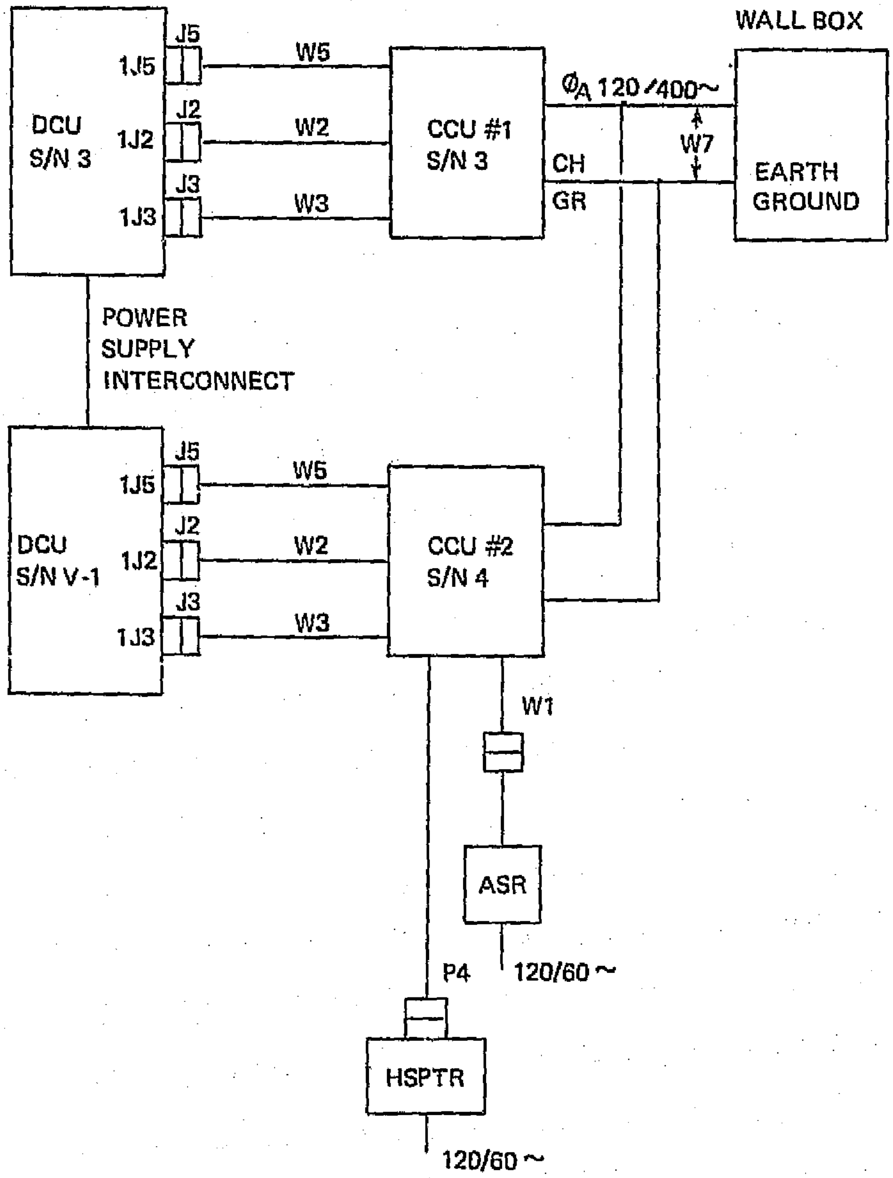

Figure 4.3-3. Test Arrangement for Extended Memory Breadboard - 24K

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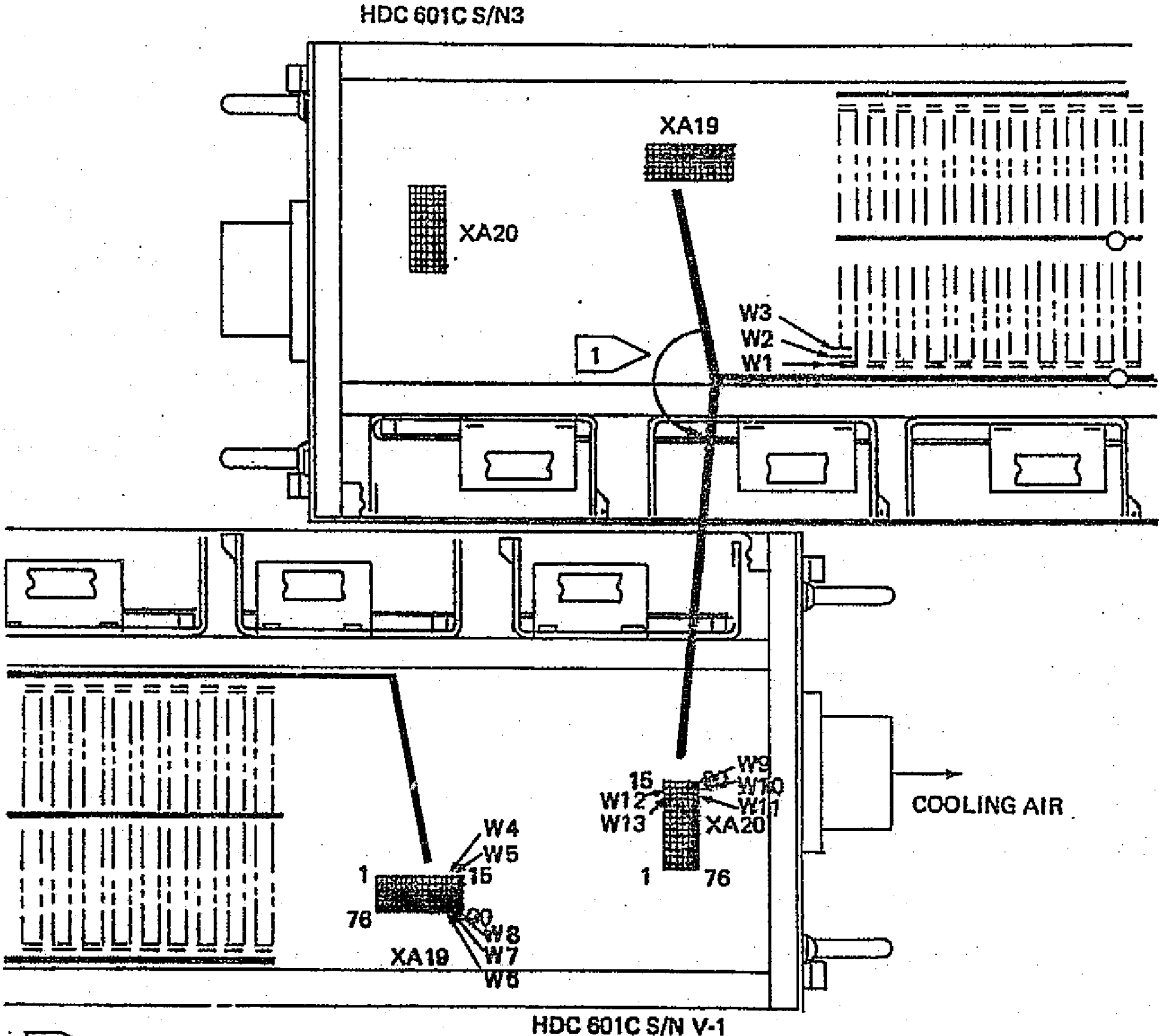

1 S/N 3 W4, 5, 6, 7, 8 BECOME
S/N V-1 W13, 12, 11, 9, 10
EXISTING S/N 3 WIRES REACH IN CONFIGURATION SHOWN.

NOTE: CONNECT S/N 3 E-3 TO S/N V-1 E-3 TO PROVIDE COMMON GROUND. CHASSIS GROUNDS ARE RETURNED TO EARTH THROUGH CCU'S

Figure 4.3-3 (Cont) Test Arrangement for Extended Memory Breadboard—24 K

failure, expects the DCU to stay on longer than it actually does. The reason for this was not determined. However, the S/N 6 unit at LeRC performs the same way. This leads to the conclusion that the test software may have been designed around the decay characteristics of the 8K DCU and never corrected for the changes related to the 16K memory module since the error is small, 10% of specified time.

One failure of a feedthrough bypass capacitor, shorted the +5 power supply of DCU S/N5 to chassis ground. The problem was found during polarity and isolation tests related to testing the S/N 3 and S/N 5 DCU's together. No cause for the failure is known and no identifiable circuit damage resulted.

4.4 CENTRAL COMPUTER BUS INTERFACE

The BØM F-15 utilizes redundant serial digital data busses to provide communication between avionics elements and the airplane central computer. The production system is shown in Figure 4.4-1. The PROFIT test airplane lacks most of the standard peripherals and the central computer. The central computer is replaced by a central computer simulator which interrogates the bus causing the peripherals to transmit data. The bus is currently monitored by the F-15 data system. For the PROFIT application the DPCU is also provided with the capability to monitor the bus to select a variety of information from it.

The following paragraphs define bus interface requirements and describe a system which has been assembled to interface the DPCU to the central computer bus.

4.4.1 Central Computer Bus Interface Requirements

The bus interface is specified by McAir Specification H009 (Ref. 17). Bus data are defined in the Central Computer T.O. (Ref. 18) and in the Central Computer Data Base Catalog. The data menu of Table 2.5-1 is representative

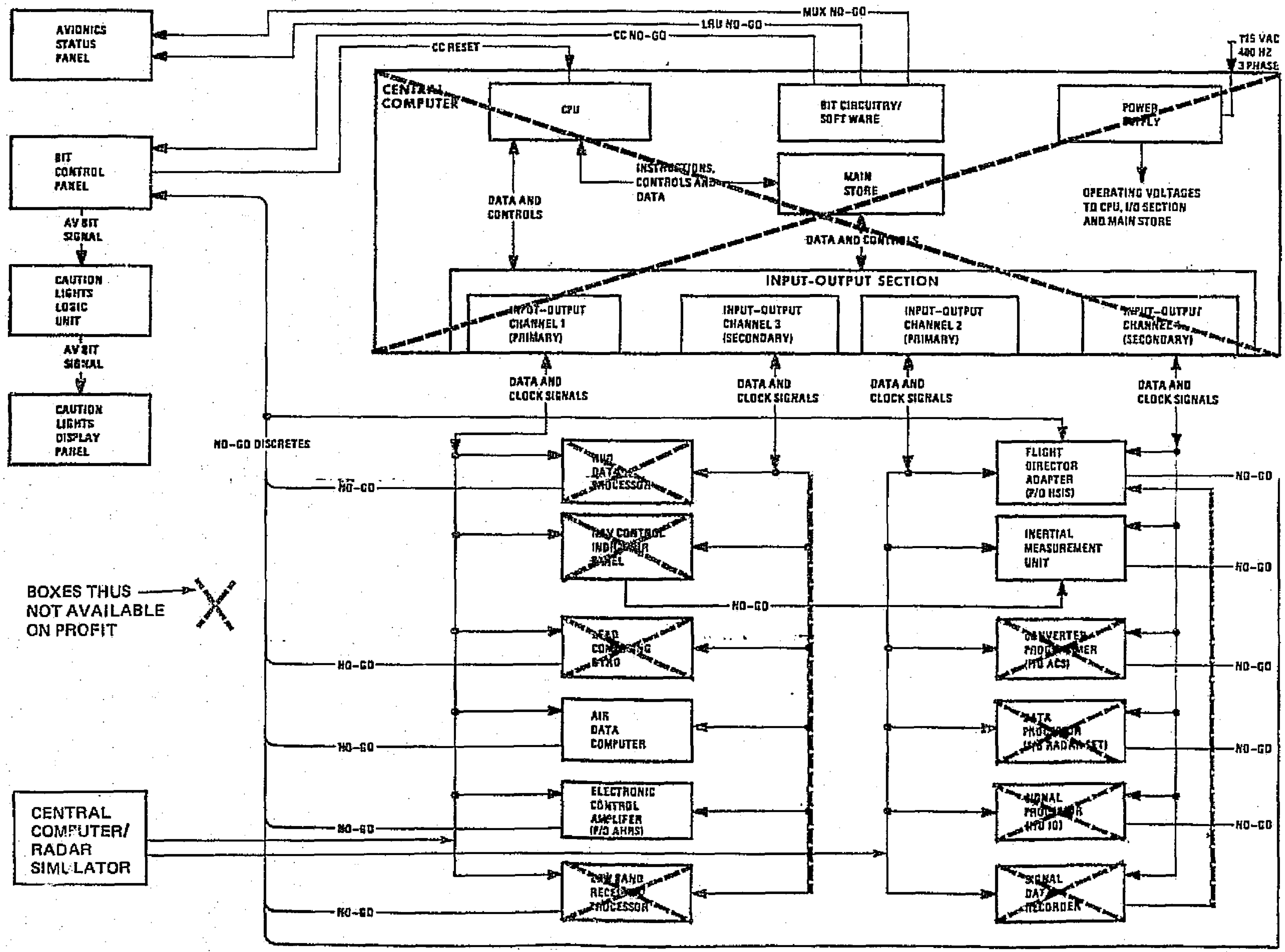

Figure 4.4-1. Central Computer System Block Diagram

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of that available from the peripherals currently in the PROFIT airplane. The following paragraphs define the bus interface using MIL-1553A as a point of reference.

Modulation/Encoding--The multiplex bus consists of two twisted pair transmission lines, one data and the other clock (1 MHz). Data is bi-phase level modulation at 1 MHz. A five bit gap is provided between data words and a minimum 8 bit gap is provided between data and a following select word for message sync. Table 4.4-1 defines various bus operating parameters.

Transmission Line--The cable type is twisted shielded pair (TSP) with characteristic impedance in the range of 70 ohms ±10%. The attenuation and capacitance are not specified but are comparable to MIL-STD-1553A. The maximum length of 300 ft. for the main bus is consistent with those specs based on MIL-STD-1553A. H009 does not define a limit on line length. It is estimated that there is a limit of approximately 75 feet. The F-15 avionics system employs two separate busses with six (6) subsystems attached to each bus.

Cable Termination Coupling and Grounding--Peripherals are transformer coupled to the bus. H009 assumes that the connections are "daisy chain." No isolation (fault protection) resistors are required by the specification. It is specified that the transmission line be terminated in a balanced to ground configuration and that shields are grounded at each terminal. The clock line is specified to the same requirements as the data line.

Word Format--Unlike MIL-STD-1553, bus synchronization is automatically available through the clock. Control (select) words are identified by a lack of data for more than 8 clock times. Data words are separated by 5 clock times.

TABLE 4.4-1

F-15 CENTRAL COMPUTER BUS OPERATING PARAMETERS

SPECIFIED OUTPUT SIGNAL LEVEL/LOADING

Output (Volts, Peak Line-Line)	Load (ohms)	Transmitter Impedance	Measuring Point	Network Condition
± 4 to ± 6	175	68	RT Term	Daisy Chain
± 4 to ± 6	$R_S = 19$ $X_C = 80$ @ 1 MHz	68	RT Term	Daisy Chain

SPECIFIED OUTPUT SIGNAL WAVEFORMS

Time Stability (ns)	Amp. Distortion (V. P-P)	Rise and Fall Times (ns)	Load Condition	Output Noise (MV. PP)
Clock/Data (Phased within 35 ns)	N/S	Clock-Sinewave Data-Smoothed	175 ohms	N/S

TERMINAL INPUT CHARACTERISTICS

Waveform	Signal Level (V.P. L-L)	Common Mode	Input Impedance (Ohms)
Smoothed	± 1 to ± 7	N/S	10,000 (Freq. Not Specified)

Data word format is specified in T.O. IF-15A-2-16-2 for each word from each peripheral. Data words are comprised either of flag bits or are fixed point 16 bit numerical data, an extended word capability is available. Data are true binary two's complement.

Select words are initiated by the Central Computer Complex (CCC) to control peripheral devices and initiate data exchanges. The select word format depicted in Figure 4.4-2 is discussed in the following paragraphs.

All data transmitted over multiplex buses interfacing with the CCC are transmitted as standard messages. A standard message is composed of a "Select" word originating in the CCC and one or more (15 maximum) "Data" words transmitted to or from a single peripheral. All select words and data words are composed of 17 bits: 16 bits of information (bits 1 through 16) plus a 17th (bit 17) bit providing odd "ones" parity. Note that McAir nomenclature is bits 0-16 which we have restated to be consistent with DCU nomenclature bits 1-17.

The content and detail format of all messages, select words, and data words are specified in the input/output digital data table for the related peripherals.

Select Words--Select words are used to initiate all data exchanges (messages) and originate only in the CCC. A select word provides one of three functions; request data transmission from a peripheral, command a peripheral to take some action other than to transmit data, or identify data to be transmitted from the CCC to a peripheral. A select word is composed of three separate fields; a four bit equipment address field (bits 1 through 4), a single bit command indicator (bit 5), a six bit control field (bits 6 through 11), a single bit T/R indicator (bit 12), and a four bit word count field (bits 13 through 16). The 17th bit (bit 17) provides odd "ones" parity. The equipment address field contains a unique code identifying the unit on the bus to which the communications are being directed. The command indicator

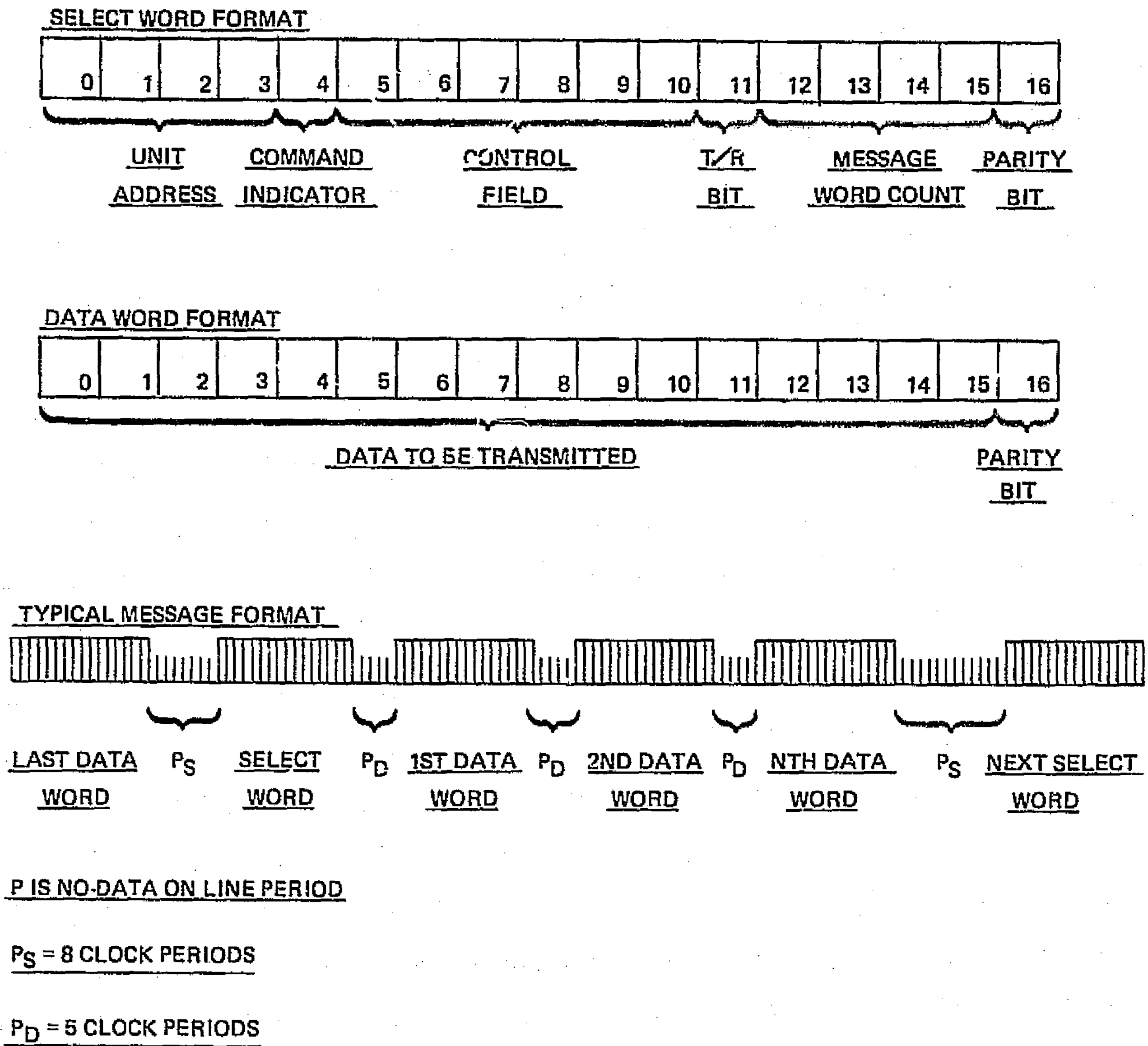

Figure 4.4-2. Central Computer Bus Message Format

identifies whether it is a command or data message. The control field identifies the data to be transmitted by the CCC or by a peripheral following the select word, or for a command message, the command which causes the peripheral to take some action other than transmit data. The command indicator (bit 5 in the select word) is a logical "one" if the select word is a command which requires no specific data from a peripheral except to acknowledge receipt of the command. Bit 12 in the select word is a transmit/receive (T/R) indicator with a logical "one" indicating the peripheral must transmit the data word(s), or a logical "zero" indicating the computer will transmit the data word(s). The word count field specifies the number of data words to follow the select word by a four bit binary number (LSB = bit 16) in bits 13 through 16. If the select word is a command the T/R bit shall be a logical "one" and the word count equals one.

Select words are always preceded by a no-data period (no signals on the data transmission line) equal to or greater than 8 periods of the reference clock signal. This no-data period identifies the word following as a select word and the start of a message. Bit 1 is transmitted first and parity (bit 17) transmitted last.

The control field, at least for the receive mode and the select words defined in Table 2.5-1, simply is a data block pointer and does not normally exceed binary 4.

The output side of the central computer interface (CCIF) mates with the existing DPCU DMA system. Its characteristics are described in the following paragraphs.

DMA System Description

The IFU side of the DMA system is shown in Figure 4.4-3. The DCU DMA hardware upon receiving a read or write request from the device connected to the channel will cause the processor to pause and relinquish the next

C-3

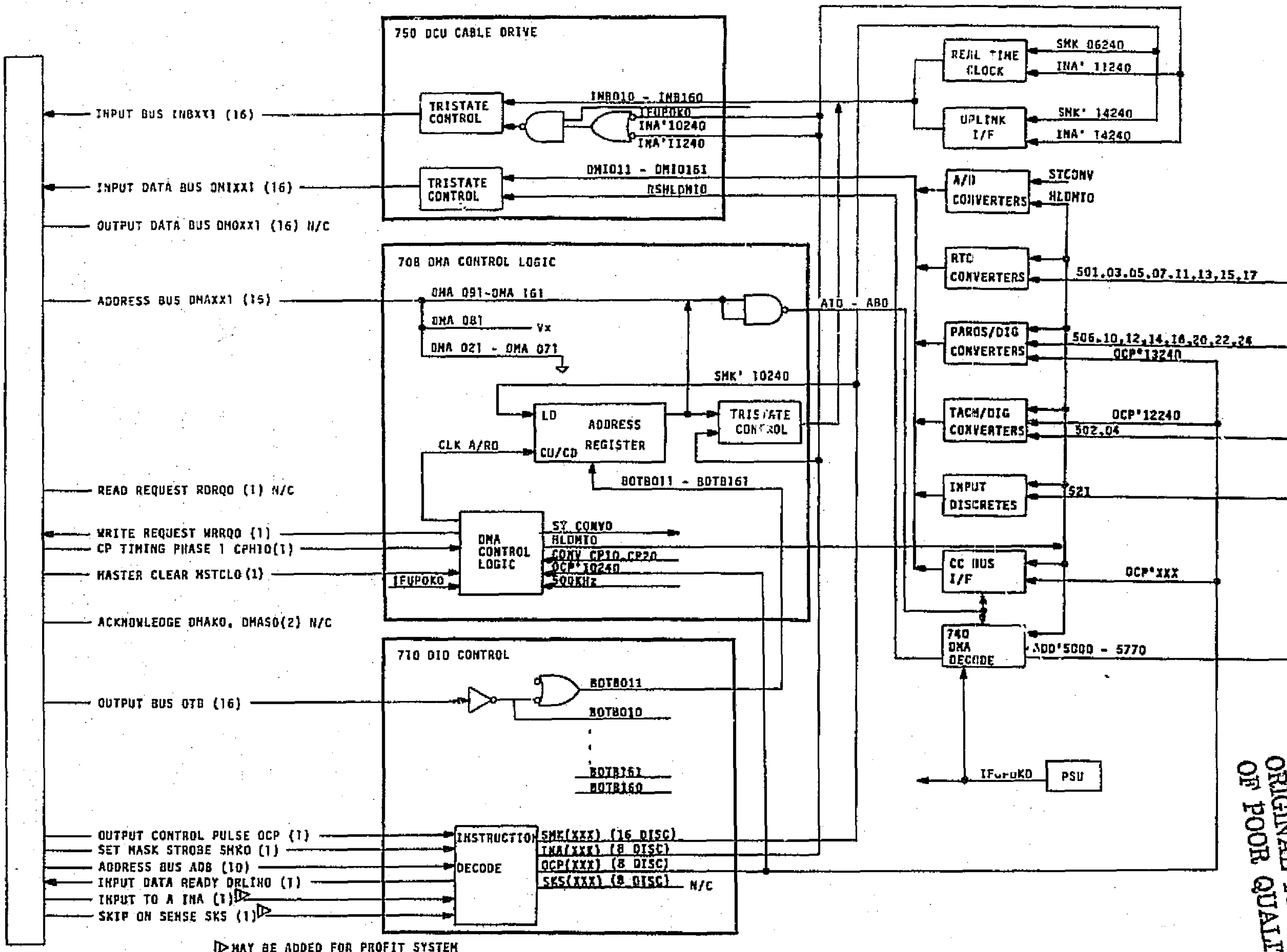

Figure 4.4-3. Computer Interface Functional Diagram

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memory cycle. Under maximum demand conditions, the DMA channel will retain control of the memory and transfer data at a rate of 800,000 words per second. The IFU, see timing diagram Figure 4.4-4, is set up to use only every other DMA opportunity thus eliminating the potential lockup condition. Since the IFU at most only transfers 256 words, including the proposed CC data, every 30 msec, the worst case effect an iteration rate, .31 msec out of 30, is negligible.

System Operation

In normal operation the DMA system operates as follows. The DCU A register is loaded with a word including starting address and range data. This is transferred via the output bus (OTB) by an SMK 1024 (DMA) instruction to the IFU DMA address register on the 708 card. Next the IFU DMA system is started by an OCP 1024. The IFU system automatically down counts the range counter and sequences the address held in the IFU DMA address register. The address lines run both to the A/D converter and to the DMA Decode card. The A/D converter uses addresses '400 - '477. Digital/digital converters, resolvers, etc., are controlled by discretes decoded on the DMA Decode card, addresses 500-577. The highest in use is 524.

Once started the DMA system sequentially presents the desired data to the DCU and asks for memory access when appropriate, using the WRRQ line. Left to itself the DMA will automatically complete the range requested and stop. It is also possible by monitoring the address register through the INA 1024 instruction to hold software processing until the DMA is finished or interrupt and restart DMA processing.

Based on the above definition of the two interfaces which must be mated the following functional requirements for the central computer bus interface are stated.

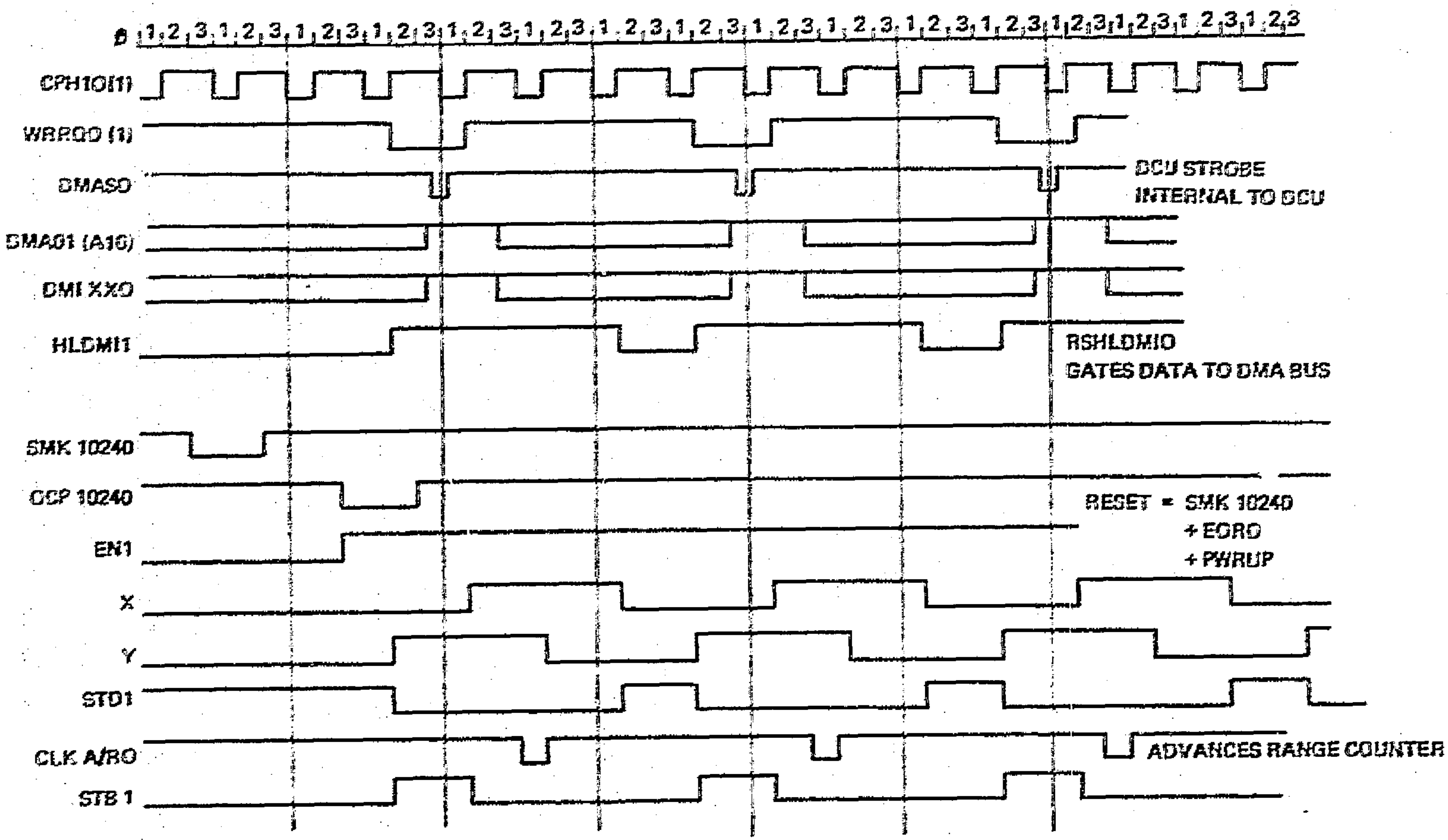

Figure 4.4-4. DMA Timing

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1. The unit shall monitor the central computer bus continually and based on information contained in the select words transfer desired data on a word by word basis to a data buffer.

2. The data word select array shall be reprogrammable.

3. All or portions of the data buffer shall be transferred to the DCU memory via the DMA system and logic existing in the IFU.

4.4.2 Central Computer Bus Interface Design

As shown in Figure 4.4-5 the Central Computer Interface is made up of a serial to parallel converter module, a control and select logic module to identify desired data and a data buffer module which stores the last sample of desired data in designated locations for asynchronous access by the DMA system.

The serial to parallel converter/bus protocol module is available from IBM as P/N 6200-920-2. This unit is actually a transmit/receiver page out of the central computer, which IBM builds, used by Dynamic Controls Corporation in assembling the Stores Management Set. One of these units has been acquired by DFRC and is currently being employed on F-15 #8. Block diagrams and interface data for the unit are shown in Figure 4.4-6. Table 4.4-2 defines unit nomenclature and signals and Table 4.4-3 defines power requirements.

This unit is currently recommended for the PROFIT program because it is a qualified element of the production F15 and is available as a module from government stores. A more modern unit if available on a production basis would be desirable to reduce packaging and power supply requirements. A change in module will not significantly change the interface signal characteristics since they are established primarily by bus protocol.

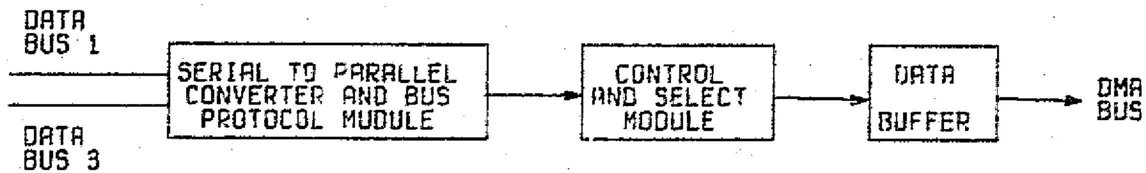

Figure 4.4-5. Central Computer Interface Block Diagram

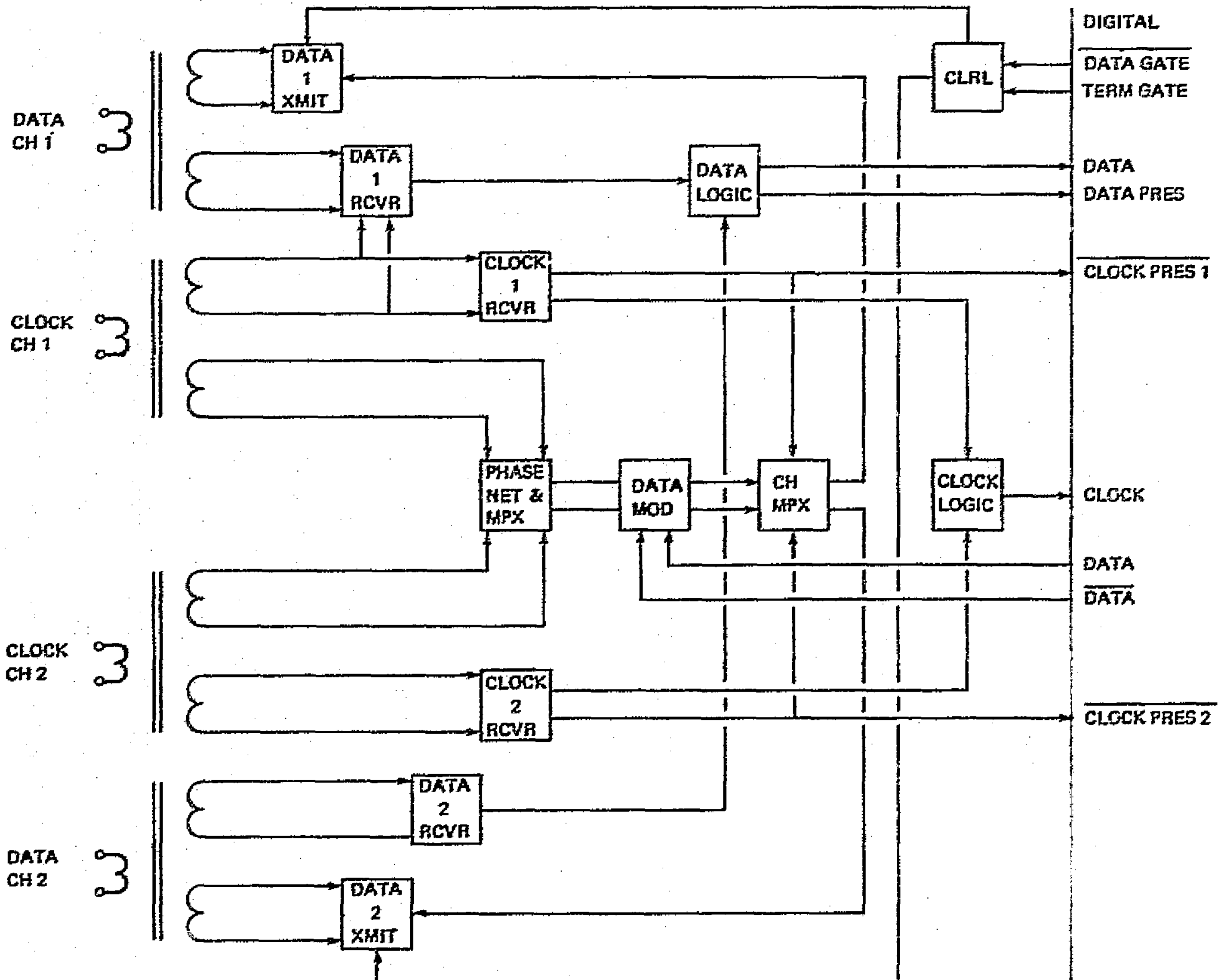

Figure 4.4-6a. Serial Converter Analog Block Diagram

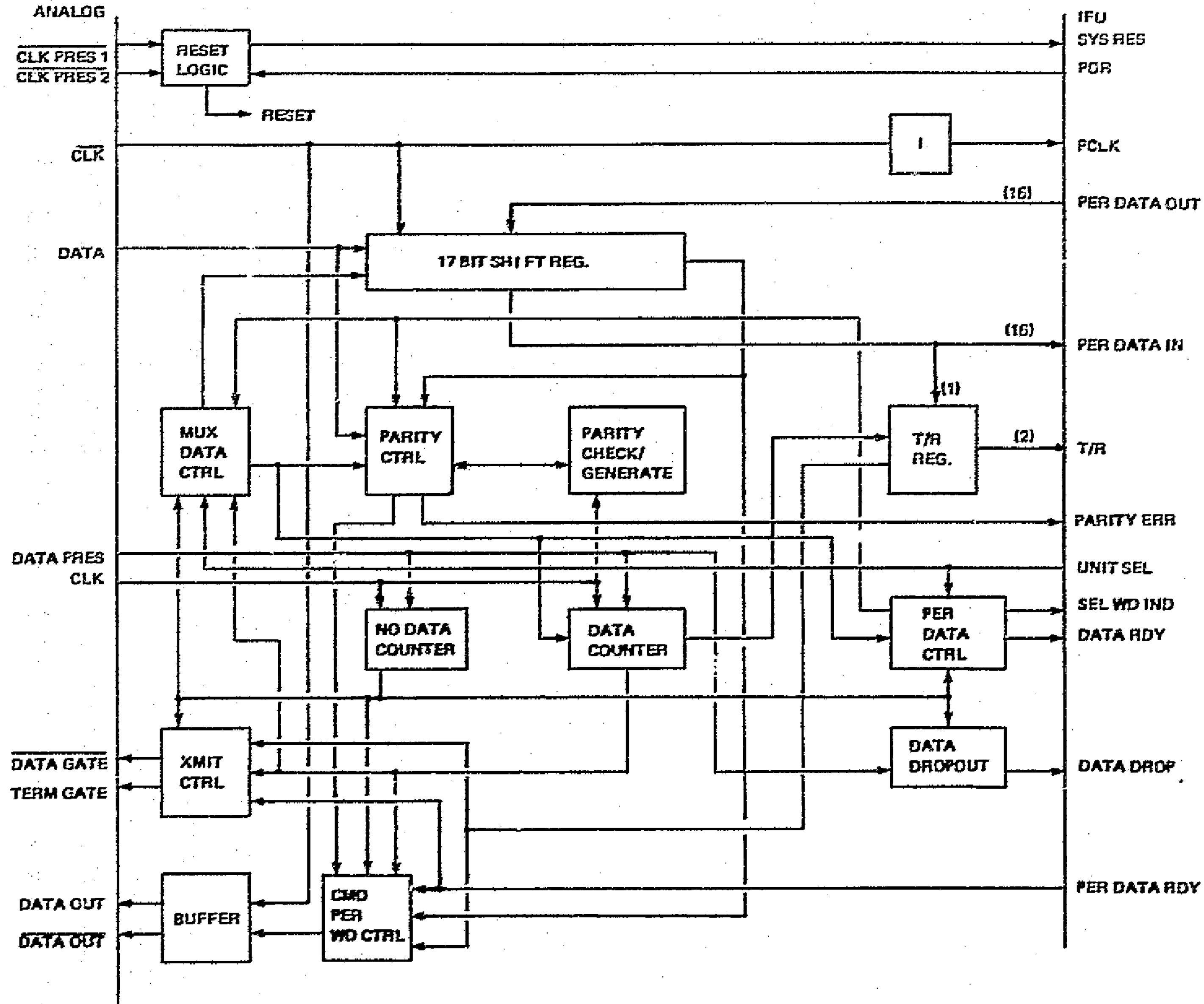

Figure 4.4-6b Bus Protocol Logic

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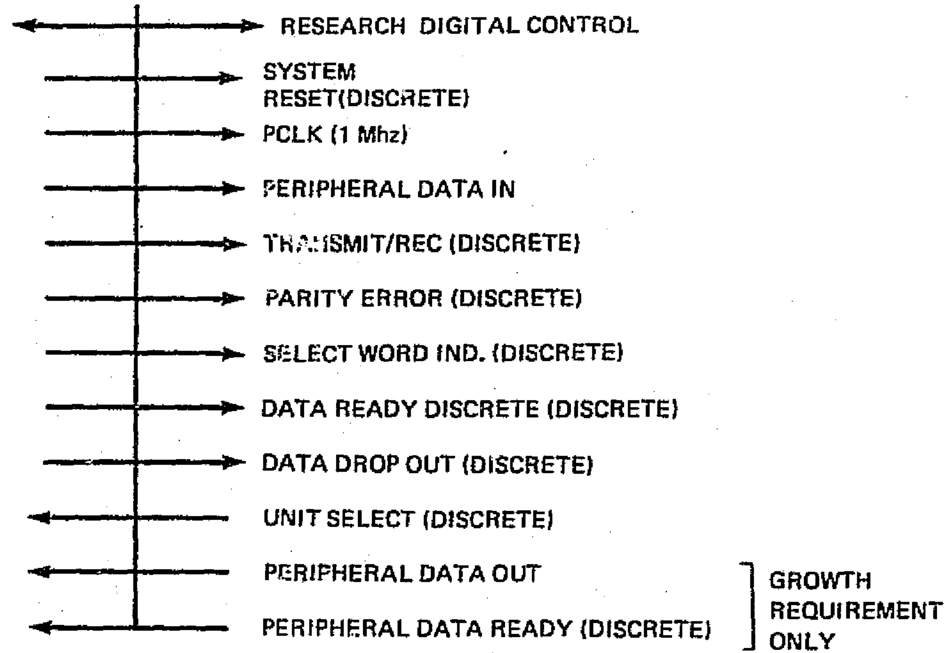


NOTES:

1.) I/F DRIVERS ARE 5405 MAX IFU CABLE LENGTH = 6'.

2.) UNIT SELECT IS A HANDSHAKE TO INDICATE RDC RECOGNIZES SEL WORD AND DESIRES FOLLOWING DATA. 2 GATE TIME DELAY IS ADEQUATE FOR HANDSHAKE.

Figure 4.4-6c. Central Computer I/F with RDC

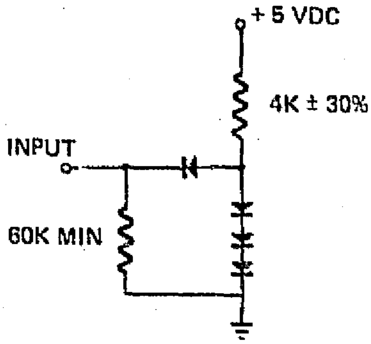
Table 4.4-2a
SERIAL TO PARALLEL CONVERTER LOGIC INPUT SIGNALS

Logical inputs to the Serial to Parallel converter from the Centrol and Select Module are defined as follows:

Serial to Parallel Input Characteristics:

o	Logical "0"	=	+0.4 volts maximum
		=	-0.4 volts minimum
o	Loading	=	10 TTL loads maximum

The equivalent input for 1 TTL load can be assumed to be the following:



Signal Description. The following are input signals to the X/R Module from the serial to parallel converter:

o	Power-On-Reset	A "1" state indicates the SPC power has been applied. The POR signal shall be applied at the same time +5V to the X/R Module is applied and held for at least 2 usec after the +5V supply has reached the +4.5V level or greater.
o	Transmit Data Bit 0 through Bit 15	Sixteen parallel lines of data to be transmitted from the X/R Module to the MUX bus.
o	Peripheral Data Ready	A "1" state indicates thet Transmit Data is available. Changes to a "1" within 1 usec after "Select Word Indicate" or "Data Ready" and remains at a logical "1" for 2 usec.
o	Unit Select	When at a logical "1", indicates the address contained in the Select Word is a valid address. Follows Select Word Indicate.

TABLE 4.4-2b
SERIAL TO PARALLEL CONVERTER LOGIC OUTPUT SIGNALS

Signal Characteristics. All output digital signals to the control and select module have the following characteristics:

o	Levels	Logical "1"	=	+2.4 volts minimum
			=	+5.5 volts maximum
		Logical "0"	=	+0.4 volts maximum
			=	-0.4 volts minimum
o	Drive Capability	Logical "1"	=	+0.4 MA
		Logical "0"	=	-16.0 MA

Signal Description. The following are output signals from the X/R Module to the control and select module:

o	Clock	1 MH_z digital signal decoded from the system MUX clock. Is available as long as one of the channel clocks is operational.
o	System Reset	A "1" state indicates both MUX channel clocks are deactivated. Remains a "1" for the duration of this condition.
o	Select Word Indicate	Indicates the word received from the MUX party line is a Select Word. Remains in a logical "1" state for 2 usec.
o	T/R Bit 1 ⊳1	A "1" state indicates that bit 11 of the received Select Word was a logical "1" (transmit mode). Remains a logical "1" for the length of the message. This signal operates regardless of the address code.
o	T/R Bit 2	A "1" state indicates that bit 11 of the received Select Word was a logical "0" (receive mode). Remains a logical "1" for the duration of the message. This signal operates regardless of the address code.
o	Data Ready/ Request	In the receive mode, indicates that 16 bits of input Received Data are available. In the transmit mode, indicates that the X/R module is ready to accept 16 bits of output data.
o	Received Data Bit 0 through Bit 15	Sixteen lines of parallel data decoded from the MUX bus.

1⊳ The NASA owned X/R module has been modified by inverting the T/R lines to permit operation of the RDC when the bus is driven by the c/c radar simulator.

TABLE 4.4-2b (CONT.)

SERIAL TO PARALLEL CONVERTER LOGIC OUTPUT SIGNALS

o	Parity Error	A "1" state indicates that the previous received word had bad parity. This signal is only present for 2 usec following the last bit of the word having bad parity.
o	Data Dropout	A "1" state indicates a data dropout condition has been detected or the time between words of a message is not five clock pulses. Once detected, this signal is held for one microsecond.

TABLE 4.4-3

SERIAL TO PARALLEL CONVERTER POWER REQUIREMENTS

Voltage	Maximum Current	Number of Wires	Minumum Wire Size	Maximum Distribution Length
+12	0.3A	2	#24	8 inches
-12	0.15A	2	#24	8 inches
-6	0.10A	2	#24	8 inches
+5	1.75A	4	#24	8 inches

A control select and data buffer system has been designed and is shown in Figure 4.4-7. Figure 4.4-8 is the corresponding timing diagram. This system was developed and breadboarded. The breadboard is documented by DFRC drawings FS-C-465 and FS-C-467.

The circuitry of Figure 4.4-7 performs the following functions:

1. Saves the current state of the bus select word

2. Identifies through the select word data to be saved in buffer memory,

3. Transfers data to the buffer memory,

4. Provides parity Error, Data Dropout Detection

System operation is as follows, the C/C radar simulator, Figure 4.4-5, generates select words to request data from the bus peripherals (HSI, ADC, AHRS, INS (IMU)). As shown in Figure 4.4-8a, the selected device transmits the requested data in reply on the transformer isolated serial synchronous bus. The C/C radar simulator has no bus listening capability. All listening is done by the two IFU's through the central computer bus interface (X/R module) which is a bus compatible serial to parallel converter. Unlike the standard aircraft PROFIT has only one non redundant bus. The output interface of the X/R module is defined by Figures 4.4-6 and 4.4-8.

The IFU I/F to the DMA bus is depicted in Figure 4.4-7. Operation is as follows. A select word is clocked into the select word register by SELWD. As each succeeding data word is received, the least significant four bits of the stored select word are downcounted so that the stored select word always corresponds to the available data word. The select word is decoded by the FPLA into a buffer memory address. Unrecognized select words decode to address 0. The least significant four bits of the address control the RAM address lines.

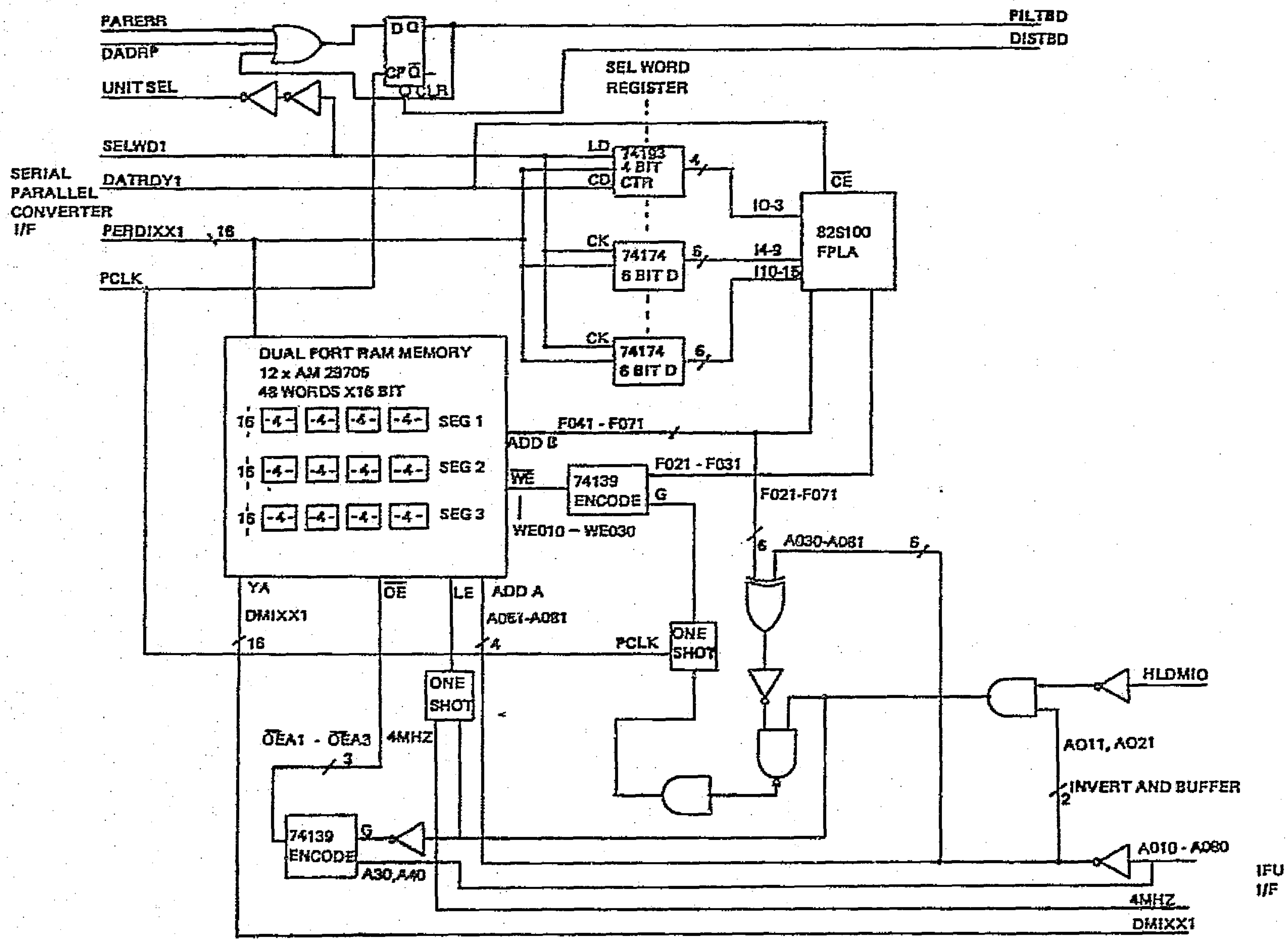


Figure 4.4-7. Control Select and Data Buffer

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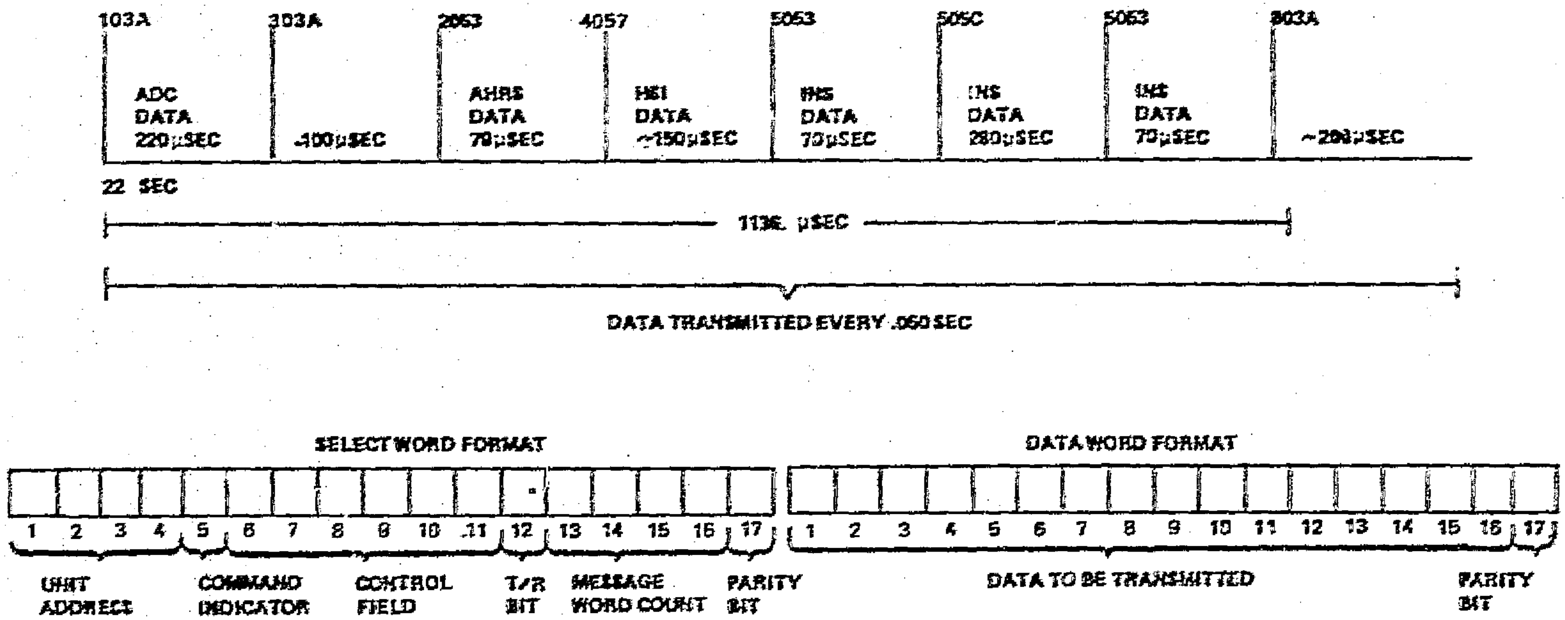
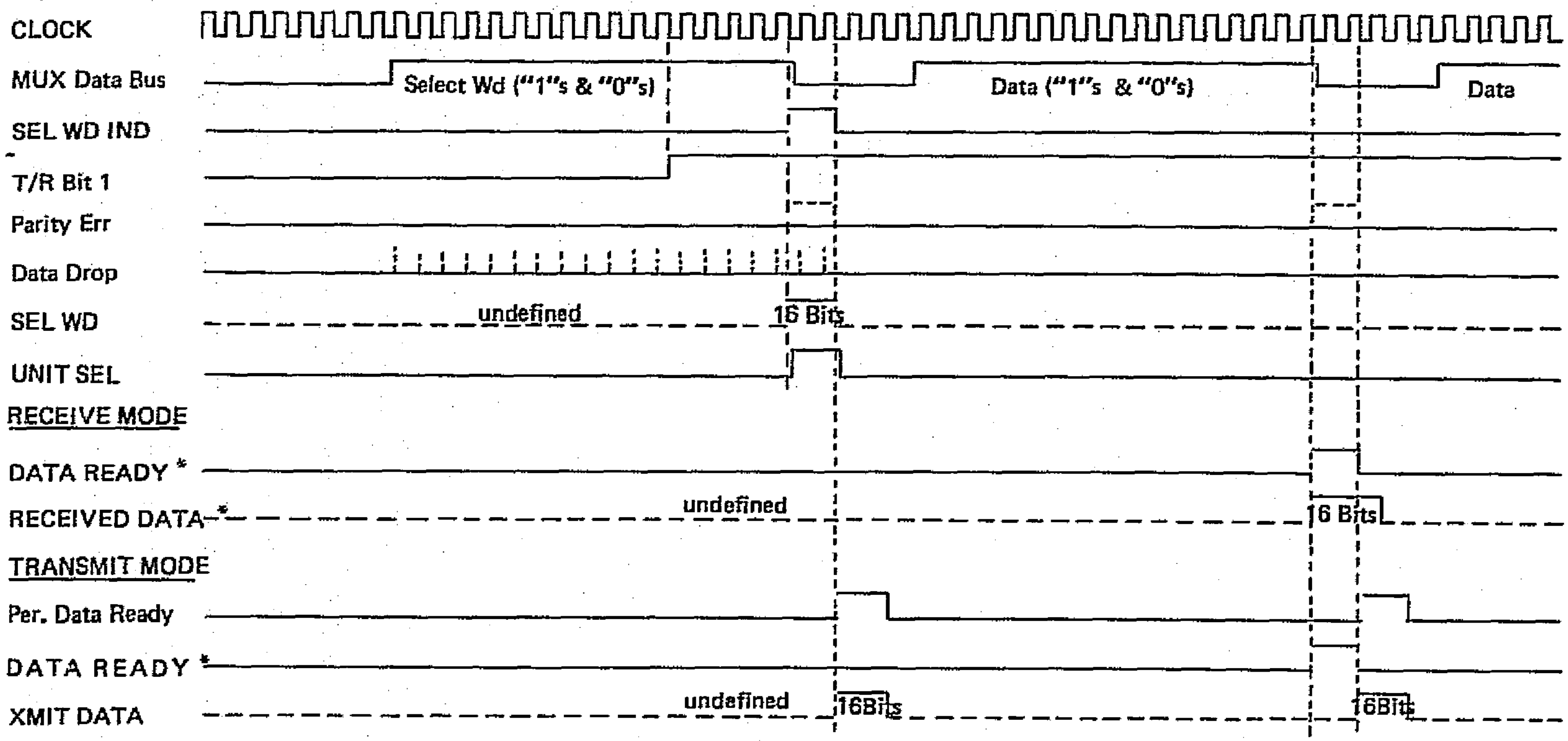


Figure 4.4-8a. C/C Bus Organization and Update



* SAME SIGNALS

Figure 4.4-8b. IFU/C/C I/F TIMING

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The most significant two bits are decoded and used to select memory segments through the RAM write enables. Writing is inhibited if the DMA system is accessing the same location as is the C/C bus. The inhibit function is provided by an exclusive or of the corresponding write and read address lines anded with HLOMI1.A011.A021 which indicates that the DMA is accessing the C/C bus interface.

Data are accessed from the buffer memory on an asynchronous basis using the existing DMA logic. HLDMI1.A011.A021 is used to latch data from the designated word within each segment into the segment output latch. This also gates the segment select line decoded from A30, A40.

4.5 GROUND SUPPORT EQUIPMENT

Ground Support Equipment (GSE) serves three related functions. System operational support, loading programs into and interrogating the flight computer, and providing displays of real time system data, is provided by an assortment of existing, or off the shelf components. Hardware checkout and trouble shooting requires, in addition to operational support equipment, monitor panels and breakout boxes to permit direct inspection of the flight hardware I/O interfaces. Finally a system simulation and appropriate interface are required to permit total system verification and trouble shooting. The following paragraphs discuss requirements and potential design solutions in these areas.

4.5.1 Ground Support Equipment Requirements

System operational support equipment must be able to do the following:

1. Load and confirm load of flight software into the DPCU.

2. Provide for read out and modification of core contents.

3. Provide for continuous (strip chart) and snapshot (digital engineering units) display of PCM data.

4. Monitor system power input and internally derived system power.

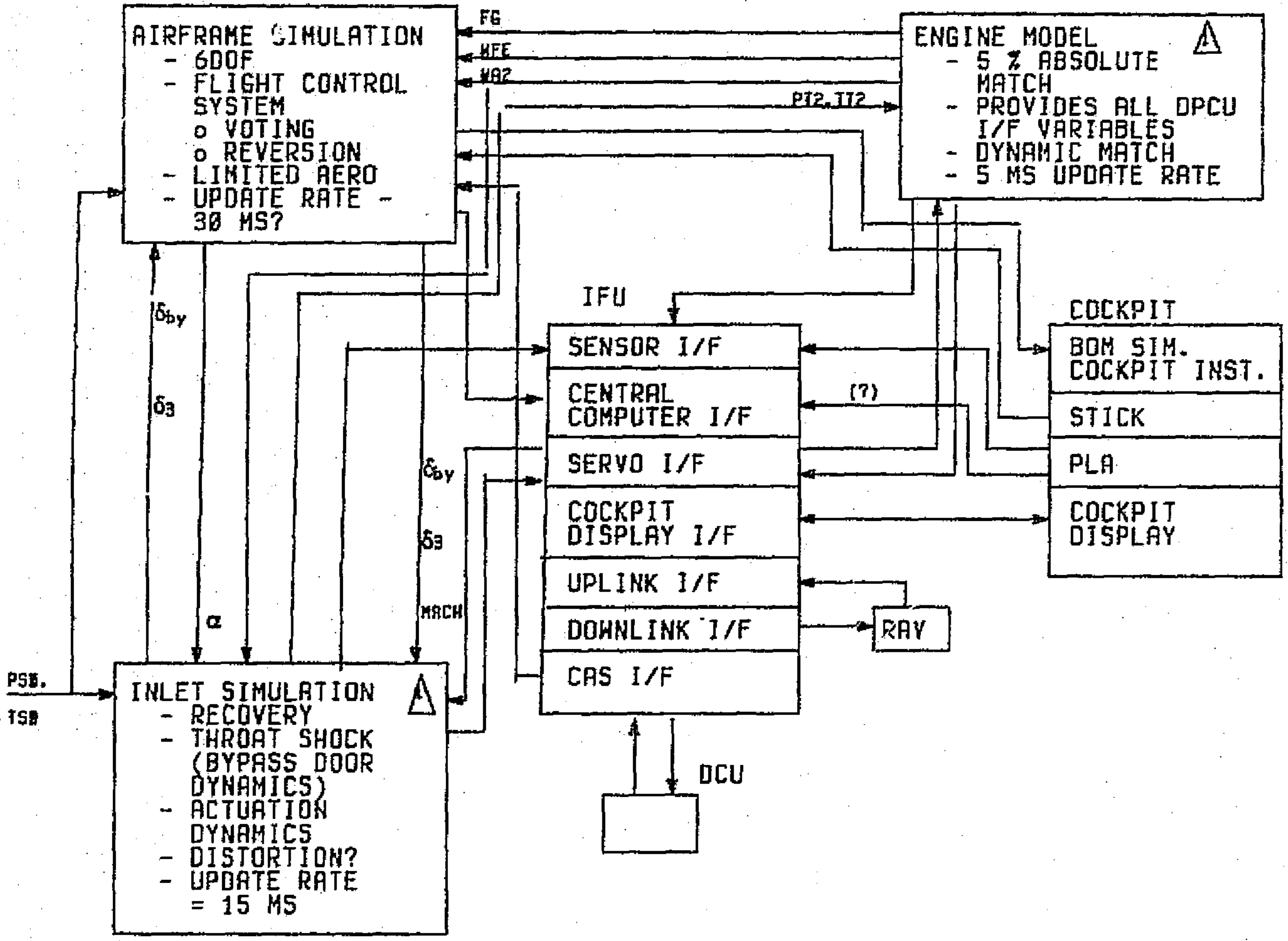
Trouble shooting equipment must provide the capability to observe any DPCU input or output signal during any phase of ground testing including ground engine runs. In general this equipment will take the form of breakout boxes suitable for temporary installation in series with normally installed cables. Cables transmitting high speed digital data, DCU/IFU interface, Central Computer Interface to IFU, and the Telemetry to IFU interconnect will not be so equipped.

The system simulation must operate in real time and be sufficiently detailed and accurate to permit closed loop software verification using a flight configuration of the DPCU. In order to do this the following functions, depicted in Figure 4.5-1, must be performed:

1. Inlet Simulation
2. Engine Simulation
3. Airframe Simulation
4. Sensor/Actuator Simulation
5. Peripherals Simulation

Assuming the first three simulations are digital the required update rate is 200 hz. The sensor/actuator simulation is by nature analog and timing of the peripherals will be identical to flight systems. Simulations will be implemented as required by overall system development. Thus for System B only an airframe and peripherals simulation will be required. System B GSE is documented in Section 4.5.3.

The inlet simulation requirement will be more accurately defined after a review of the McAir digital inlet simulation. Currently a 6th order dynamic



WHEN BOTH RDC'S ARE USED SIMPLIFIED SIMULATIONS OF INLET, ENGINE REQUIRED FOR RH SIDE

Figure 4.5-1. PROFIT Simulation Requirements

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model including frequencies perhaps as high as 10 hz, and a detailed recovery model is considered adequate.

The engine simulation requirement is defined by the LERC hybrid engine model, Reference 19. This consists of a 16th order model incorporating high frequency duct dynamics, compressor and turbine maps and RCVV and CIVV effects. Depending upon the simulation approach used it may be permissible to reduce the model band pass from that achieved at LeRC to achieve real time operation at the desired sample rate.

NASA DFRC is currently developing a real time simulation of the F-15. For PROFIT application this must provide, in addition to the basic airframe model and flight control system model, a detailed representation of the flight control system backup modes and failure detection system so that PROFIT software failure mode behavior can be tested and verified. In addition for cruise mode interactive control a highly detailed trim drag model is required. Since PROFIT, for a variety of reasons, is not intended to fly integrated control modes at extreme angles of attack the airframe model need not have sophisticated high angle of attack aerodynamics.

The sensor and actuator simulation requirement is to provide a simulation of actuator and sensor dynamics with IFU compatible interfaces on one side and simulation compatible interfaces on the other.

The peripherals simulation must provide, at a minimum, the same rate of inputs to the interrupt structure and DMA system as provided by the flight hardware. In addition these simulations may be used to provide information transfer to and from the DPCU.

4.5.2 GSE Design (System A)

Figure 4.5-2 depicts system operational support equipment. The high speed paper tape reader in conjunction with the computer control unit loads and

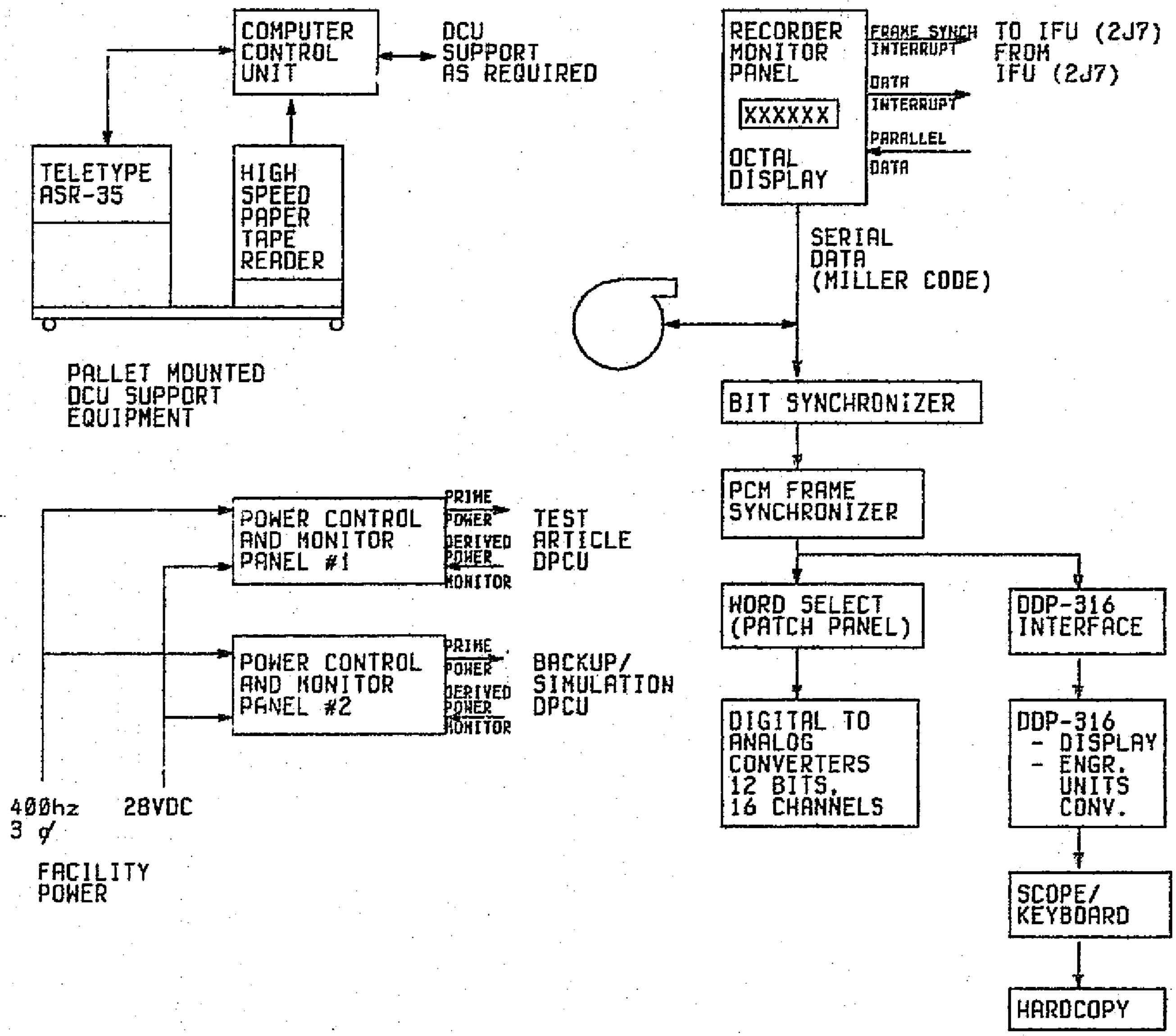

Figure 4.5-2. PROFIT GSE - System Operational Support Equipment

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verifies, in conjunction with system software, object tapes into the DCU. Data are punched on the object tapes in 50 word blocks which incorporate a checksum computed during the tape generation process. The DCU verifies correct receipt of each block against this checksum. This hardware/software system was successfully used throughout the IPCS program. The teletype working through the CCU provides a backup paper tape reading capability and a convenient means of interrogating or modifying core. This equipment is mounted on a mobile pallet so that it can be moved close to the DPCU location when required to meet the 6 foot DCU/CCU interconnect requirement.

Continuous and snapshot display of DPCU data and an event playback capability is provided by the equipment shown in figure 4.5-2. The Recorder Monitor Panel used throughout the IPCS program provides the interrupts necessary to drive the DPCU PCM downlink interface of the IFU. When the system is operating the IFU provides a sequence of 59 data words plus a frame synch word in parallel format to the recorder monitor panel which provides an octal display of any single word in the data stream and serializes the data. The serial data is recorded for playback and returned to parallel format and decommutated by the bit synchronizer and PCM Frame Synch unit, and then displayed through digital to analog converters on strip chart recorders. An interface between the DDP-316 minicomputer and PCM Frame Synch unit provides for processing of data snapshots into engineering units for display by 316 peripherals. A simple scope keyboard/ hard copy generator operating through the existing teletype current loop interface to the 316 provides snapshot display. The existing teletype unit could be used for this purpose but is slow and noisy and thus not recommended.

Two power monitor and control panels, one removed from the IPCS test set and another built to the same print are incorporated in the GSE. One provides prime power control and derived power monitoring to the backup/ simulation DPCU. The other provides these functions for the test article.

The simulation configuration used for software verification and integrated control mode testing at DFRC differs somewhat from that used to support engine running at ground facilities.

Because virtually all airframe inputs to the DPCU pass through the central computer bus, a central computer bus simulator driven by a simple program in the DDP 316 can supply the necessary bus data to represent the airframe during engine test facility activities. The same is true of the RAV uplink. Thus the only dynamic simulation required for field operations is of the engine and inlet. As shown in Figure 4.5-3 the engine/inlet simulation is conceived as a hybrid simulation utilizing the DDP-316 to calculate maps and the analog computer to perform integrations and summations. The DDP-316 is indicated as the digital element of the hybrid because two are available at DFRC and because it is software compatible with the flight computers. The D/A, A/D interface is assembled from commercially available components and will work on a handshake basis with the DIO system. Estimated computational requirements for the analog computer are shown in Table 4.5-1.

Servo and sensor simulations are provided separately from the analog computer because they use a large number of computing elements but don't really require the level of accuracy and flexibility provided by the analog computer, and because a large part of the simulation consists of modulators and other networks to represent hardware component characteristics which must be built up specially anyway. In addition the servo simulator can be used as a stand alone unit for DPCU open loop testing and checkout.

A cockpit simulation is provided including all cockpit panels, a simulated caution light panel, and a power lever.

The backup DPCU is connected to the simulator during ground tests to provide a parallel software debug tool immediately available during engine test. This arrangement should simplify software configuration control since debug

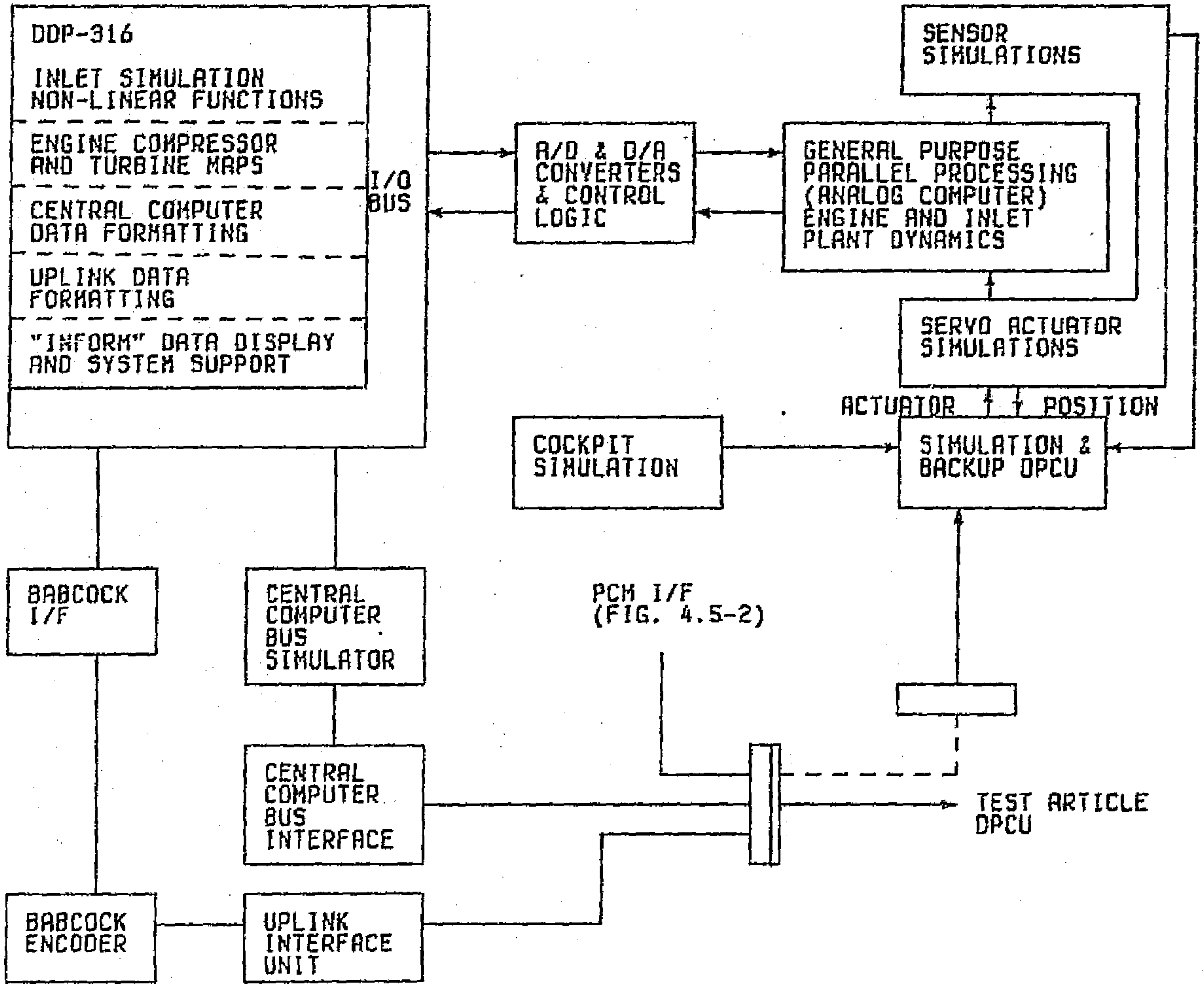

Figure 4.5-3. PROFIT Engine/Inlet Simulation

TABLE 4.5-1

COMPUTATIONAL REQUIREMENTS FOR ANALOG PORTION OF ENGINE/INLET SIMULATION

COMPONENT TYPE	POTS	SUMMERS INVERTERS	INTEGRATORS	MULTIPLIERS	DIVIDERS	DACS	DAMS	ADC
ENGINE	150	84	16	35	21	13	8	10
INLET	Inlet Requirements not yet defined							

NOTE: These requirements do not include sensor and servo dynamics which are incorporated in the Simulation Interface Adapter.

changes and tests won't be made on the DPCU controlling the engine. In addition, controller changes can be quickly tested without risking engine damage.

4.5.3 Ground Support Equipment (System B)

System B GSE is structured around existing or facility hardware to reduce cost. Figure 4.5-4 depicts the hardware involved and it's arrangement.

DCU support equipment is existing IPCs hardware used to load programs into and communicate with the RDC. The NASA airframe simulation including BØM AFCS is interfaced to the RDC through two interface simulations. The CAS I/F simulator is basically a set of four 400 hz demodulators. The airframe I/F simulator includes two analog channels (To, α) and a digital multiplexer simulating the output of the X/R module. The airframe simulation is also interfaced to both the airplane and simulator cockpits. The existing TSU is retained to provide breakout and power control capabilities and to support the data reduction capability described above.

4.6 N1/N2 INPUT INTERFACE

Figures 4.6-1, -2 compare the F100 BØM tachometer output characteristics in terms of voltage and frequency to the input characteristics of the IFU tachometer frequency to digital converters. The following paragraphs discuss modifications required to make the devices compatible.

4.6.1 N1 Input Interface

As shown in Figure 4.6-1 the N1 input interface is unmatched both in terms of input frequencies and minimum input voltage. These mismatches are rectified as follows:

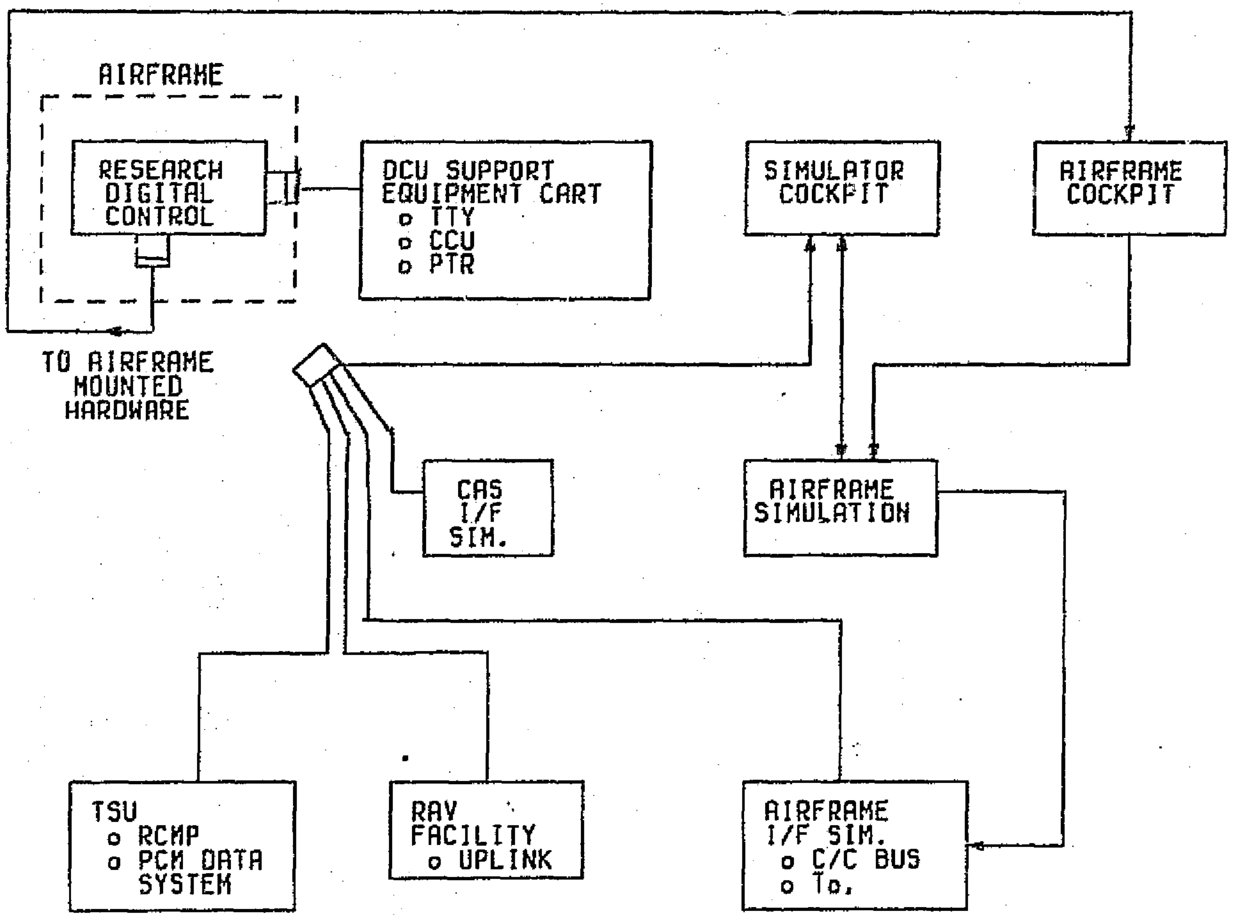

Figure 4.5-4. System B GSE

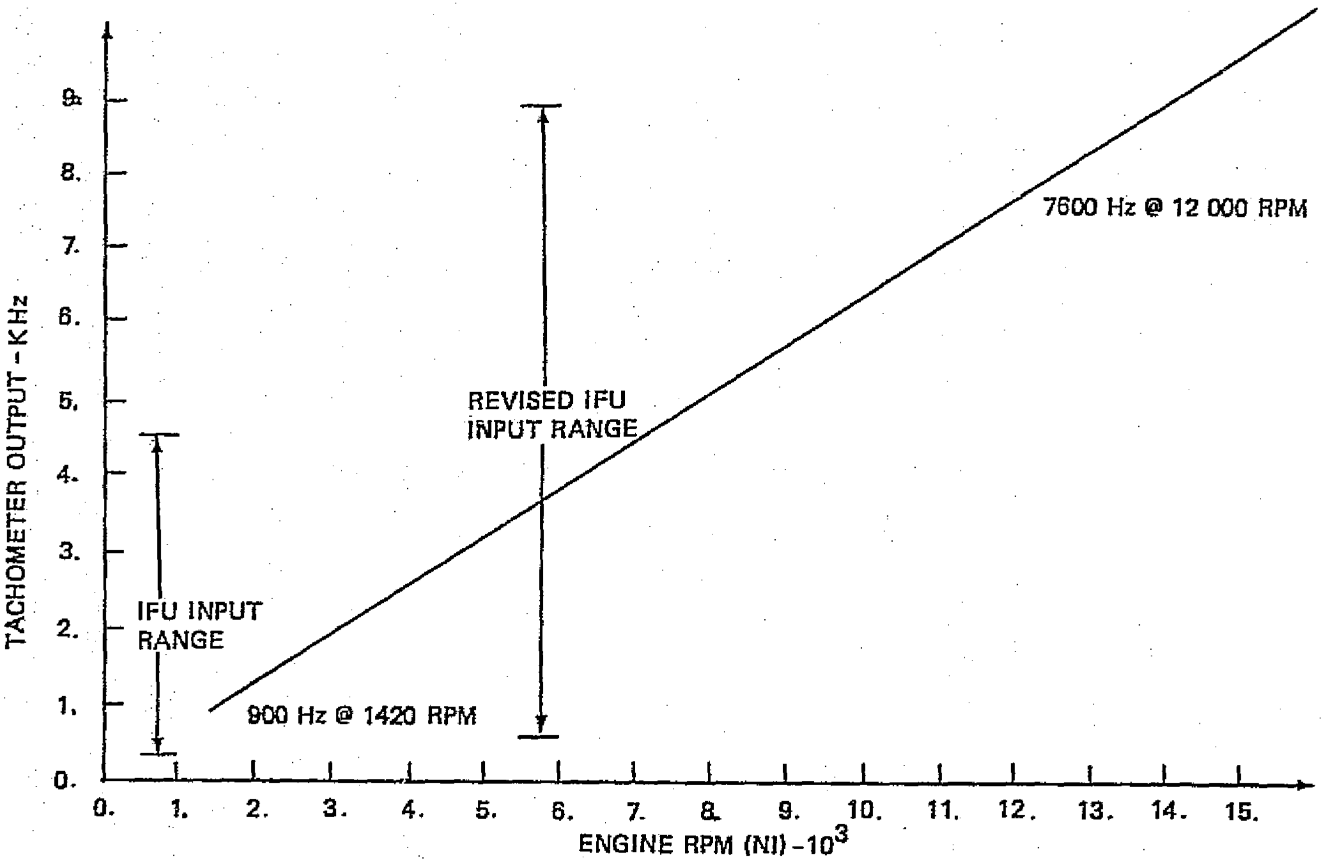

Figure 4.6-1. N1 Interface Characteristics a. Frequency

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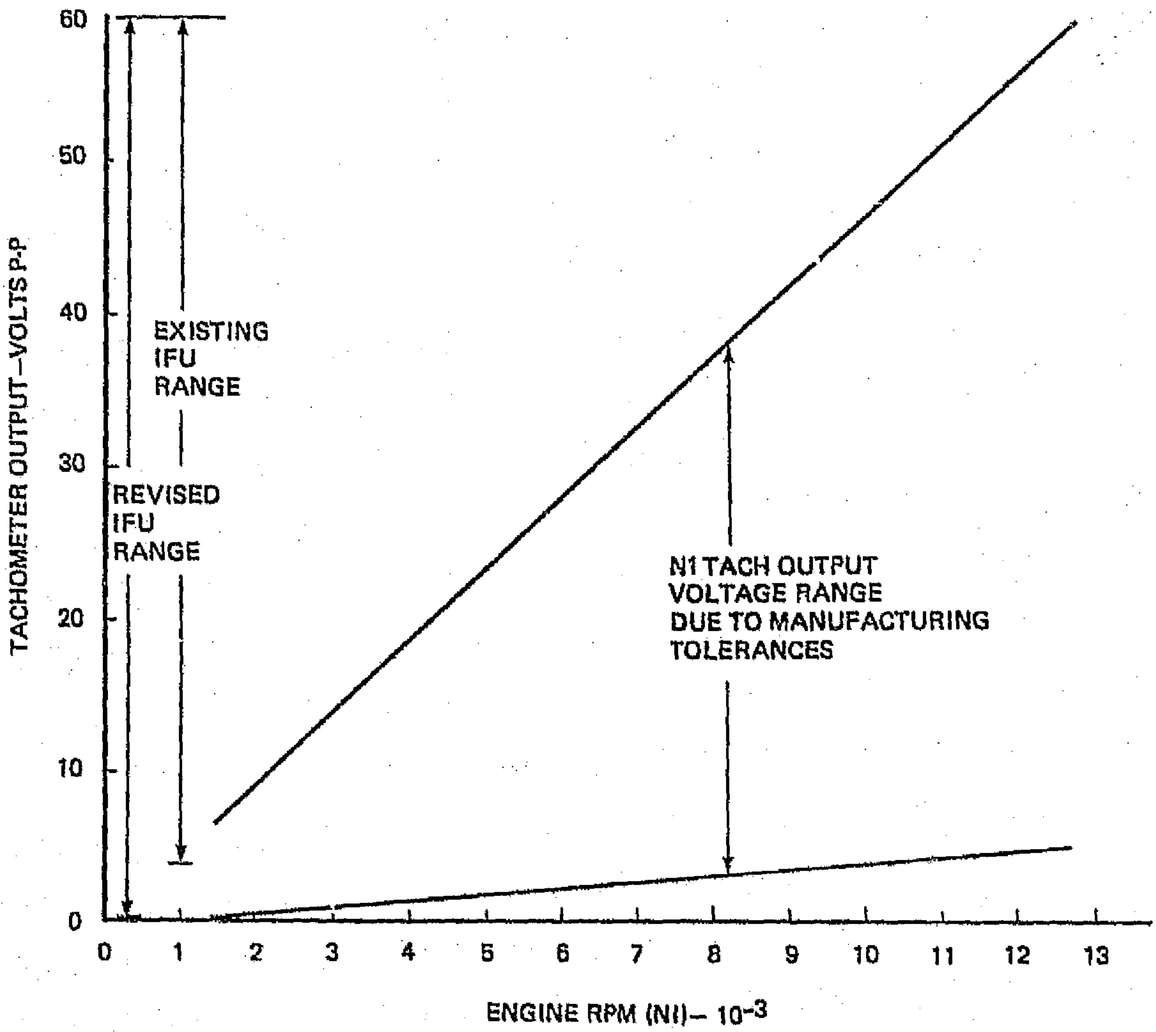

Figure 4.6-1 N1 Interface Characteristics b. Voltage

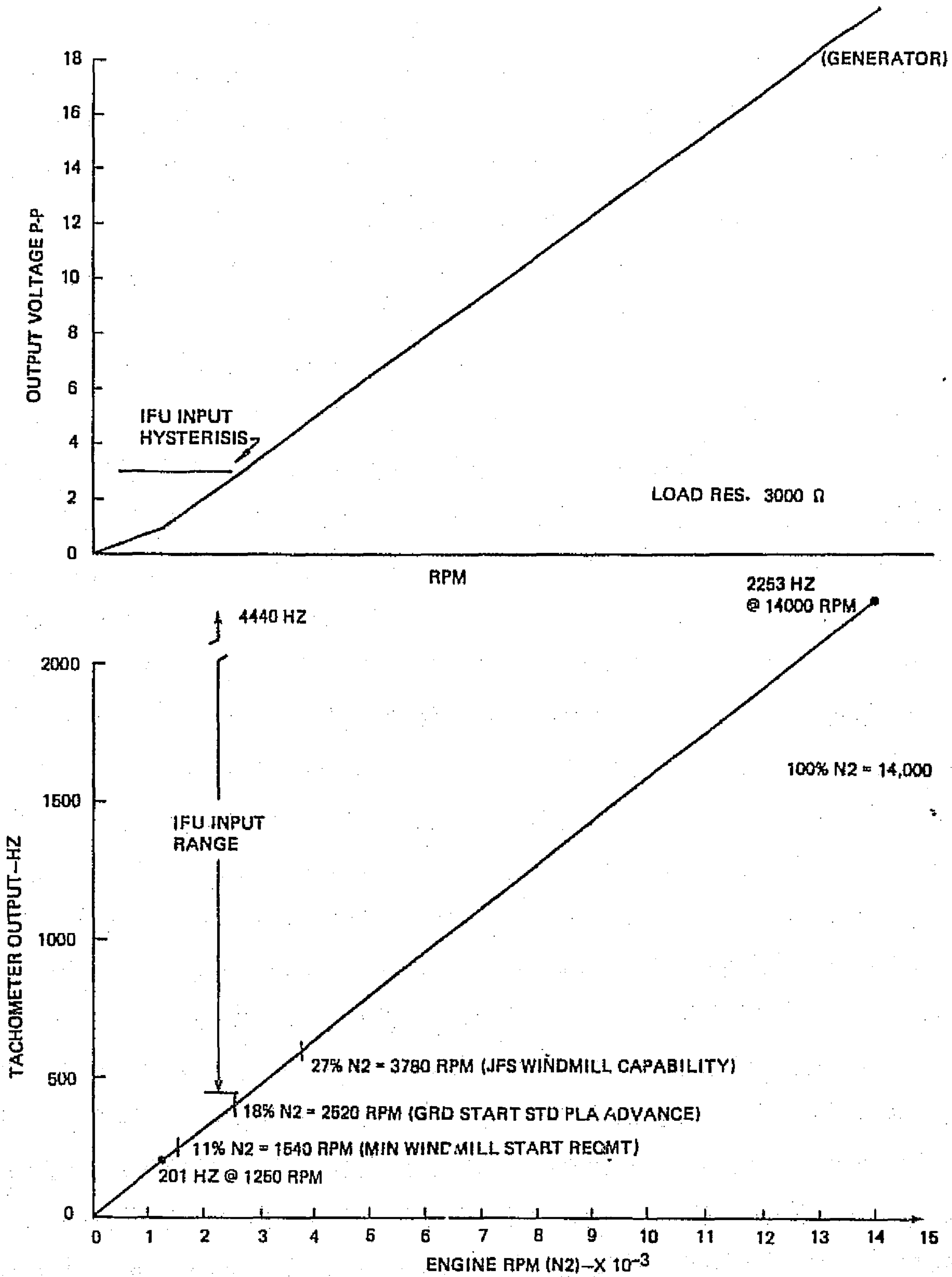

Figure 4.6-2. N2 Interface Characteristics

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1. Revise minimum voltage by reducing 702 card input hysteresis by changing resistors R9, R10 (Channel 1) and R20, R21 (Channel 2),

2. Insert a divide by two counter after the input conditioning amplifier in each channel.

Because new cards must be built for N1 processing anyway, the original IFU design only provides two tachometer inputs, change 1.) is trivial, change 2.) requires a minor change in board art to install an additional 5474 dual D flipflop to provide the divide by two counter.

4.6.2 N2 Input Interface

As shown in Figure 4.6-2 the N2 tachometer interface is acceptable if electronically controlled starts are not initiated (power level not advanced above cutoff) below 20% N2. This is similar to procedures used in IPCS. Its acceptability from a flight safety standpoint (air start) on this aircraft requires review.

4.6.3 Additional N1, N2 Processing Modifications

As a result of IPCS experience a minor circuit change, Figure 4.6-3, is made to clear converter data registers before counting each sample. This eliminates a potential sneak failure mode in which a tachometer failure results in valid appearing but unrelated data at the interface card output.

4.7 LVDT INTERFACE

The existing IPCS LVDT excitation generators and processing circuitry are not configured to operate at the design frequency and voltage of the F-15 inlet LVDT's. The table below presents the contrast.

MODIFY A16 (10048702) CARD AS SHOWN
NOTE: 5400 I. C. U 00 MUST BE ADDED TO BOARD

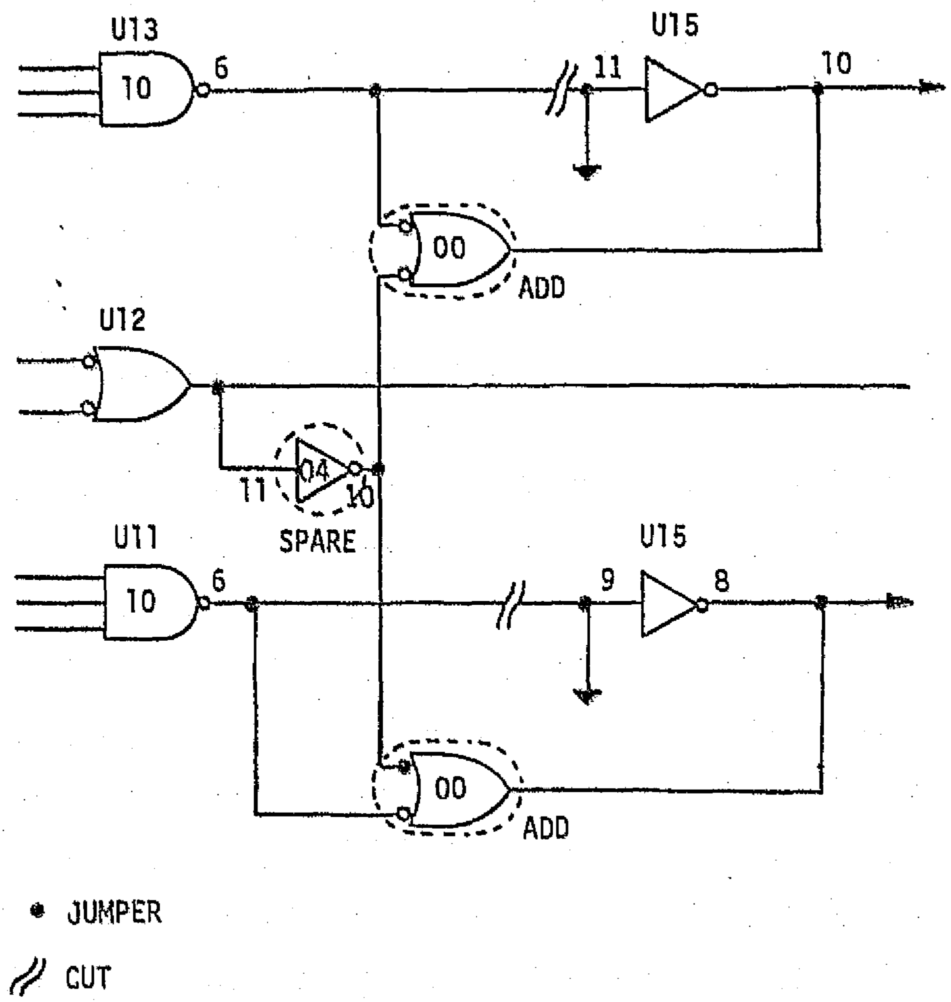


Figure 4.6-3. N1/N2 Converter Modification to Clear Converter Prior to Each Sample

	F-15	IFU Ch. 1	IFU Ch. 2, 7
RMS VOLTAGE	7 VAC $\pm$ .025	9 VAC $\pm$ 10.%	9 VAC $\pm$ 10.%
FREQUENCY	2.5 Khz	3.906 Khz	.9776 Khz
LOAD VA/DEVICE	TBD	TBD	TBD

There are two ways to resolve this problem. Operate F-15 LVDT's off design at .9776 Khz or rework the excitation generators and demodulators to 2.5 Khz. The bypass door LVDT will be selected to be compatible with .9976 Khz excitation for convenience. The large discrepancy in excitation accuracy is not significant since the IFU also demodulates the LVDT excitation and software is used to adjust the raw data and command as required.

The existing demodulators can be changed to 2.5 Khz by replacing two passive components per channel. Changing excitation frequency is somewhat more difficult, requires a large number of passive component changes and 2.5 Khz is not a conveniently available frequency in the timing chain. The consequences of operating the LVDT's off design were reviewed with the manufacturer (MOXON) with inconclusive results. A lab test to determine LVDT behavior at the frequencies and voltages of interest would be required to permit their operation off design in the airplane.

4.8 PAROS CONVERTERS

No significant changes are required to the 704 card input interface or excitation because Paros transducers similar to those used on IPCS are used.

4.9 RESOLVERS

All IPCS resolvers were wired as shown in Table 2.5-4b and operated within one quadrant. The resolvers to be used for PROFIT are electrically identical to the IPCS units with the exception that the redundant WFG resolvers are wired as indicated in Table 2.5-4b and operate over more than one quadrant.

Thus resolver interface cards for eight of the resolvers are unchanged from IPCS. Processing of the two fuel flow units will be changed as necessary to match the DEEC resolver configuration.

4.10 ANALOG TO DIGITAL CONVERSION

All analog inputs to the IFU will be arranged to fall into either a $\pm$5.12 VDC or $\pm$30 MVDC range. Three IFU modifications are requred in this area:

1. Build and install -688 card in IFU A2 slot to extend low level mux to 32 channels.

2. Add wiring from card slots to input connectors as required.

3. Remove or modify specialized input resistance networks on -748 card.

4.11 DISCRETES

Existing input and output discrete cards will be modified as required to meet interface requirements.

4.12 SERVO LOOP CLOSURES

As shown in the block diagram, Figure 2.5-1, the torque motor controlled servo loops are closed on an analog basis through resolver demodulators and torque motor drivers. Servo commands are generated in software and output to the servo cards through the IFU D/A converters. This provides good servo response without imposing sampled data constraints on the control or creating software complexity attendant to performing servo loop computations at minor cycle sample intervals. The approach is selected because it maximizes research system flexibility. In a production system servo loops might be closed through software.

The dual servo loop closure card is derived from two existing IFU card designs. The amplifier output stage is a current feedback torque motor driver similar to that used in 728 Spike and Cone Driver. The resolver demodulation, error summation, compensation and error buffer stages are identical to those used in the 694 Main Fuel Control. Different compensation and gain will be provided as necessary by appropriate selection of passive circuit elements. As shown in the figure two complete sets of loop closure electronics fit on a single IFU card.

Where LVDT feedback is used in lieu of resolvers the demodulated LVDT voltage is connected to the error summation instead of the output of the resolver demodulator. A preliminary card design for the dual servo card is shown in Figure 4.12-1.

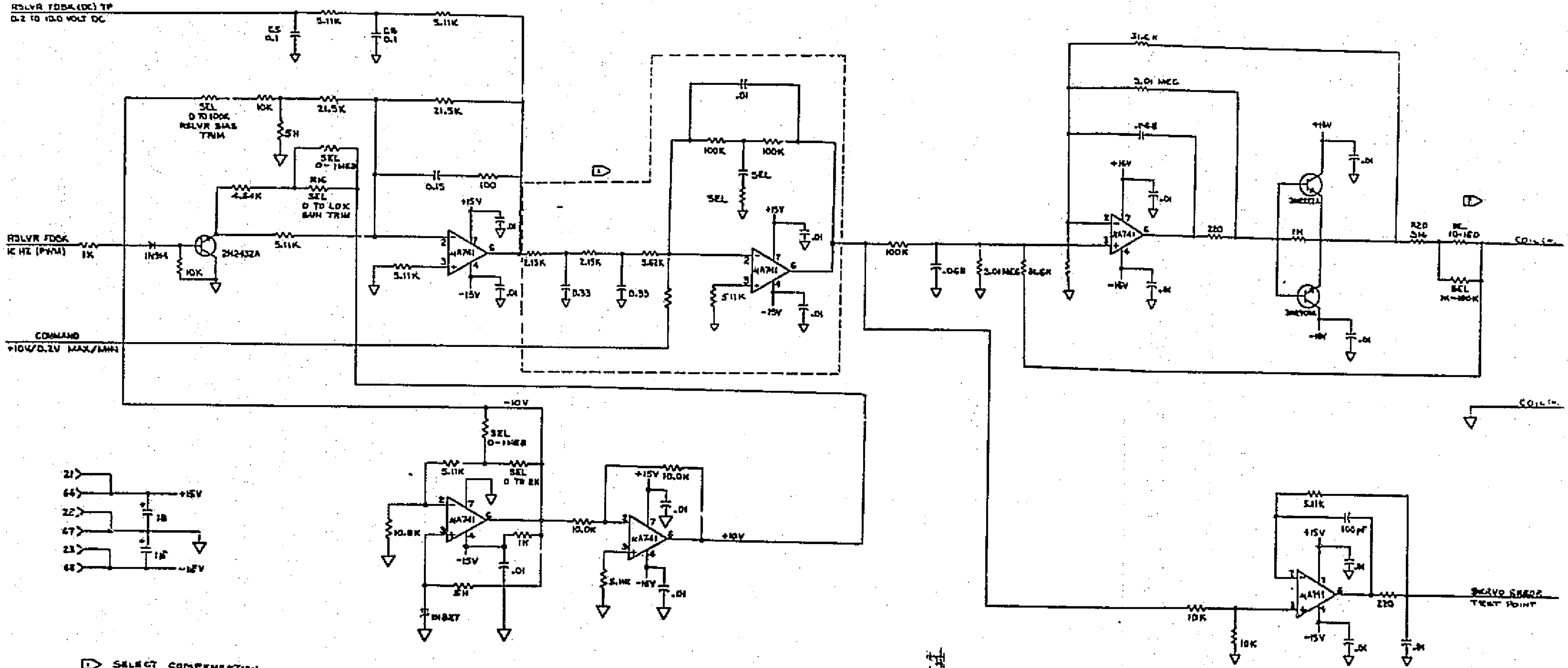
4.13 CAS INTERFACE

4.13.1 CAS Interface Requirements

Each Research Digital Control (RDC) outputs two ± 10 VDC signals proportional respectively to roll rate command, $\emptyset^{o}_{c}$, and normal acceleration command, nZ_{zc}. These analog data must be reformatted as indicated in Table 2.9-1. In addition, the inputs from the two RDC must be error checked to the following criteria:

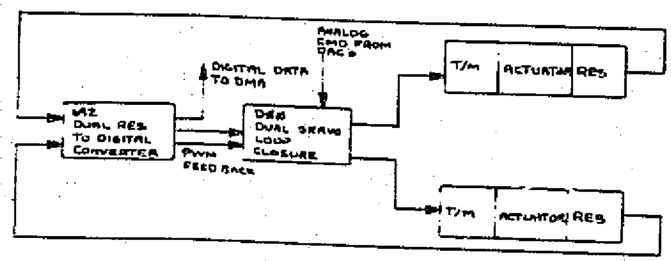
1. |Command differential| $\geq$ Differential limit,
2. Normal accel cmd GT.7.G or LT.-3.G
   Absolute roll rate cmd GT. Roll Rate Limit,
3. Master disengage,
4. Measured normal accel GT.7.G or LT.-3.G,
   Measured absolute roll rate GT. Roll Rate Limit,
5. RDC power off.

If any of statements are true the CAS interface outputs must disengage if engaged or inhibit engagement if already disengaged. In the disengaged



1 SELECT COMPENSATION ESMN AS REQD

2 CHANNEL 1 ONLY SHOWN
CHANNEL 2 IDENTICAL



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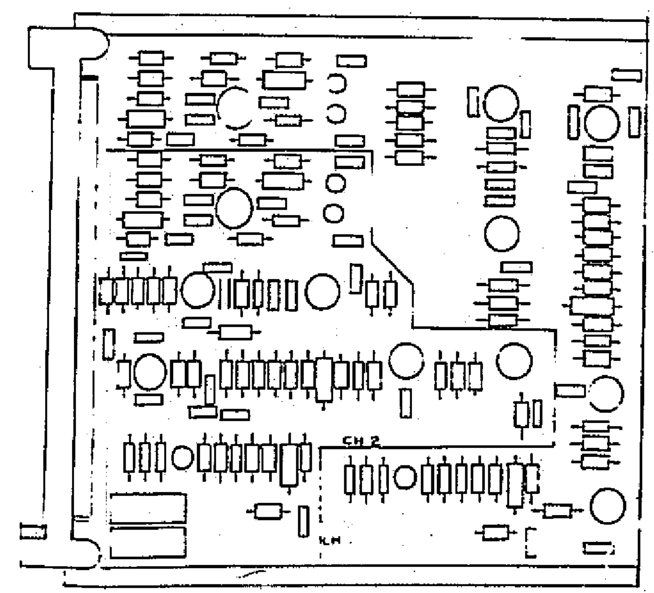

Figure 4.12-1. Dual Servo Loop Card

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mode the CASIF shall short the differential inputs to the CAS and open the outputs of the CAS modulator. The CAS interface power shall be supplied by the RDC. CASIF engage/disengage shall be controlled by cockpit and RDC discretes. When disengaged due to an indicated system error, CASIF power shall automatically be turned off.

4.13.2 CAS Interface Design

The following paragraphs describe a preliminary circuit design to meet the requirements of 4.13.1. Since inputs from both RDC are required it is assumed that this circuitry will be packaged in a separate box.

The CAS Interface Modulator, Figure 4.13-1, converts roll rate and normal acceleration commands generated by the DCU and output as analog voltages by the D/A converter to 400 hz amplitude modulated signals compatible with the existing CAS force sensor inputs. No modifications to the CAS are required since input and excitation are connected to the existing aft seat connections.

The modulator uses the CAS excitation voltage used by the pilot (aft stick) inputs as a frequency source. The excitation is modulated by an analog multiplier controlled by the d.c. command level output by the D/A converter. The multiplier output is buffered and a.c. coupled to eliminate offset. Transfer and positive disengagement are provided by relays which both crowbar the buffer output and remove power from the board. These relays are controlled by logic not shown in the schematic to meet disengage requirements. The excitation is demodulated and tied back to the DPCU A/D converters so that DCU commands can be corrected for excitation voltage variations. An excitation validity check may also be performed prior to engagement. Alternatively the multiplier output could be demodulated and compared to the desired command for calibration and validity checks.

As shown schematically in Figure 2.5-4, the CASIF box incorporates a low cost normal accelerometer and roll rate gyro to provide an independent

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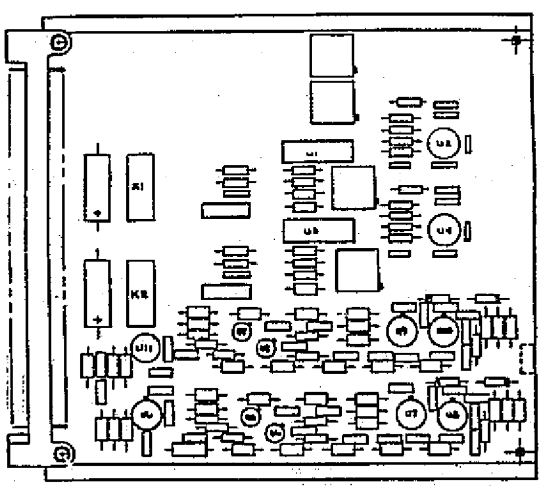

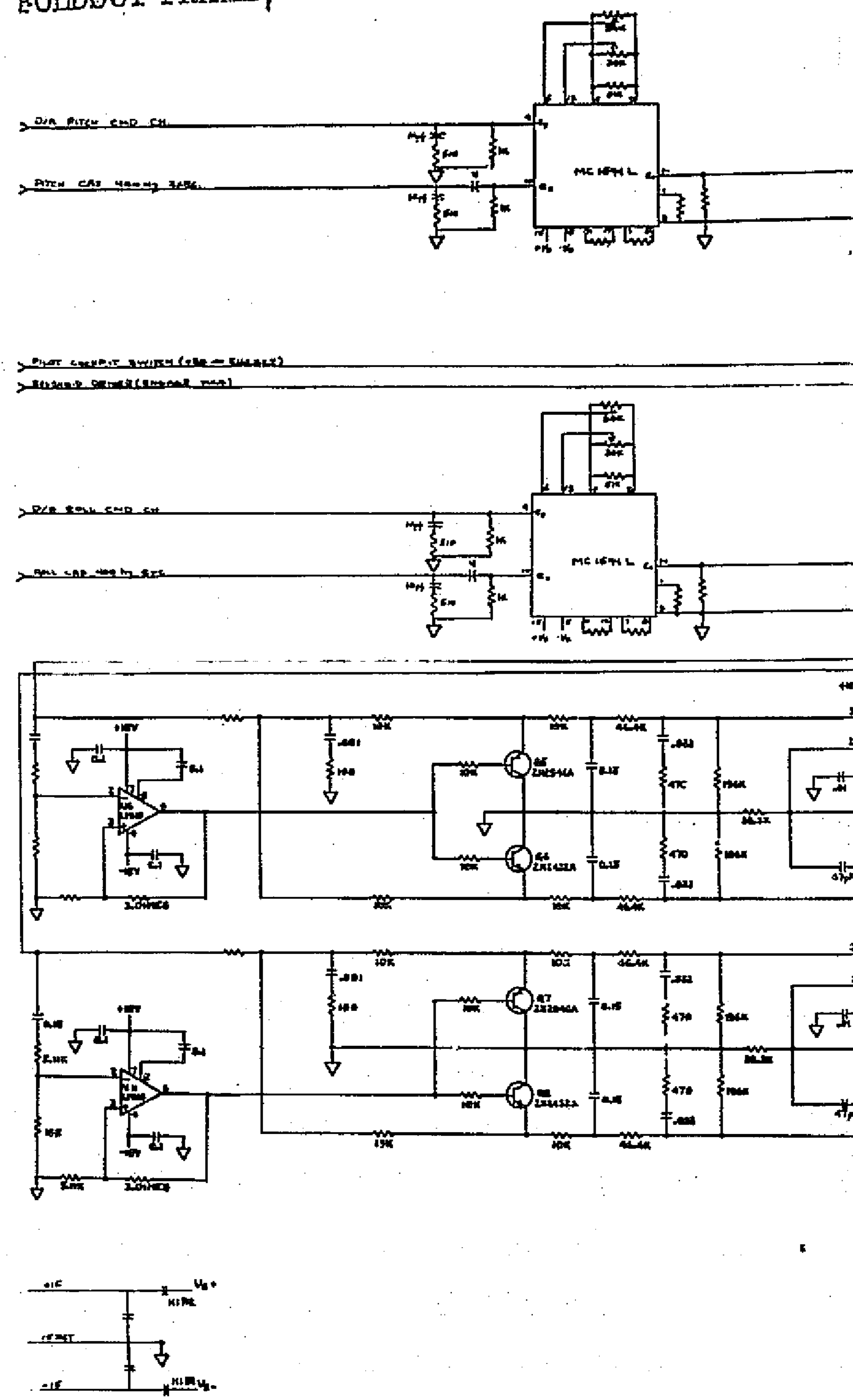

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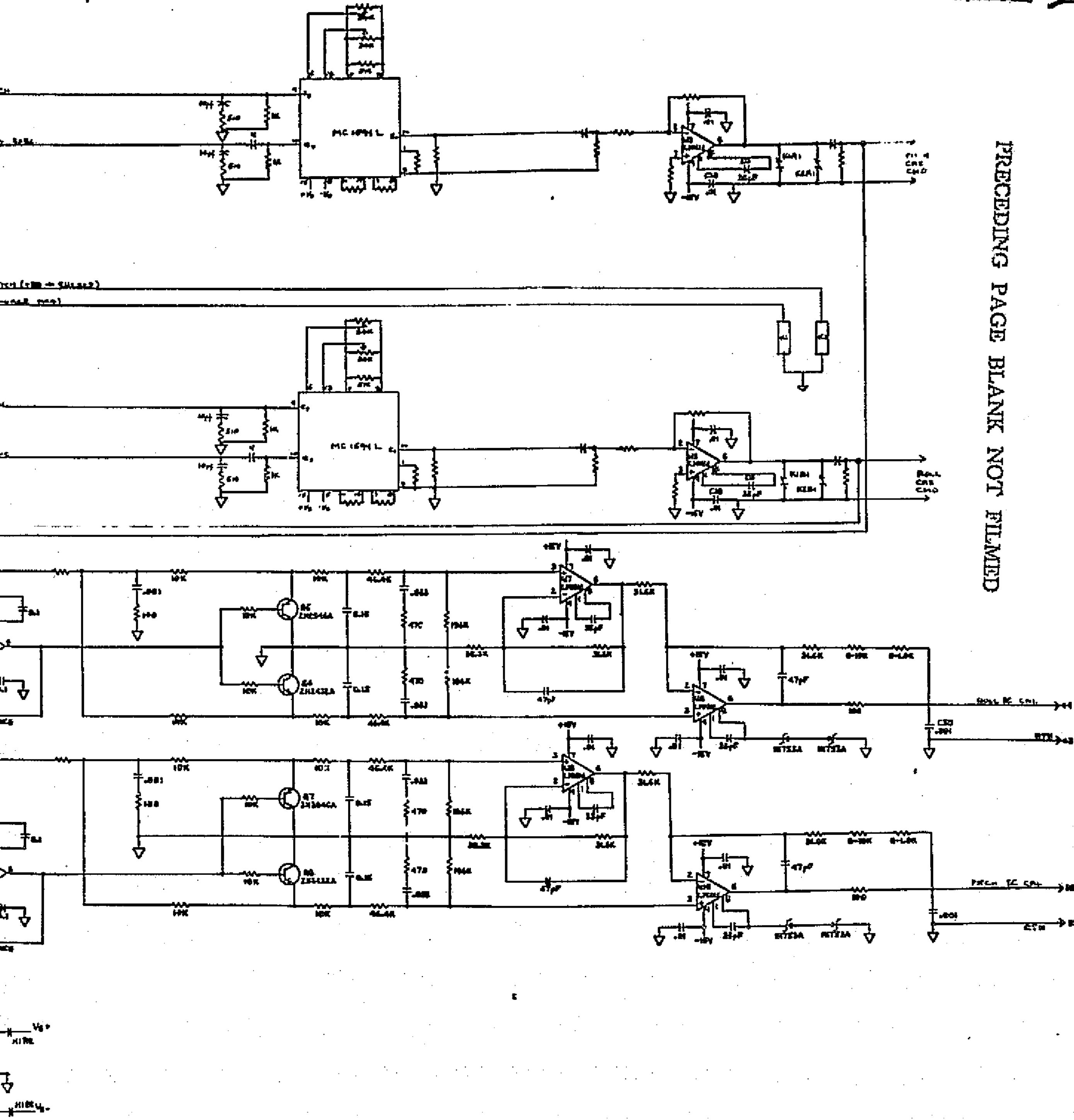

Figure 4.13-1. CAS Interface Modulator Card

check of airframe motion. These are independently powered off 'rframe 28 VDC.

4.14 AUTOTHROTTLE

4.14.1 Autothrottle Requirements

The autothrottle system requires the following inputs from the RDC.

1. Excitation for the five discrete switches. This will be either 5 or 28 VDC with the load selected as convenient for the RDC, and consistent with noise suppression and switch characteristics.

2. The A/C servo motor requires control voltage from the IFU consistent with servo loop forward gain and the torque speed characteristics of Figure 4.14-1.

3. The magnetic clutch is engaged by a d.c. voltage. Nominal engage signal is 28 VDC @ .25 amp.

4. Resolver excitation, 26 volts at 400 hz, .06 amps.

5. Required servo slew rate is 15^{o}/sec PLA.

6. Required servo closed loop bandpass is $10.sec^{-1}$.

Items 5 and 6 are based on a review of B-1 terrain following system data.

4.14.2 Autothrottle Design

The selected autothrottle is an engine mounted electromechanical servo originally used on the F-14 program. As shown in Figure 4.14-2, an A/C

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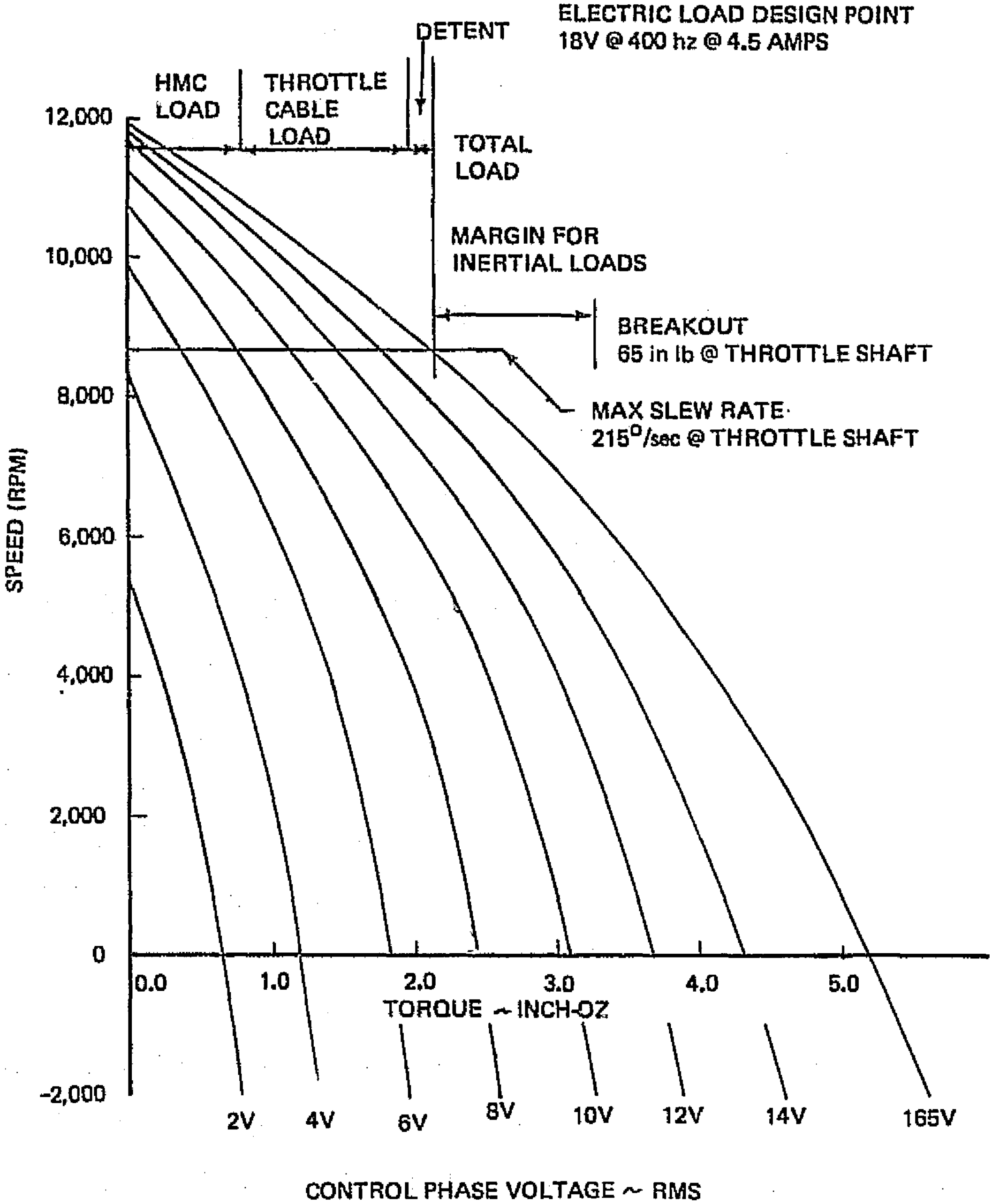

Figure 4.14-1 Typical Motor Speed Torque Curve

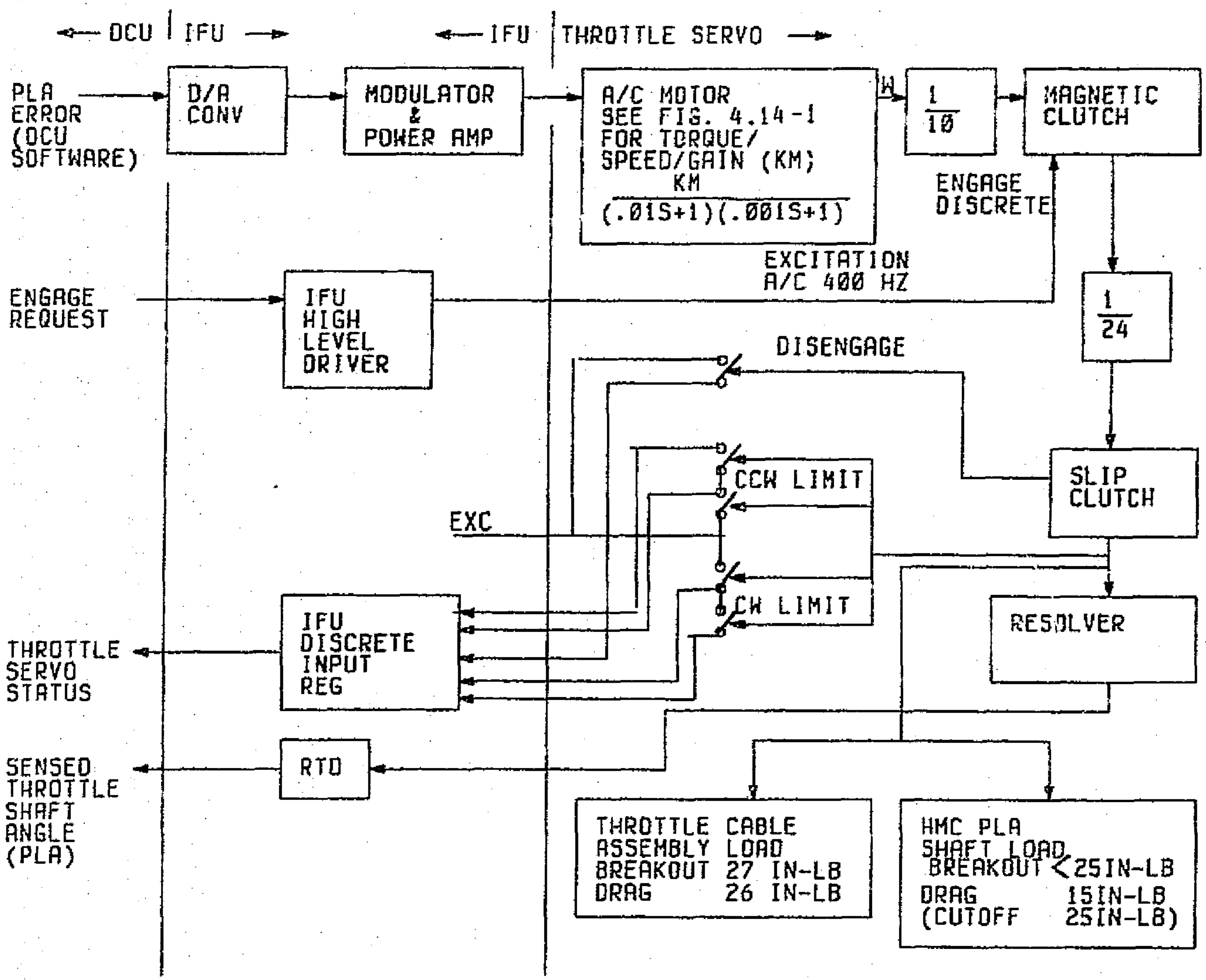

Figure 4.14-2. Autothrottle Servo Diagram

torque motor is used to drive the throttle shaft through a gear train and two clutches. Torque capability is ample to provide the required slew rate. The magnetic clutch provides pilot/DCU controlled engagement while the override disengage slip clutch system provides an automatic disengage in case of electrical system failure or gear train jam. The breakout torque is adjustable from 40-65 in. A servo analysis has not been conducted but in its F-14 application the unit operates at a significantly higher bandpass.

4.15 POWER SUPPLY (SYSTEM A)

The IPCS power supply unit (PSU) is slightly modified for the PROFIT application, see Figure 4.15-1. For IPCS a 3 phase transformer and rectifier arrangement was used to generate raw 33 VDC power for stepper motors and solenoids. Since the stepper motors are not used for PROFIT some or all of this supply may be rearranged to provide transformer isolated power to new peripherals used in PROFIT, nominally the Uplink Interface Unit, and Central Computer Interface Unit. A zener is shown across the UIU supply. Analysis will probably show this to be unnecessary. The Central Computer Interface is supplied 60 watts of phase C which is converted through simple series regulators built into the CCIF into the required CCIF D.C. supply voltages. Phase B of the 37 volt transformer is wired to the IFU for use as spare power where required. Depending on solenoid selection this may be rectified in the PSU and used exclusively to drive high current solenoids.

Table 4.15-1 presents the IPCS IFU/PSU power budget and the current estimated budget for PROFIT. Total loads are summations of worst case estimates thus the fact that margins on the $\pm$15 volt supplies are nil is acceptable.

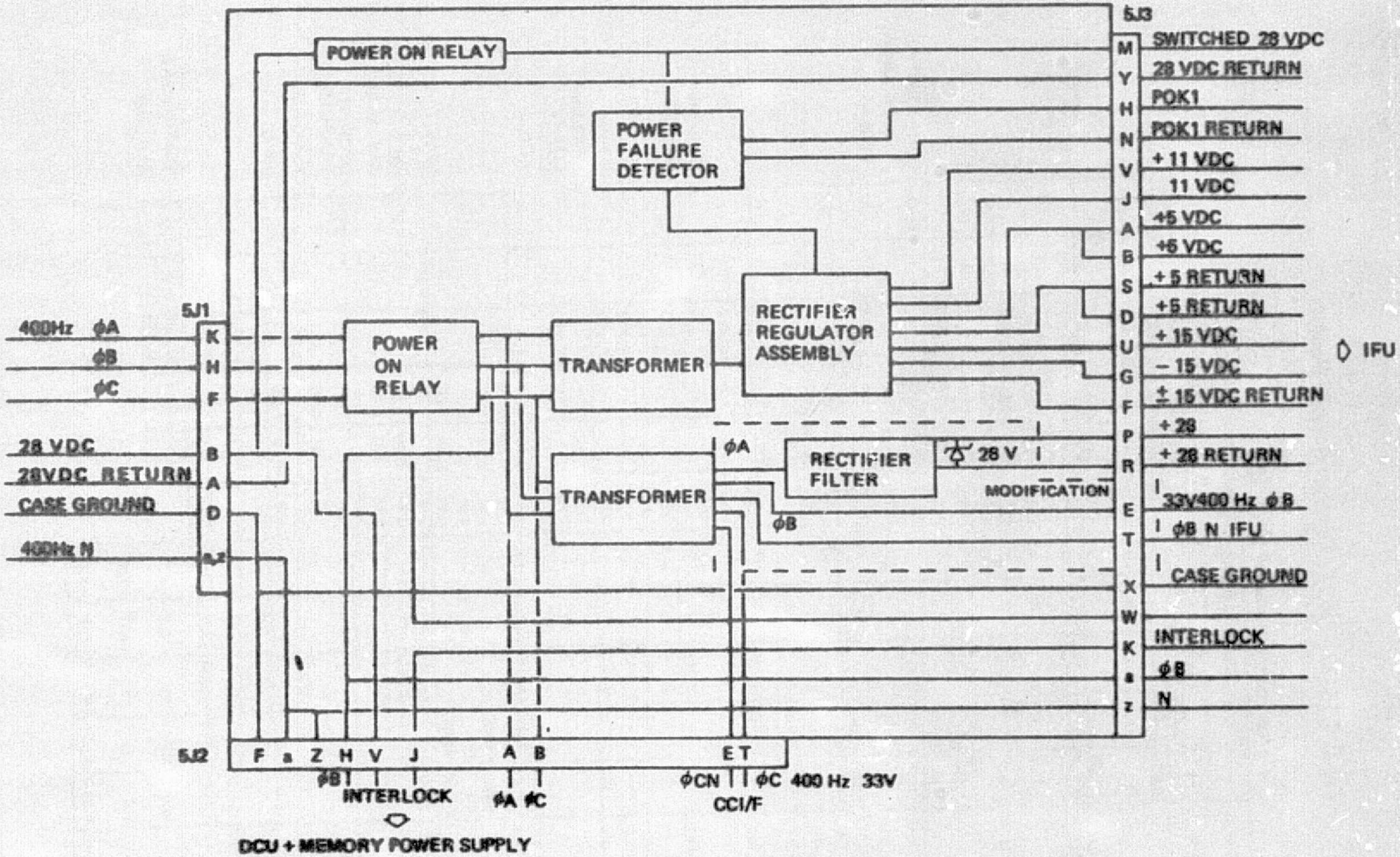

Figure 4.15-1. PSU Modification

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Table 4.15-1. *PROFIT Power Supply Budget*

CARD SLOT	CARD NO	FUNCTION	IPCS LOAD SUMMARY (1) LOAD CURRENT–AMPERES +15VDC	-15VDC	+5VDC	+28VDC	+33VDC	PROFIT CARDS (2)	+15VDC	-15VDC	+5VDC	+28VDC	+33VDC	
A1	686	LL MUX	0.005	0.005	–	–	–	686	0.005	0.005	–	–	–	
A2	698	MUX 16	–	–	–	–	–	698	–	–	–	–	–	
A3	686	MUX 16	–	–	–	–	–	686	–	–	–	–	–	
A4	746	HL MUX	0.005	0.005	–	–	–	746	0.005	0.005	–	–	–	
A5	742	MUX CTRL	0.170	0.170	0.360	–	–	742	0.170	0.170	0.360	–	–	
A6	690	A/D CONV	0.025	0.025	0.6	–	–	690	0.025	0.025	0.6	–	–	
A7	690	A/D CONV	0.025	0.025	0.6	–	–	690	0.025	0.025	0.6	–	–	
A8	692	RTDC	0.045	0.045	1.438	–	–	692	0.045	0.045	1.438	–	–	
A9	692	RTDC	0.045	0.045	1.438	–	–	692	0.045	0.045	1.438	–	–	
A10	692	RTDC	0.045	0.045	1.438	–	–	692	0.045	0.045	1.438	–	–	
A11	692	RTDC	0.045	0.045	1.438	–	–	692	0.045	0.045	1.438	–	–	
A12	694	MFC	0.15	0.15	–	–	–	D00	0.060	0.060	–	–	–	– DUAL SERVO LOOP CLOSURE (DSLC)
A13	700	SYNC DEMOD	0.230	0.060	–	–	–	700	0.060	0.060	–	–	–	
A14	698	B/T/R	0.030	0.030		–	–	698	0.030	0.030	–	–	–	
A15	696	TIGT CONV	0.025	0.025	0.5	–	–	702	0.010	0.010	0.9	–	–	
A16	702	TACH CONV	0.010	0.010	0.9	–	–	702	0.010	0.010	0.9	–	–	
A17	704	PAROS CONV	0.010	0.010	1.	–	–	704	0.010	0.010	1.	–	–	
A18	704	PAROS CONV	0.010	0.010	1.	–	–	704	0.010	0.010	1.	–	–	
A19	704	PAROS CONV	0.010	0.010	1.	–	–	704	0.010	0.010	1.	–	–	
A20	704	PAROS CONV	0.010	0.010	1.	–	–	692-1	0.045	0.045	1.438	–	–	
A21	706	DISC INPUTS	–	0.016	0.547	–	–	706-1	–	0.016	0.547	–	–	
A22	750	CABLE DR	–	–	0.414	–	–	750	–	–	0.414	–	–	
A23	SPARE	–	–	–	–	–	–	D04	–	–	2.1	–	–	– BUFFER MEMORY
A24	740	DMA DECODE	–	–	0.240	–	–	740	–	–	0.24	–	–	
A25	738	S/E LOGIC	–	–	0.345	0.1	–	738-1	–	–	0.345	0.1	–	
A26	708	DMA CTRL	–	–	1.101	–	–	708	–	–	1.101	–	–	
A27	710	DIO CTRL	–	–	0.711	–	–	710	–	–	0.711	–	–	
A28	714	REC I/F	–	–	0.378	–	–	714	–	–	0.378	–	–	
A29	SPARE	–	–	–	–	–	–	D02	–	–	1.5	–	–	– CENTRAL COMPUTER CONTROL LOGIC
A30	718	RTC	–	–	1.170	–	–	718	–	–	1.170	–	–	
A31	SPARE	–	–	–	–	–	–	SPARE	–	–	–	–	–	
A32	720	AC EXC	0.366	0.366	0.2	–	–	720	0.366	0.366	0.2	–	–	
A33	722	DC EXC	0.15	0.05	0.030	–	–	722	0.15	0.15	0.03	–	–	
A34	724	DAC	0.020	0.020	0.6	–	–	724	0.02	0.02	0.6	–	–	
A35	726	MUX SAH	0.1	0.1	–	–	–	726	.1	.1	–	–	–	
A36	728	S/C DRIVE	0.025	0.025	–	–	–	D00	0.06	0.06	–	–	–	– DSLC
A37	730	DISC OUTPUT	–	–	0.410	–	–	730	–	–	0.410	–	–	
A38	732	S/M LOGIC	–	–	0.700	–	–	D00	0.06	0.06	–	–	–	– DSLC
A39	732	S/M LOGIC	–	–	0.700	–	–	D06	0.05	0.05	–	–	–	– CAS MODULATOR
A40	SPARE		–	–	–	–	–	SPARE	–	–	–	–	–	
A41	736	S/M SWITCH	–	–	–	–	1.	D08	–	–	1.5	–	–	– COCKPIT PANEL I/F
A42	736	S/M SWITCH	–	–	–	–	1.	D00	0.06	0.06	–	–	–	– DSLC
A43	744	SO-1 DRIVE	–	–	0.05	–	3.	744	–	–	0.05	–	3.	
A44	736	S/M SWITCH	–	–	–	–	1.	D00	0.06	0.06	–	–	–	– DSLC
A45	746	HI CUR SWITCH	–	–	0.05	3.0	–	746	–	–	0.05	3.	–	
A46	734	SOL DRIVERS	–	–	0.135	1.5	–	734	–	–	0.135	1.5	–	
IPCS CALCULATED			1.386	1.302	19.883	4.6	6	UIU CCI/F	– –	– –	1. –	– –	1. 1.3	
PSU NOMINAL LOADS			1.2	1.2	20.	4.3	5.5		1.581 –	1.597 –	26.821 5.379	4.6 0.1	6.3 2.3	PROFIT LOAD MARGINS
PSU DESIGN RATING			1.6	1.6	32.	4.7 (3)	7.6							
MARGINS			0.214	0.298	12.117	0.1	1.6							

NOTES

(1) +9VDC SUPPLY FOR MUX IS UNCHANGED FOR ALL SYSTEMS– HENCE NOT TABULATED.

(2) +11 IS DEDICATED TO D.C. EXCITATION CARD

(3) 28VDC RATING SET BY RELAY CONTACTS EASILY INCREASED IF REQD

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5.0 PROGRAM PLANS

As described in the preceding sections, two different approaches to development of a flying test bed have been considered. This section describes the program plans for these two approaches. In the first program (Section 5.1) the entire system capability is developed in one cycle. The initial research use of this system would be for flight evaluation of the AFAPL/NASA/LeRc multivariable engine control. This would be followed by a research phase in which both propulsion/flight control integration and engine control evaluation would be conducted.

The second program (Section 5.2) features a three phase approach in which a minimum system would be developed for propulsion/flight control integration work in the first phase and the necessary capability for engine and inlet control evaluation is added in a later phase of the program. The initial system, described in paragraph 2.9, consists of the research digital controllers coupled with the flight control system and autothrottles for thrust control. This system will be used for research programs involving trajectory management prior to installation of the engine and inlet control systems.

5.1 SYSTEM A DEVELOPMENT PROGRAM

The controls research facility to be developed in this program has been described in the preceding sections. The entire capability, including the uplink and control computer bus interfaces, will be demonstrated in a series of tests.

The program has been structured around the development of a digital implementation of the bill of materials control system. There are two primary reasons for taking this approach: the bill of materials system is reasonably well defined and this system sould serve as the basis of comparison for future advanced control systems. Expansion of the RDC memory to 32 K will

provide adequate capacity for co-residence of the bill of materials and advanced control modes (Section 3.3). Thus it will be possible, through the use of a switch in the cockpit, to obtain back-to-back transients for control comparisons. This will provide more reliable performance measurement than could be obtained by comparisons with data from other engines or previous testing on the same engine.

Advanced engine control modes can be developed and tested at LeRC and incorporated in the flight software for testing at DFRC. The specifications developed for the flight software will identify the location of the data base, core locations that can be used, and allowable cycle time for the advanced engine control. Thus advanced control modes could be developed and tested on NASA/LeRC hardware and incorporated in the flight software at DFRC. Only closed loop testing with the simulation to verify compatibility between the controls and the remainder of the software would be required before use on the aircraft.

Since the software could be developed without the need to return the flight engines to LeRC for testing, it is advisable to avoid a requirement to retest the engines for hardware changes. As a result, sufficient control instrumentation is included to provide for anticipated programs. This will permit evaluation of the measurements using control sensors during the tests at NASA/LeRC and the flight test. Furthermore it may eliminate the need to remove an engine to incorporate advanced controls for flight test.

The overall program schedule is presented in Figure 5.1-1. Figure 5.1-2 shows the flow of the various tasks relative to each other.

The multivariable engine control has been included in this program because it will demonstrate system operation with non-bill of materials controls and the control law development is near completion at this time. Work on the test set can begin with items such as the engine simulation and design of the hardware installation in the trailer which are not dependent upon

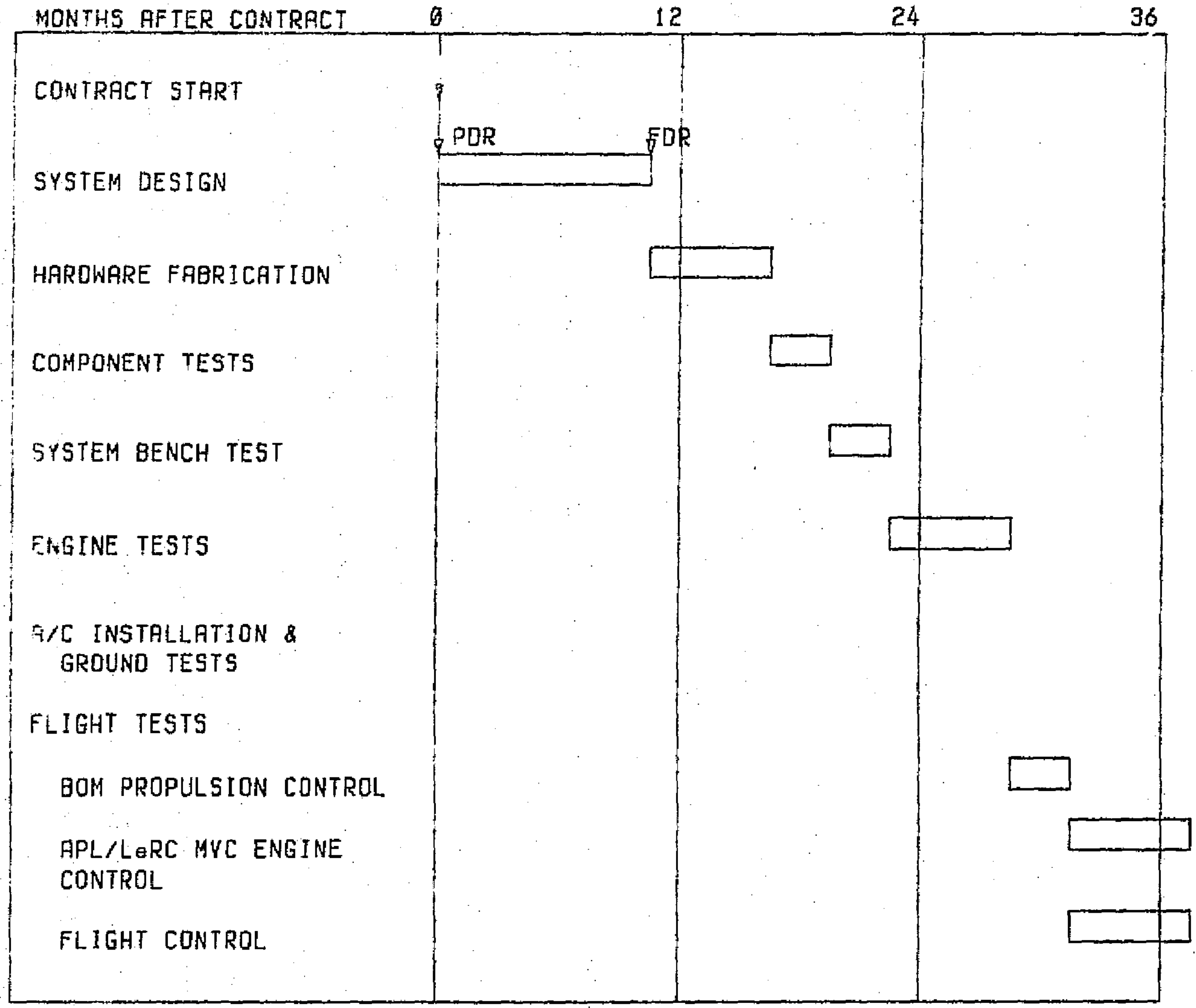

Figure 5.1-1. Program Schedule

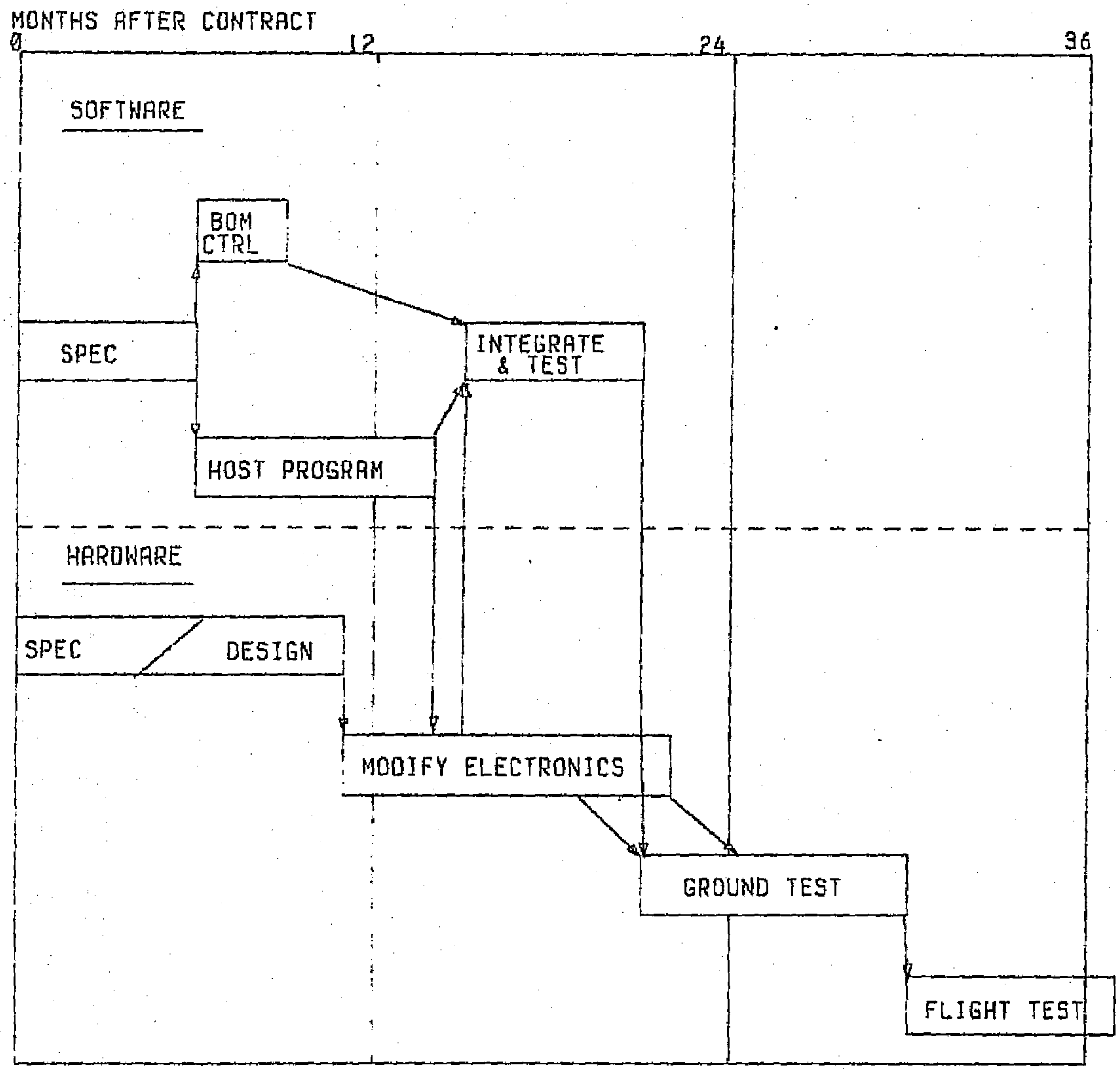

Figure 5.1-2. Development Program Flow

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the details of the final system configuration. The test sequence timing is based on the schedule achieved during the IPCS program. The following paragraphs deal with specific portions of the development plan and present more detailed schedules.

5.1.1 System Analysis and Simulation

This task consists of the development and use of simulations in the definition of system requirements. Figure 5.1-3 presents the schedule. The development of the real time engine and inlet simulations is discussed in paragraph 5.1.4.2 since they are included in the test set.

A major portion of the cycle time study has been completed (see Section 3.2). A similar study will be required for the multivariable engine control. The backup control system and the inlet/inlet control will be included in the simulation. This simulation will be used to develop the logic required for engage/disengage criteria, sensor sampling and failure detection.

Transducer accuracy requirements must be defined and sensors selected. This must be completed by PDR as sensor selection will have some impact on the IFU design.

A comprehensive iron bird simulation facility will be developed at DFRC. This facility, described in Section 2.8, will be used by all the F-15 flight test programs. As a result it will be developed as a DFRC capital facility.

5.1.2 Engine Hardware

The engine hardware described in paragraph 2.3 is being developed by P&WA in a separate program. The design and fabrication of the first three sets of Digital Electronic Engine Control (DEEC) hardware are being performed during FY 1977 and FY 1978 under the P&WA program. This hardware will be

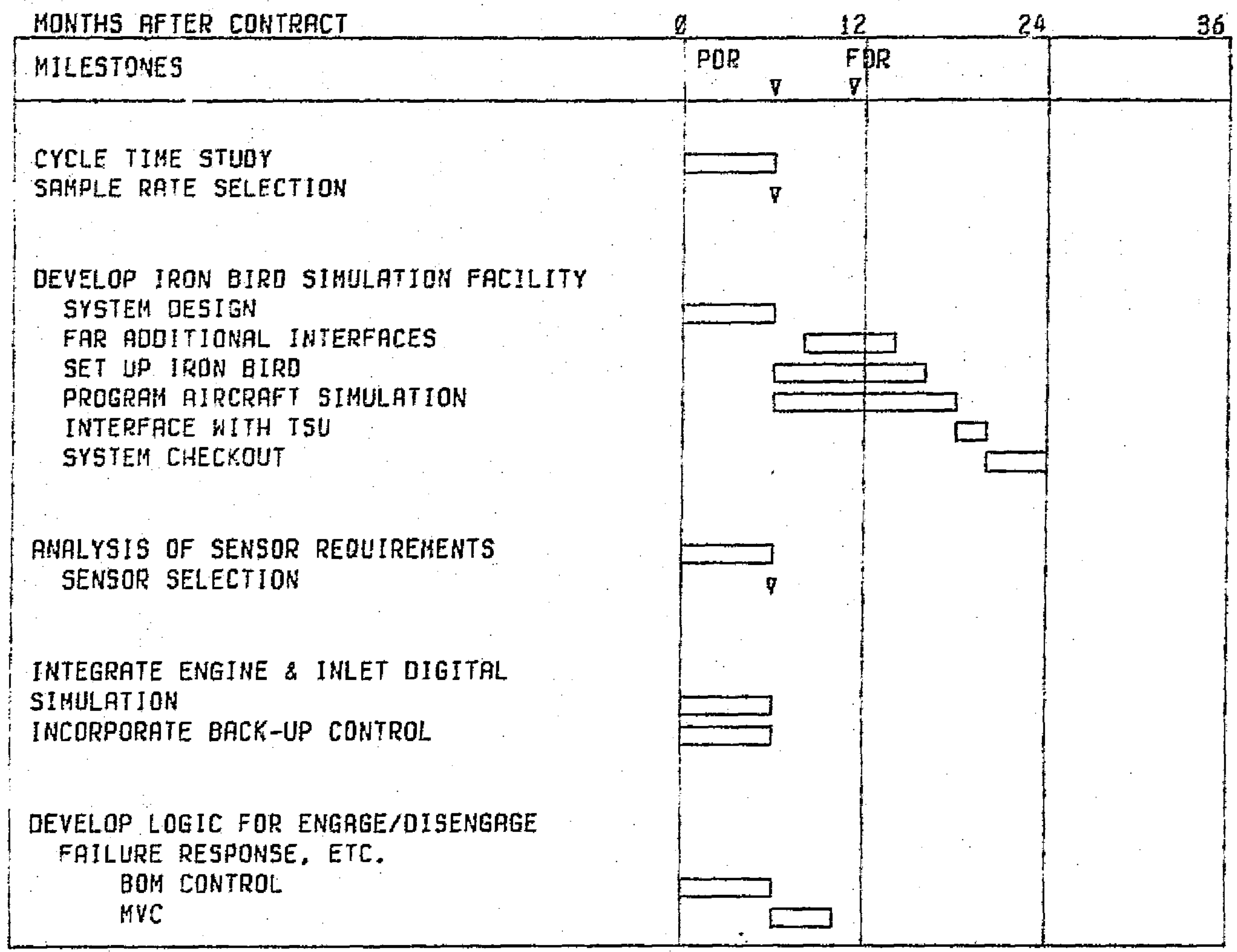

Figure 5.1-3. System Analysis and Simulation Schedule

tested by P&WA on F100 engines at sea level and at the AEDC altitude test facility prior to completion of the PROFIT design phase. The design and the results of these tests will be reviewed to ensure compatibility with the PROFIT system. Following the final design review, P&WA will be given a go-ahead to build and checkout 3 sets of hardware for the PROFIT program. The schedule is shown in figure 5.1-4.

Design and fabrication of a box for the engine pressure transducers will be done in parallel with development of the hydromechanical hardware.

5.1.3 Electronic Hardware

Development of the flight electronic hardware and the test set are discussed in this section. While these activities are closely related in the interface area, much of the test set development is in simulations. As a result the two are discussed separately.

5.1.3.1 Flight Hardware

A significant amount of the preliminary design and breadboarding of the flight hardware have been completed. Expansion of the DCU memory to 32 K using flight quality hardware has been demonstrated (paragraph 4.3.3). The majority of the required IFU modifications have been breadboarded (paragraphs 4.2.2, 4.4.2).

A major portion of the preliminary design phase will be devoted to the packaging necessary to meet aircraft installation requirements. Additional breadboards will be built during the final design phase. Lead time requirements dictate early ordering of the connectors, memories, and memory power supplies (figure 5.1-5). A final design review will be held prior to the beginning of hardware fabrication. The DCU modification will be conducted separately, starting prior to the beginning of this program.

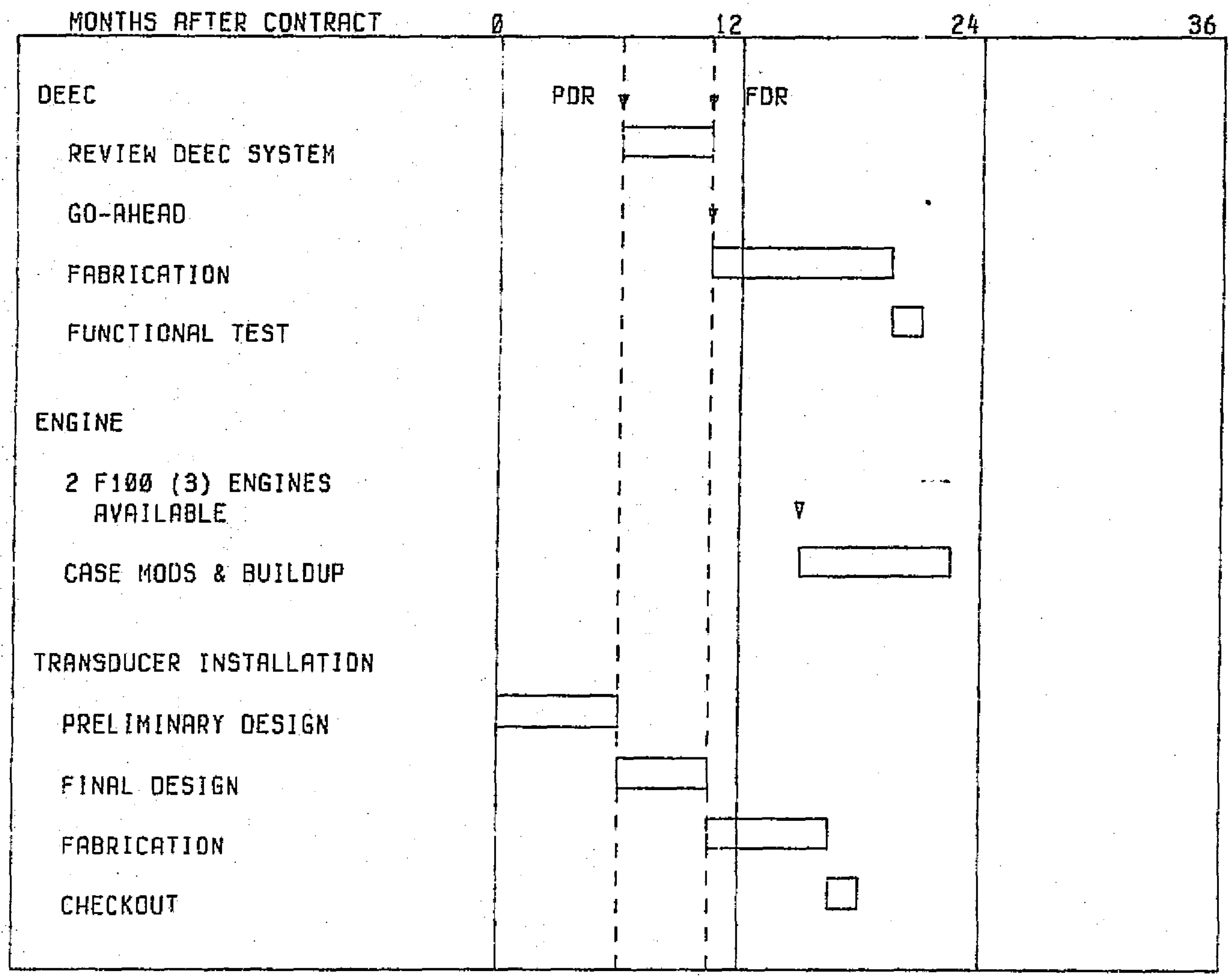

Figure 5.1-4. Engine Hardware Schedule

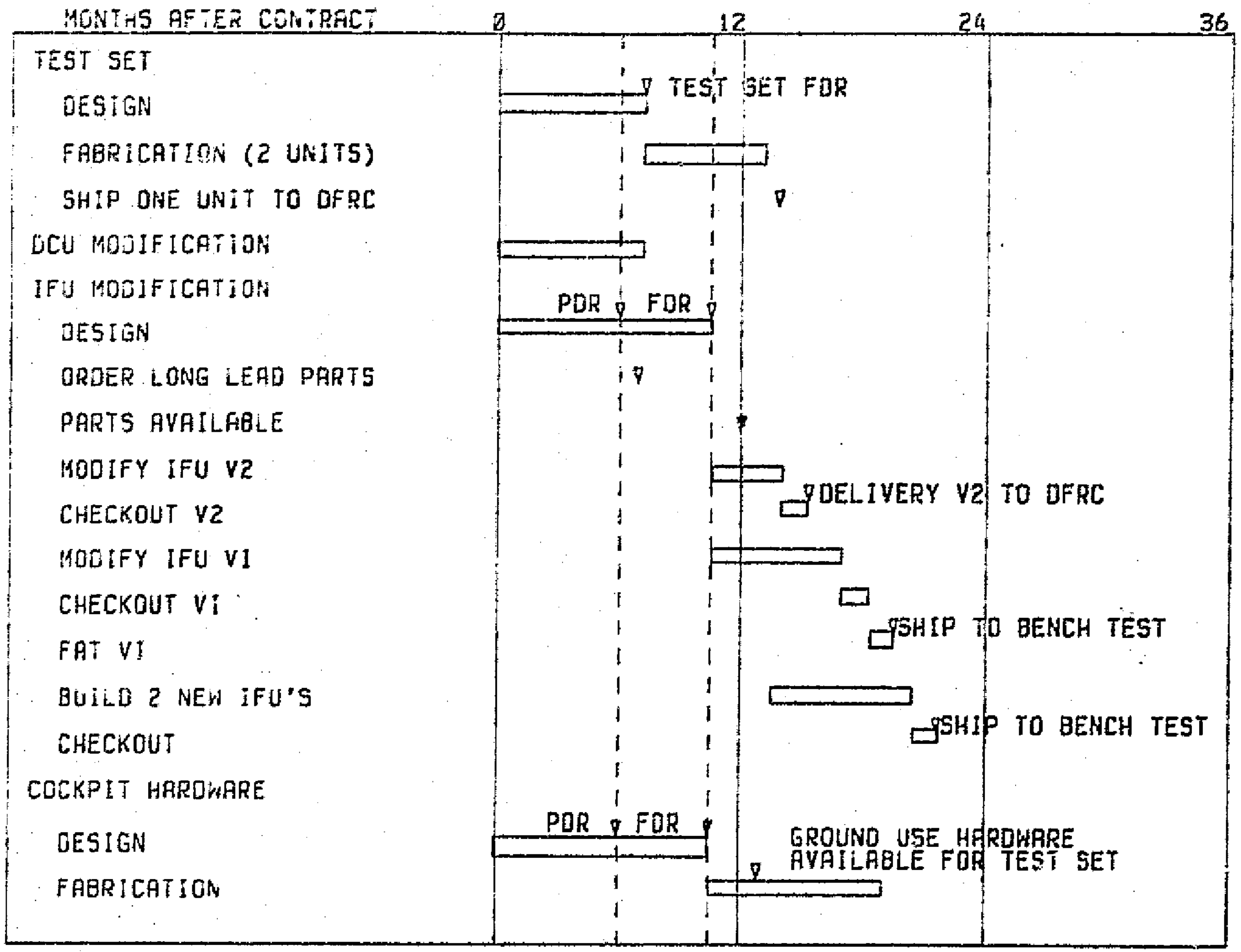

Figure 5.1-5. Electronic Hardware Schedule

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It is a requirement for the development of flight software that the DFRC simulation facility have computer hardware available essentially all the time. In addition it is desirable that the flight systems use the new IFU's and the NWC DCU's because they have fewer operating hours.

IFU V2 will be modified first and delivered to DFRC with DCU V2 for software work. This system will be delivered prior to completion of the flight assurance testing (FAT) to provide continuous software support at DFRC. The V1 system will undergo FAT after modification and start the bench test. The two new systems, using the modified NWC computers, will go to bench test as soon as they are available and proceed through the remainder of the system tests. These systems will be the primary flight units. The V1 system will be used to support engine control work at LERC following the bench test.

5.1.3.2 Test Set

Two test set systems will be built. One will be used as part of the DFRC simulation facility to provide software development and the other will support the system tests. Both will be functionally the same and use the same hardware, but only one will be packaged to be mobile.

The DFRC system, which will be a part of the iron bird simulation facility, will be checked out prior to the beginning of the integration of the PROFIT host program and engine control software (paragraph 5.1.5). The mobile test set will be installed in the trailer and checked out in time to be sent to the electronics vendor for flight hardware checkout. It will be used to validate the design changes and operation of the V1 system and sent to the bench test with the V1 system (Figure 5.1-6). One of the existing IPCS test sets will be modified sufficiently to conduct acceptance tests on the two new IFU's prior to delivery to the bench test. This avoids the cost of building another test set or shipping the DFRC system for such a short time of use. No major changes to the TSU will be required.

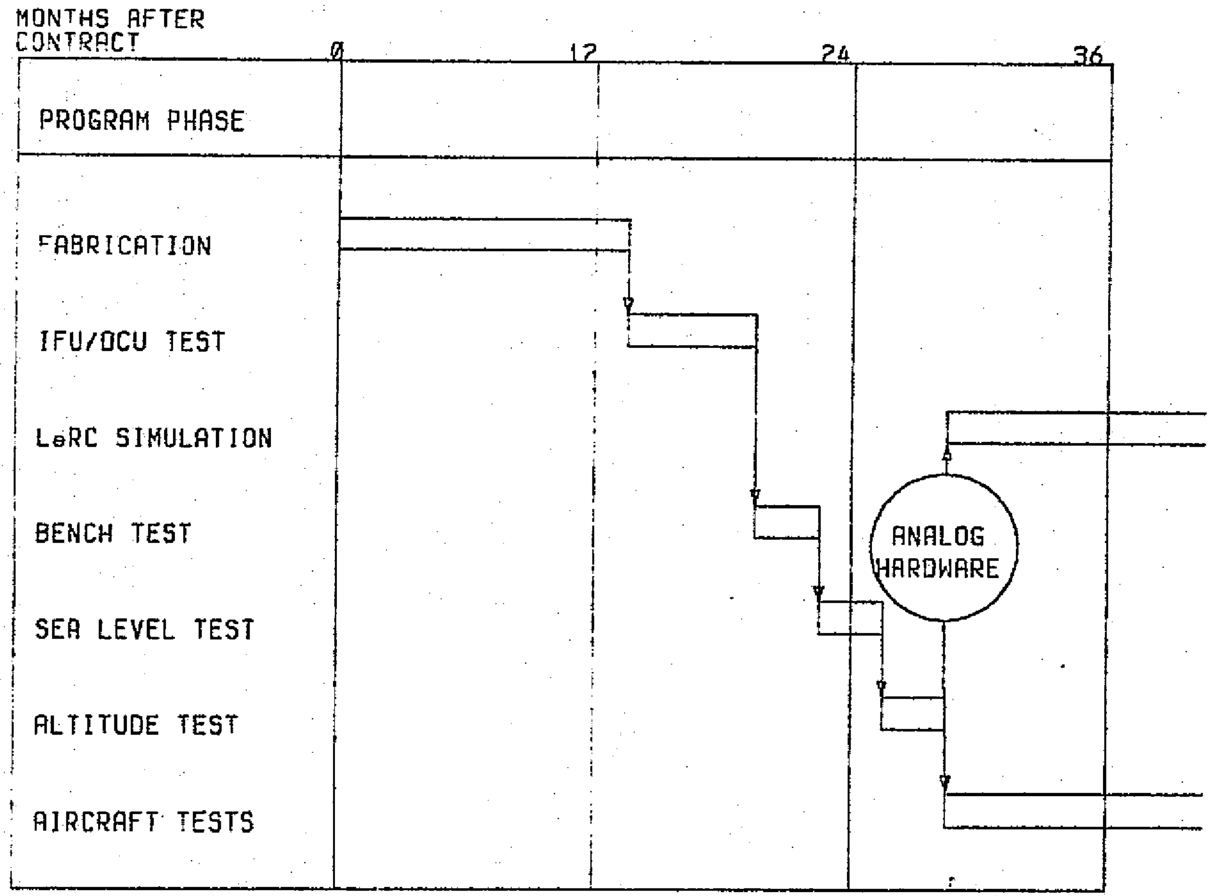

Figure 5.1-6. Mobile Test Set Flow

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The mobile test set will be used to support the system tests through the altitude test. At the conclusion of the altitude test the analog simulation hardware will be removed from the trailer for use at LeRC to support engine controls development. The trailer with the 316 computer, data interface and strip charts, simulations of the uplink and central computer interface, and other hardware necessary to run the system with an engine will be used to support ground testing at DFRC.

5.1.4 Aircraft Installation

The design of the aircraft installation will be done in parallel with the design tasks described in the preceding paragraphs (Figure 5.1-7). A decision must be made on the cockpit design either to use a microprocessor based system design similar to the YF-12 Coop control system or to use individual analog and discrete I/O as in IPCS. Actual installation on the aircraft will not be started until the last quarter of the second year to keep the aircraft available for other flight programs. Installation should be completed in 6 months as in IPCS.

5.1.5 Control Software

Three software activities have been started. An assembler is being developed at DFRC. It will operate on the CYBER 73 computer as a batch operation accepting input source code either as cards or magnetic tape. Output will be magnetic tape which is processed on the Varian computer to produce the required paper tapes. This step is necessary because the CYBER does not have paper tape. The other two activities which are underway are the writing of a software specification for the BOM control (paragraph 3.2.1) and coding the BOM control at LeRC.

As discussed in Section 2.6 the software is modular. Different portions may be coded in different places and integrated at DFRC into a program which will be flown on the test airplane. The software specification

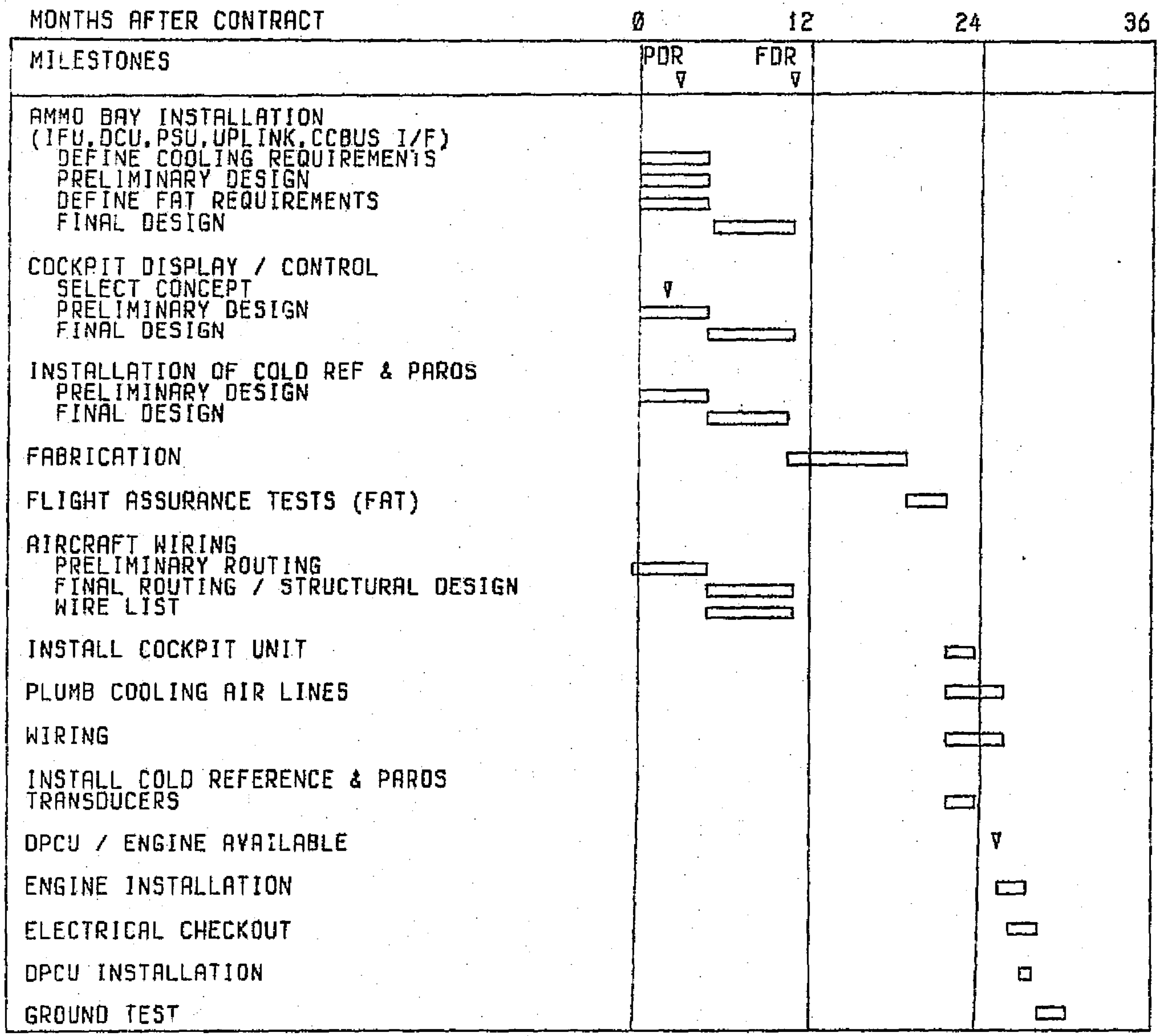

Figure 5.1-7. Aircraft Installation Schedule

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details the requirements for all portions of the software. It identifies the area of core to be reserved for advanced controls, the location of the data base and the cycle time to be allowed for advanced controls.

Prior to bench test the BOM control version of flight software will have been exercised on the engine/inlet simulation in the test set. During the system tests, changes will be incorporated in this software and it will be rerun on the dynamic simulation. New releases will then be sent to the test site for use in the test program. The schedule is shown in figure 5.1-8.

5.1.6 System Tests

A series of four system tests will precede the initial flight test: a bench test, a sea level static test, an altitude test, and a ground test of the system installed in the aircraft. This sequence has been demonstrated to be effective in minimizing the problems encountered during the flight test program. Figure 5.1-9 presents the system test schedule.

The movement of engines through test series is the key to the program (Figure 5.1-10). The first set of engine control hardware tested at bench test will be used on the first engine at sea level. This engine will be used in the altitude test.

The second set of hardware and engine will be briefly tested at SLS and installed in the airplane during the altitude test. This reduces the calendar time required for the tests and results in the engine with much less ground test time in the airplane. The final test for the #1 engine is a SLS test of the multivariable control on the Edwards SLS stand. Following this test the engine will be available for engine control tests at NASA/LERC.

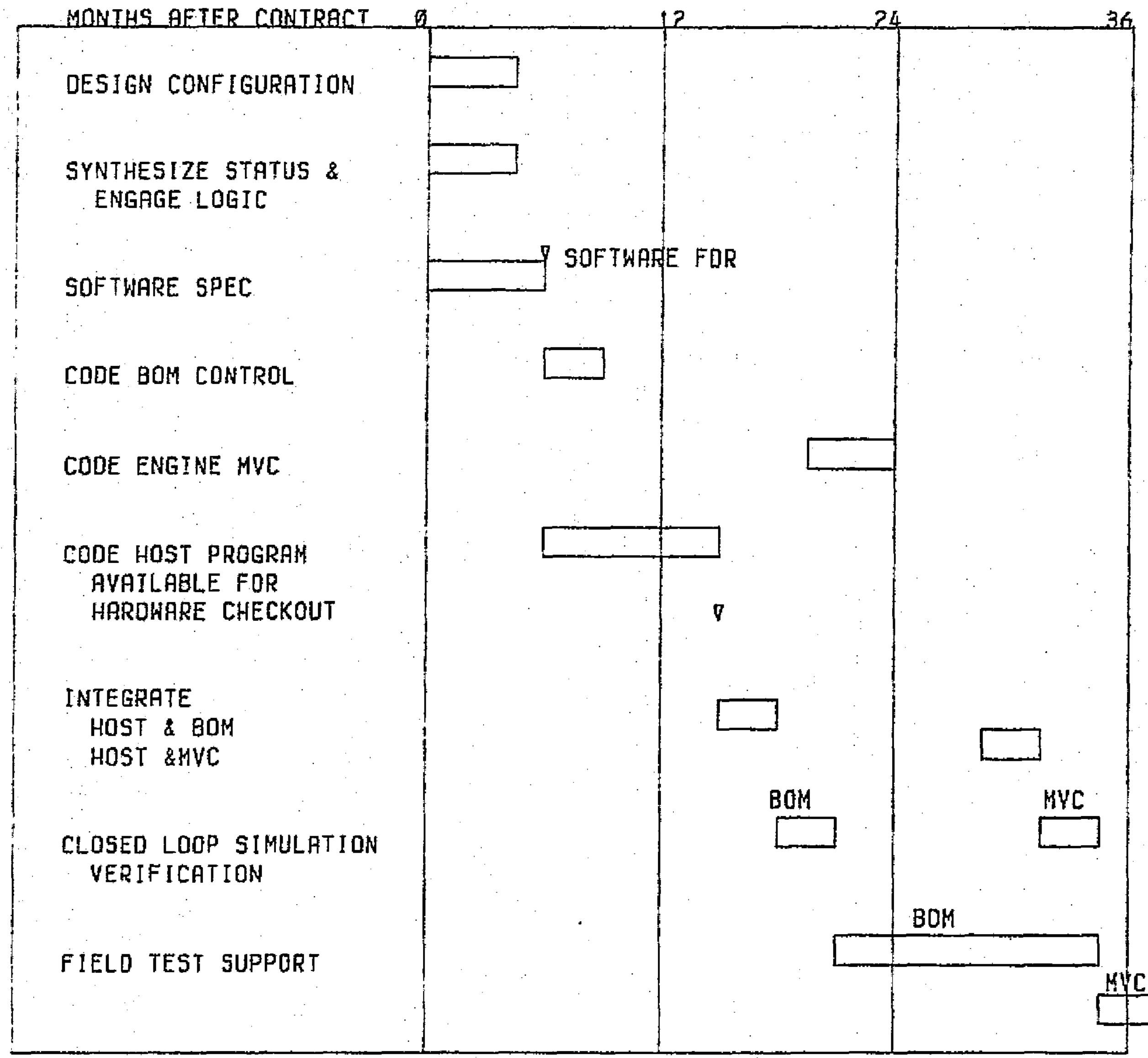

Figure 5.1-8. Software Development Schedule

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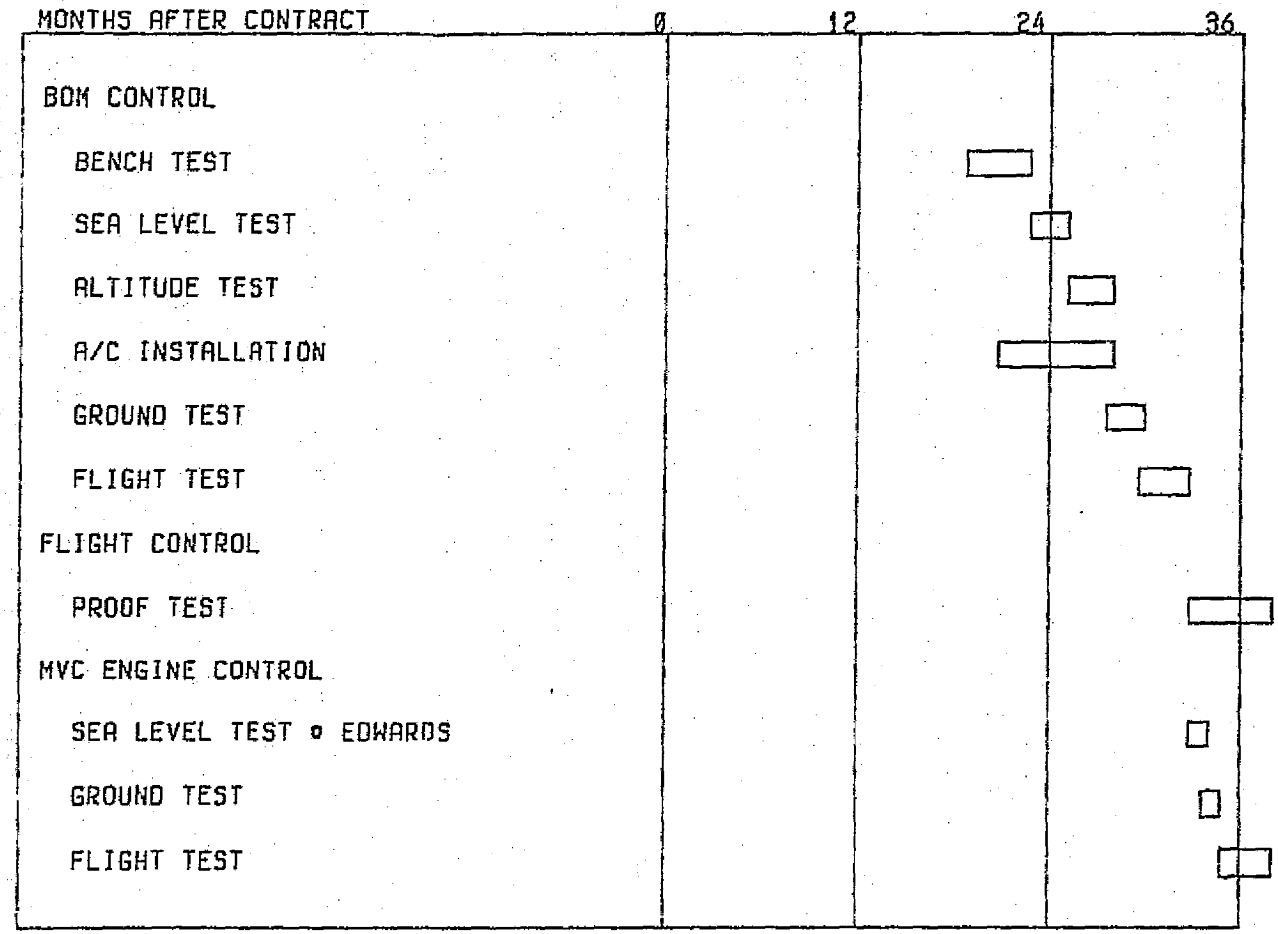

Figure 5.1-9. System Test Schedule

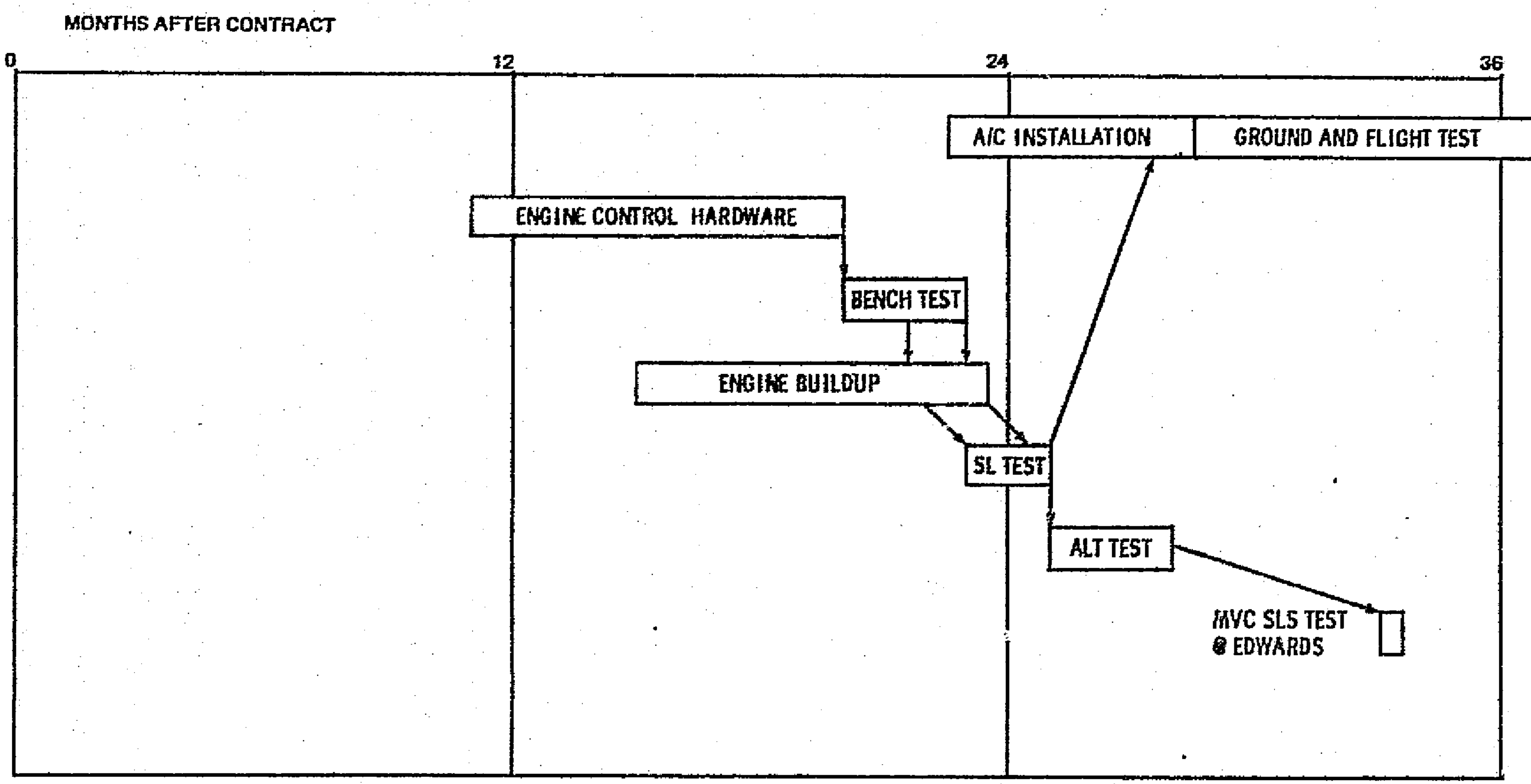

Figure 5.1-10. Test Engine Flow

Data processing, described in Section 2.7, and software support will be essentially the same for the entire test series. During the tests, engineers will support the software on-site. The necessary changes will be made in the form of patches generated on-site. Toward the end of the test, the program will be recompiled to incorporate the accumulated changes. As in the IPCS program, this new program tape will be tested prior to the end of the test.

The following paragraphs discuss each of the tests. The ground test of the installed system is treated as a portion of the flight test program.

5.1.6.1 Bench Test

The objective of the bench test is to verify proper operation of the control hardware and software with the entire system functioning together. The software previously will have been tested using the DFRC closed loop simulation and the engine hardware design will have been tested extensively as part of the P&WA DEEC program. Thus the primary emphasis of the bench test will be on the various system interfaces.

The engine mounted control hardware will be operated with fuel flows representative of operation on the engine. The engine and inlet will be dynamically simulated and all sensors and actuators in the engine and inlet controls will either actually be operated or will be electrically simulated. The controller will be run over the full range of operation. All I/O interfaces will be calibrated carefully to ensure hardware compatibility. Successful completion of the bench test will provide good confidence that the system can be run at SLS.

5.1.6.2 Sea Level Static Test

The purpose of the sea level test will be to verify the operation of the modified engine control hardware and DPCU and demonstrate the software.

The test at sea level will provide the necessary system verification under conditions where the engine operation is well understood. Both engines will be tested. The tests will provide assurance that the systems are safe to be installed and operated in the altitude facility and the airplane. The sea level static testing will be conducted at the Air Force test stand at WPAFB.

Sensor calibrations will be an important part of the sea level static test. A careful calibration of the temperature sensors will be conducted prior to the sea level test. In this calibratior a DPCU sensor will be placed in a controlled flow with a reference sensor. An equivalent to the flight cable configuration will be used to connect the control sensor to the DPCU. Using this system a calibration can be made including the effects of interfacing with the DPCU and heating of the cable. All pressure lines will be equipped with a connection which can be used to pressurize che transducer. All transducers will be calibrated over the full range prior to the initial engine run and periodically during the test.

During the testing, facility instrumentation will be used in parallel with control sensors to provide additional calibration. Where practical double thermocouple probes will be used for temperatures and tees will be incorporated in pressure sensing lines. During the intial steady engine running these data will be used to develop calibrations for all control sensors. A similar set of data will be taken near the end of the test to determine any shifts in calibrations.

The testing on each engine will be divided into two periods - an engineering evaluation of the system followed by an acceptance test witnessed by the appropriate government quality assurance organization.

Sufficient data will be recorded to permit evaluation of engine performance with the control modifications.

The data will be analyzed to ensure that the engine is in satisfactory condition before further tests are conducted.

The engineering evaluation of DPCU control will include a steady-state performance calibration from idle to maximum afterburning and the following throttle transients:

- idle-intermediate
- intermediate-idle
- idle-max
- max-idle
- intermediate-max
- max-intermediate
- intermediate-idle-intermediate bodie

In addition to the testing under DPCU control, reversion to the backup control will be demonstrated at a number of throttle positions. It is during the engineering evaluation that the necessary troubleshooting and corrections will be made to achieve satisfactory control performance. The acceptance tests will provide the assurance that the system is safe to install in the airplane and the altitude cell.

5.1.6.3 Altitude Test

The altitude test will be conducted in the altitude facility at NASA/LeRC. The purpose of the testing will be to demonstrate satisfactory system operation at conditions simulating the entire flight envelope. A common set of conditions will be used in the initial analysis and simulation work, the altitude test, and the flight test. Figure 3.2-1 presents a similar set of conditions for the F100 engine generated for the LeRC multivariable control.

As with the sea level test calibration will be an important part of the initial testing. The first testing will be at the Mach 1.4, 40000 ft condition. This condition corresponds to 80^0 and approximately 0.5 Reynolds number index. At this condition a steady-state power line will be tested from ground idle to intermediate. This will provide data for calibration of the control sensors relative to facility instrumentation. If during the course of testing there is an indication of sensor problems, testing at this conditions can be repeated to differentiate between sensor shifts and condition related problems.

The testing at each flight condition will consist of a steady-state powerline from idle to maximum afterburning and the same series of throttle transients as were conducted in the sea level test. The resulting data will be compared with data from the closed loop simulation testing performed at DFRC using the flight software.

5.1.6.4 Flight Testing

Installation on the aircraft will begin with the necessary wiring and plumbing as described in paragraph 5.1.4. Prior to the system installation all wiring and plumbing will be checked out.

The wiring and plumbing required for operation with two systems on the aircraft will be installed and checked out at this time. Only the left hand PROFIT system will actually be flown during the early tests.

A series of tests will be conducted with the PROFIT system operational prior to any engine running. These tests will include calibration of all sensors and tests of the data acquisition system, the uplink, and the central computer bus interface. The ground engine tests will largely duplicate the sea level tests.

The purpose will be to identify and correct any installation related difficulties. The final engine run will provide verification that the system is ready for flight test. A high speed taxi test will follow the final verification engine run. The data handling portion of the test set will provide on line data display during the ground tests.

The initial flight test series will be devoted to testing the BOM engine and inlet controls. The uplink and central computer bus interface will be tested during this series for data transmission, but are not expected to be part of the actual control operation. The testing will consist primarily of a series of throttle movements designed to provide the same six throttle transients used in the sea level and altitude tests. Conditions throughout the flight placard will be tested with emphasis on matching the conditions tested in the altitude test. The data will be compared to the results of the altitude test and data from running with the closed loop simulation.

The second series of flight tests will be devoted to a demonstration of the effectiveness of the RDC operation of the flight control system. In this testing progressively higher g maneuvers will be conducted throughout the flight envelope, subject to any placard restrictions.

The multivariable control will be evaluated in parallel with the flight control proof test.

Initially a short ground test of the MVC will be conducted on the Edwards SLS test stand. This test will be run to ensure safe operation of the MVC when it is tested on the airplane. The test will be run using the #1 engine which was tested at altitude test. This avoids disturbing the engine/control system installed in the aircraft. The only data support required during this test will be on line use of the test set data handling system.

Once the SLS testing has been completed successfully, the MVC version of the software will be loaded into the flight computer and a ground test which largely duplicates the BOM control ground test will be conducted. The MVC control flight test will also duplicate the BOM test. At this point the system will be ready for integrated controls testing described in paragraph 5.1.7.

5.1.7 Integrated Controls Testing

The integrated controls research is clearly less well defined at this time than the facility development. Figure 5.1-11 presents a schedule in terms of months after contract award for the development program. The most significant thing to note is that program definition and contractor selection must begin early in the development program to provide a flight system in a timely manner. There may be parallel development of several integrated control schemes by different contractors and different government agencies. Each new control will go through the same development program prior to flight test.

The first phase is the development of the control laws. This will include analytical design of the controls and verification of the modes operating on suitable dynamic simulations. During this phase any requirement for hardware modification will be identified and the necessary design work completed. The next phase is software generation. The PROFIT software specification must be revised to incorporate a detailed specification of the research control software. The research control modes are coded and then integrated into the PROFIT software at DFRC.

The schedule allows time for a sea level test at Edwards following the multivariable engine control test and an altitude test at NASA/LeRC. Unless significant changes are made to the engine control these tests would not be needed. There is sufficient time between the end of the multivariable engine control flight test and the beginning of the ground test to install any modified hardware in the aircraft.

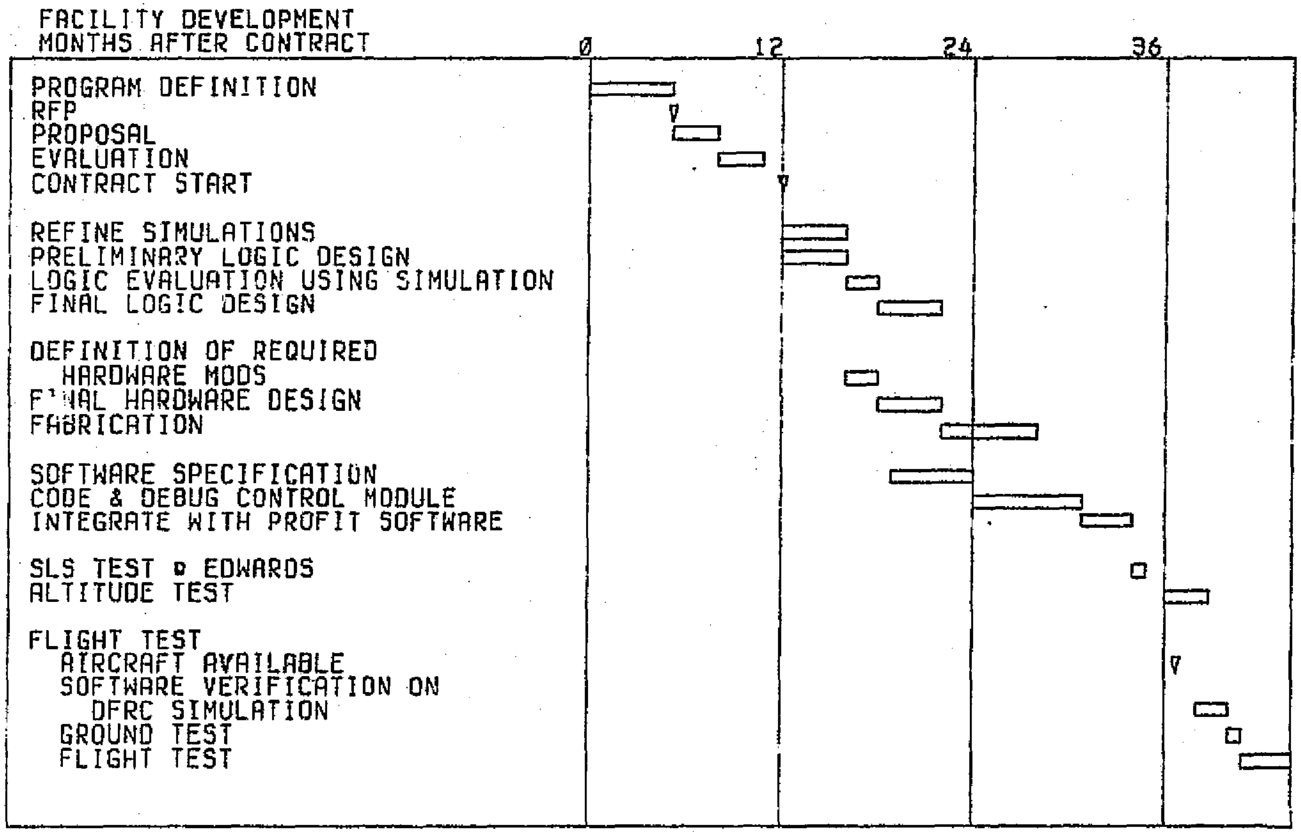

Figure 5.1-11. Integrated Controls Research Schedule

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For each research control the final step is verification of proper operation of the software on the DFRC iron bird simulation facility. A short ground test of the entire flight system is required prior to the beginning of the flight testing.

5.2 PROGRAM PLAN - SYSTEM B

The program for system B consists of three phases - Development, Trajectory Management, and Propulsion Control. The schedule overview for the whole program is presented in figure 5.2-1. The Development Phase (paragraph 5.2.1) consists of modifying the RDC to interface with the central computer bus, CAS, uplink, and auto throttle; developing the necessary software to checkout the system; installing the system in the airplane; and conducting a series of flight tests. This system will have the capability to provide inputs to the flight control surfaces through the existing CAS and to the engines through the autothrottles. The Trajectory Management Phase (paragraph 5.2.2) at the moment consists of a flight evaluation of different terrain following algorithms using simulated terrain and radar. The configuration demonstrated in the Development Phase will be used without modification other than software changes. This phase could be expanded to include energy management or engine diagnostics programs if sufficient time is available prior to the start of propulsion control testing.

The third phase, Propulsion Control (paragraph 5.2.3), begins concurrently with the Terrain Following Phase. In this phase the system will be expanded to include full authority electronic control of both inlets and the left hand engine. The phase consists of fabrication of the engine control hardware, the propulsion servos and the IFU modification to interface with the propulsion servos and data bus, development of propulsion control software, a series of bench and engine tests, and flight testing.

At this point the engine control hardware has not been defined completely. There is a possibility that the Navy developed FADEC engine control computer

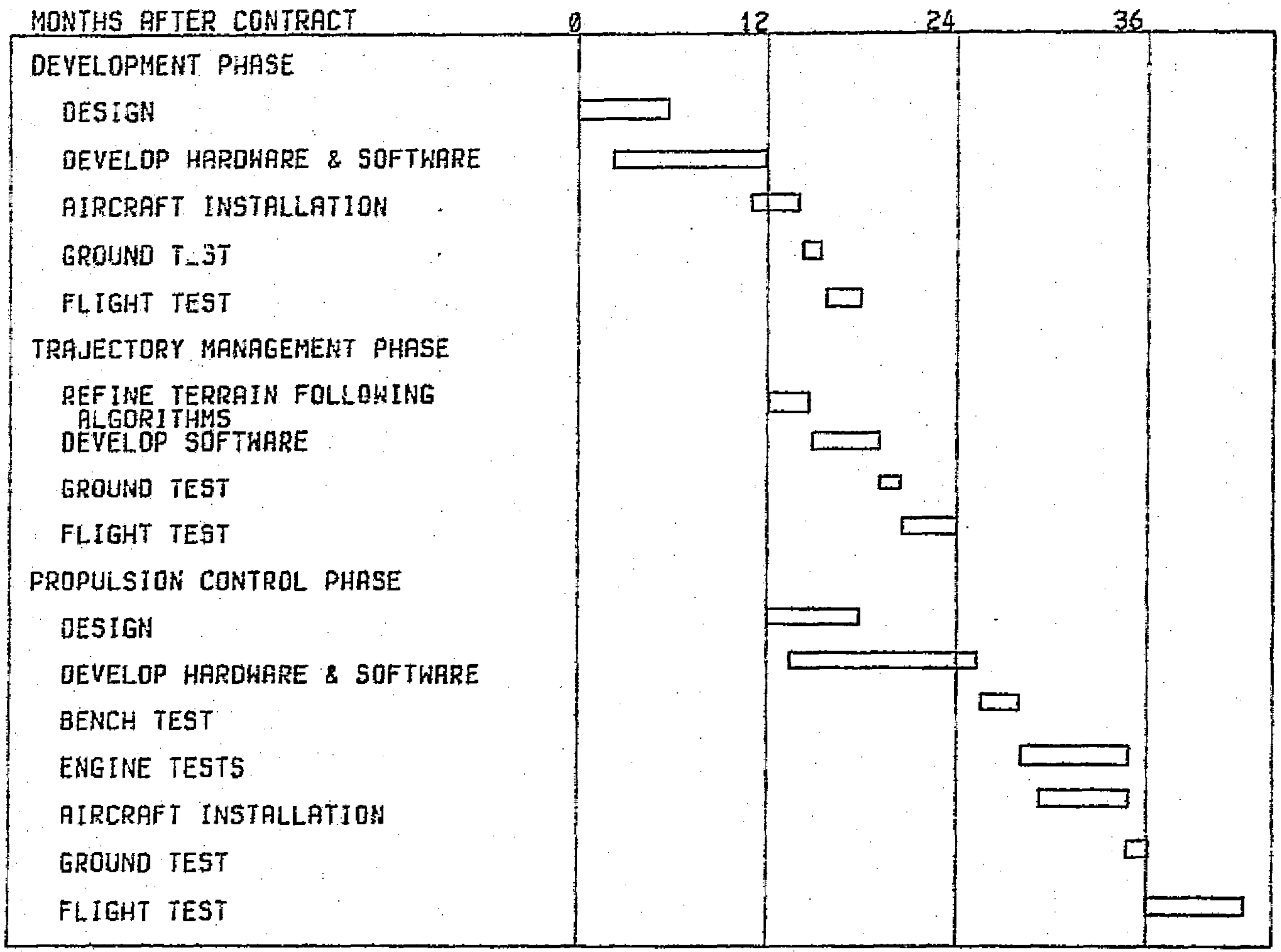

Figure 5.2-1. System B Schedule Overview

will be used. There are several possible engine interface configurations. To minimize the impact of the uncertainty about FADEC, the candidate configurations will work with or without FADEC. The major decision is whether to include engine servo loop closures in the IFU. The recommended approach is to output commanded servo positions on a data bus and close the servo loops either in FADEC or an external servo box. In the alternative approach servo loop closure would be included in the IFU along with the data bus connection to FADEC.

With either approach the program schedule is not greatly dependent upon the FADEC decision. It is anticipated that the BOM and MVC controls will be co-resident and tested together during the flight test program.

The program has been structured to minimize requirements for fabrication of additional computers and interface units. Only two flight worthy systems will be used in the program (figure 5.2-2). Initial software support will be provided by the existing 32k IPCS DCU. The Development Phase flight system will consist of this DCU, the other IPCS DCU expanded to 32k and 2 modified IPCS IFUs. The flight system will be used in the simulation facility for software verification and then installed in the aircraft.

All cards of the (2) Naval Weapon Center (NWC) machines will be upgraded to 32K configuration for use as spares. In addition, one NWC machine will be upgraded to the 32K configuration using lab power supplies, for use in software development. To the extent required a lab special IFU will be built to interface with the simulation facility.

In the Propulsion Control Phase the flight IFUs will be modified to include the MIL-1553A data bus. During engine testing the two flight units will be used on-site, one to control the engine and one with the on-site simulation (para. 4.5). Both systems will be installed in the aircraft for flight testing.

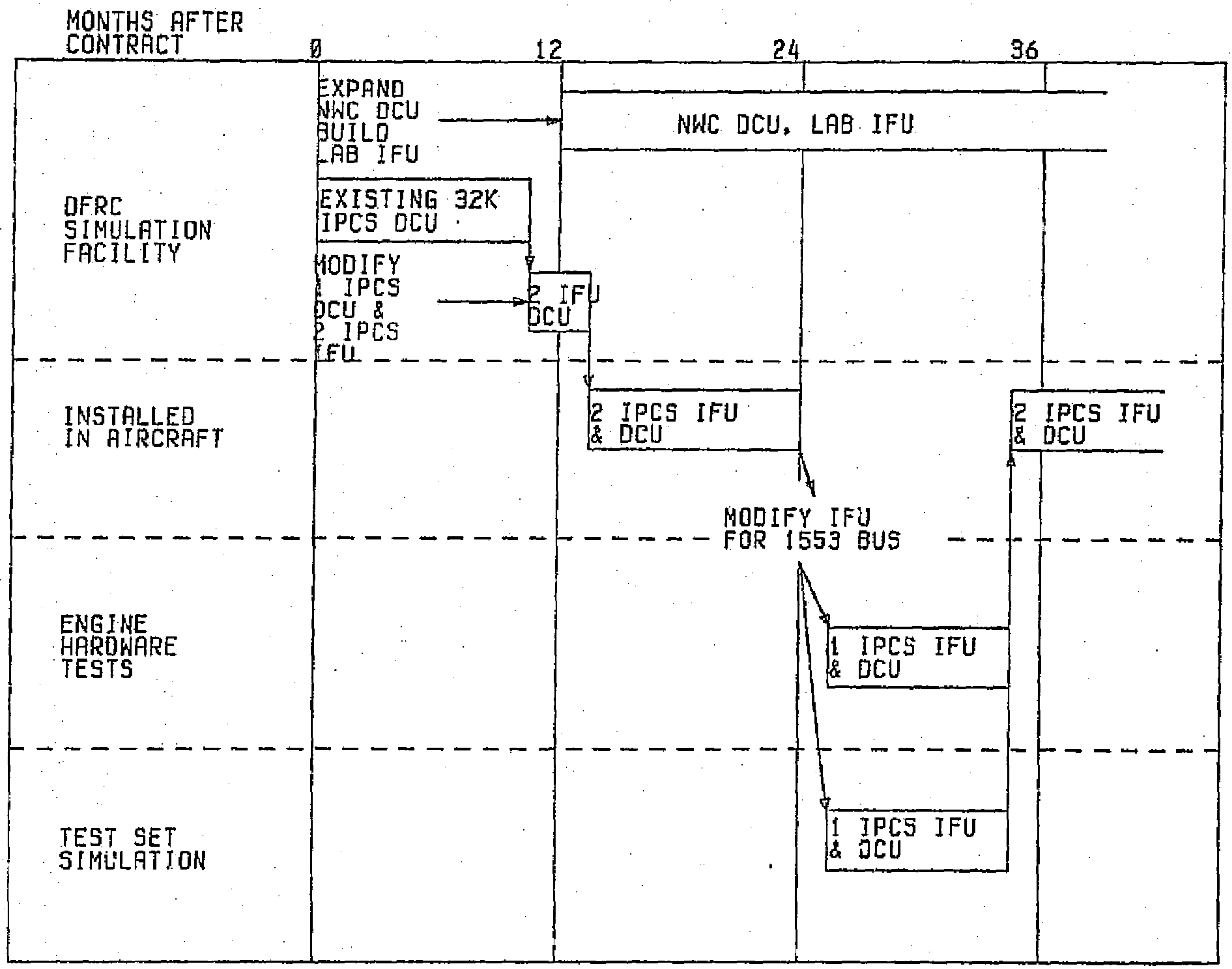

Figure 5.2-2. DCU/IFU Flow - System B

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Throughout the program the requirement for spares will be met with the spare boards from the second NWC DCU and the spare IFU boards and components purchased under the IPCS program.

There are two major advantages of the system B approach compared to system A. The first is the reduced initial cost of the program due to delay of the fabrication of the expensive engine control hardware. The second is earlier flight testing of the PROFIT system without any significant overall program slide (figure 5.2-3).

5.2.1 Development Phase

The purpose of the Development Phase is to build and flight demonstrate a configuration capable of performing the Trajectory Management Tasks. This phase covers an 18 month period. The following paragraphs discuss specific portions of this phase.

5.2.1.1 Design

The design will be completed in the first six months (figure 5.2-4). This is possible because substantial portions of the system have been designed and tested, at least at the breadboard level. Three areas are included in the design task: Hardware design, assembler and software definition, and development of the simulation facility. It is possible that the 601 expansion to 32k will take place independently. The DAP 16 assembler is currently under development at NASA/DFRC. This should become available without any additional contract related effort. The aircraft simulation, required for the simulation facility, is also in work at NASA/DFRC. The final design review will be conducted prior to the start of hardware fabrication and software coding (paragraph 5.2.3). The one exception is the expansion of the 601 which will be started as soon as the design is finalized.

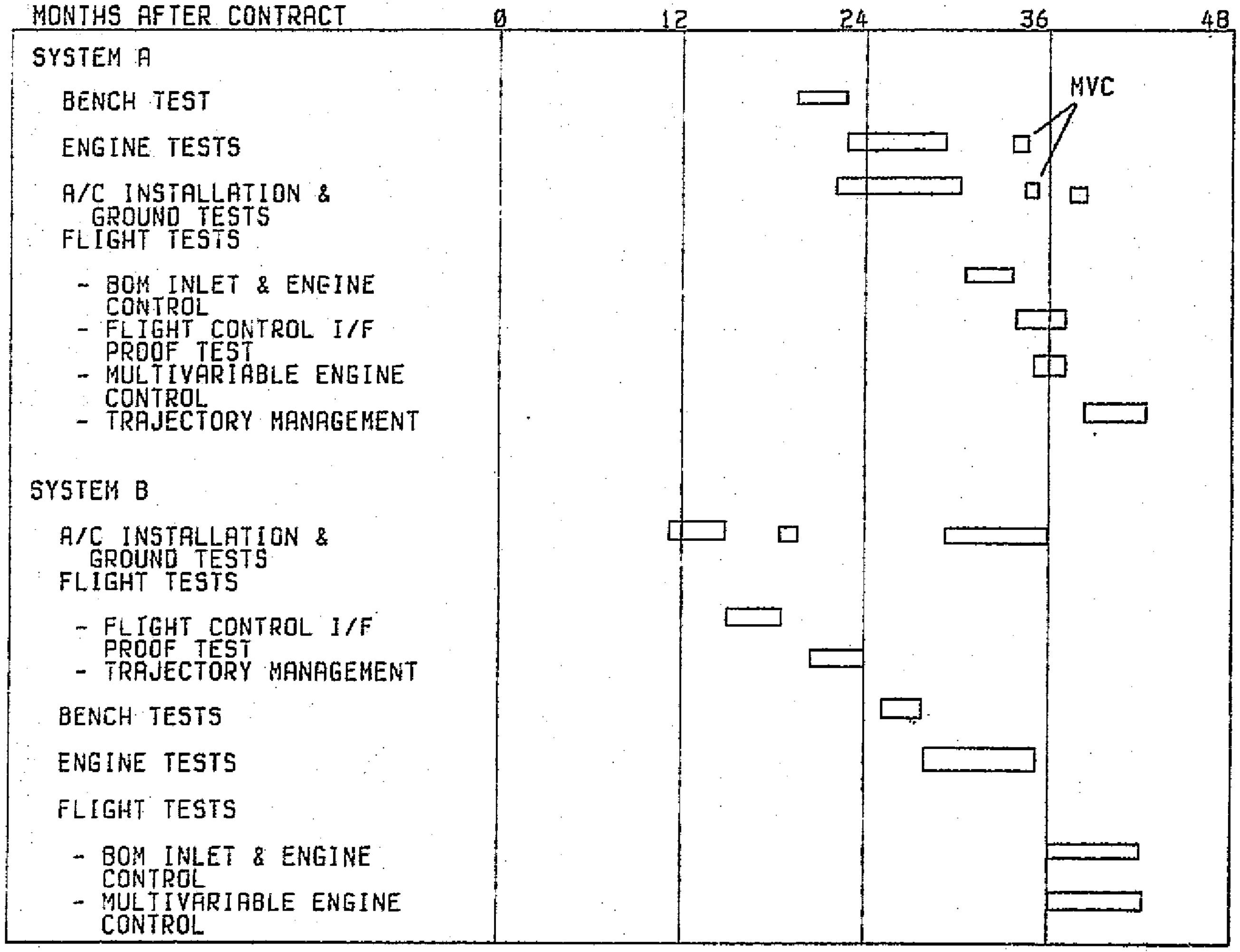

Figure 5.2-3. System Test Schedule Comparison

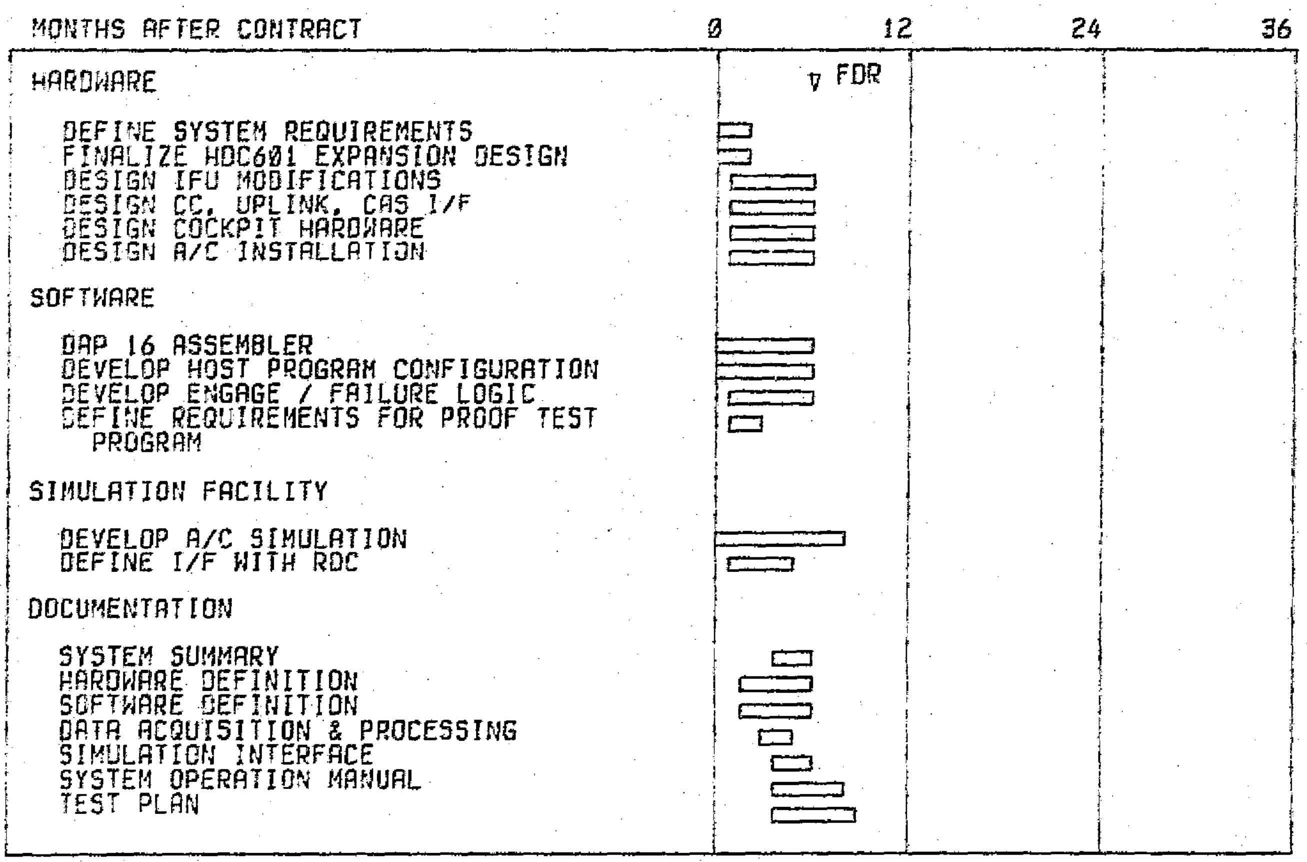

Figure 5.2-4. System Design and Documentation

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5.2.1.2 Documentation

Seven documents, identified in figure 5.2-4, are required to identify and control system configuration, operating procedures, and testing. Tables 5.2-1 through 5.2-7 define the scope of these documents. Subsystem level test procedures are contained in the relevant definition documents. Plans and procedures for system verification on the simulation facility, the aircraft ground test, and the flight test are contained in the Test Plan Document (Table 5.2-7).

5.2.1.3 Fabrication and Installation

The expansion of the 601 computers to 32k will be the first item in the fabrication effort (figure 5.2-5) unless it is performed under a separate contract. This work can begin prior to FDR since the requirements are well defined and are not dependent upon details of the system design. The two IPCS units will be modified to be the flight worthy computers. One of the NWC DCUs will be expanded using lab power supplies to provide a 32K unit for the simulation facility. If changes to the 32K IPCS DCU, created during the current program, are required, they will be made after one of the other 32K computers is available. This will provide required computer capability for software development.

The two IPCS IFUs will be modified to the configuration described in section 2.9. These will be the flight IFUs. The interface between the DCU and the simulation will be built as special lab hardware. The required additional interface boxes will be built and checked out at the same time.

The software will be coded while the simulation facility is being completed. Initial checkout of the software can be done on the available DCU.

The aircraft installation will consist of mounting 2 RDCs in the weapons bay along with the necessary plumbing to provide cooling air, installation

TABLE 5.2-1

PROFIT SYSTEM SUMMARY DOCUMENT

- o RESEARCHER ORIENTED
- o CONTAINS A BRIEF SUMMARY OF:
  - * SYSTEM CONFIGURATION
  - * SYSTEM CAPABILITY
- o USED FOR:
  - * TRAINING
  - * MANAGEMENT COORDINATION

TABLE 5.2-2

PROFIT HARDWARE SYSTEM DEFINITION DOCUMENT

- o CONTROLS ALL SYSTEM INTERFACES
  - * AIRFRAME
  - * FLIGHT CONTROL SYSTEM
  - * ENGINE
  - * DATA SYSTEM
  - * SOFTWARE (RDC INTERFACE)
  - * EXPERIMENTS
- o DOCUMENTS SUBSYSTEM & COMPONENT CHARACTERISTICS/CONFIGURATION
  - * DPCU
  - * HYDROMECHANICAL COMPONENTS
  - * UPLINK
  - * CENTRAL COMPUTER BUS
  - * AFCS
  - * EXPERIMENTS
- o DEFINES SUBSYSTEM TEST PROCEDURES
  - * REFERENCE EXISTING ONES
  - * INCORPORATE NEW ONES

TABLE 5.2-3

PROFIT SOFTWARE SYSTEM DEFINITION DOCUMENT

- CONTROLS RDC SOFTWARE CONFIGURATION
- DEFINES REQUIREMENTS
- DOCUMENTS CURRENT CONFIGURATION
  * DATA BASE
  * EXECUTIVE
  * EXPERIMENTS
- DEFINES SOFTWARE DEBUG PROCEDURES

TABLE 5.2-4

PROFIT DATA ACQUISITION AND PROCESSING DOCUMENT

- o DEFINES SYSTEM REQUIREMENTS
- o DESCRIBES SYSTEM OPERATION
- o CONTROLS SYSTEM CONFIGURATION
    - * DATA FLOW
    - * HARDWARE CONFIGURATION
    - * HARDWARE I/F
    - * SOFTWARE CONFIGURATION
- o DEFINES DATA SYSTEM TEST PROCEDURES

TABLE 5.2-5

PROFIT SIMULATION INTERFACE DOCUMENT

- o DEFINES INTERFACE REQUIREMENTS
- o CONTROLS INTERFACE CONFIGURATION
- o DEFINES TEST PROCEDURES

TABLE 5.2-6

PROFIT SYSTEM OPERATING MANUAL

- o DESCRIBES SYSTEM OPERATION
- o USED FOR REFERENCE, TRAINING

TABLE 5.2-7

PROFIT TEST PLAN DOCUMENT

- o CONTAINS
  - * OBJECTIVES
  - * TEST PLANS
  - * DETAILED PROCEDURES
- o THREE TESTS
  - * SYSTEM VALIDATION ON SIMULATION
  - * GROUND TEST
  - * FLIGHT TEST

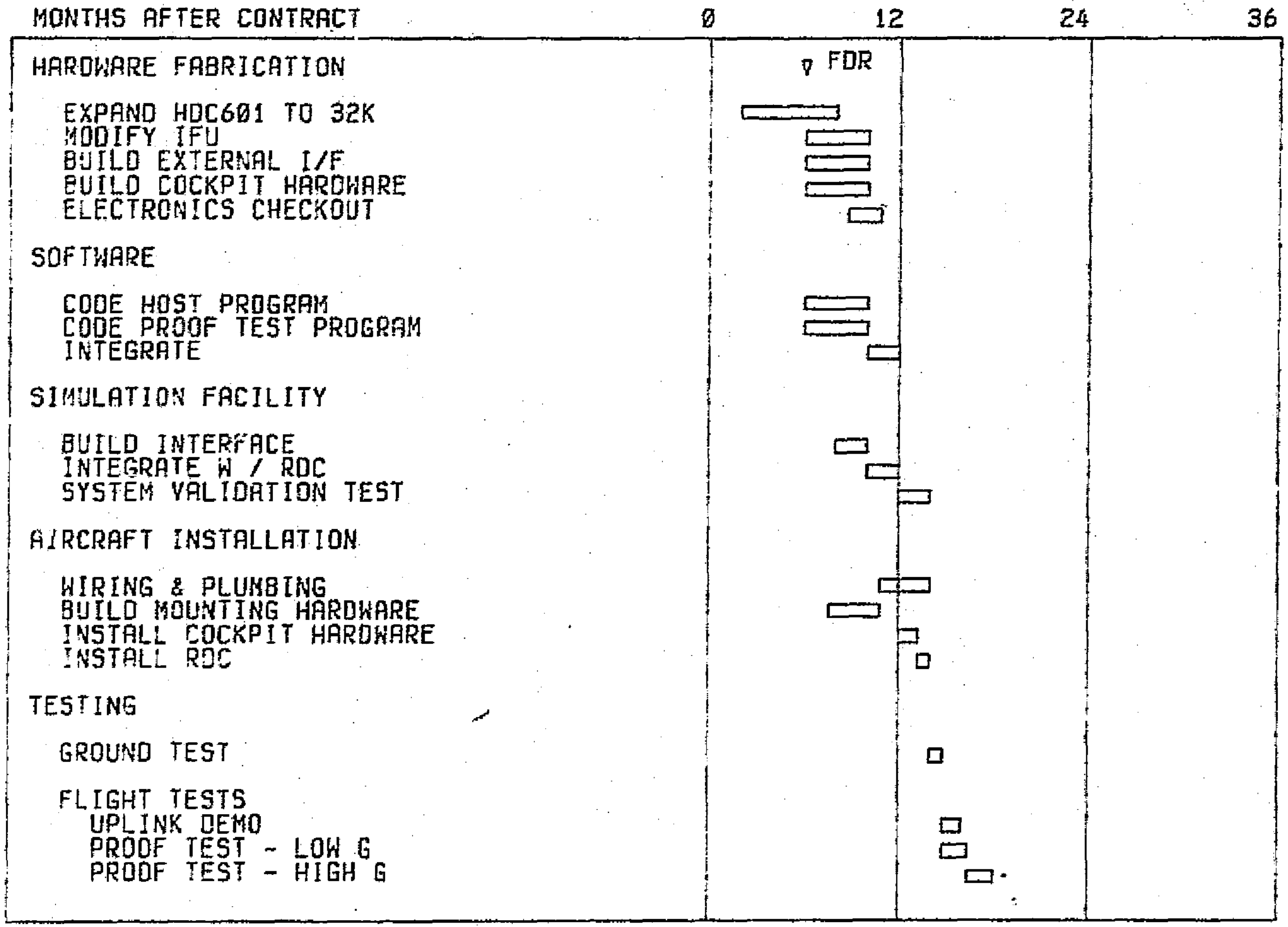

Figure 5.2-5. System Fabrication and Testing

of the cockpit hardware, and the wiring to supply power to the system and interconnection between subsystems installed on the aircraft. The additional wiring to accommodate inlet control and engine control will not be installed until the Propulsion Control Phase.

5.2.1.4 System Testing

Three system level tests are planned: system verification using the simulation, a ground test of the system installed in the aircraft, and the flight test.

The system verification test will couple the flight electronic hardware to the aircraft simulation and simulated cockpit. The planned flight test program will be conducted and the aircraft/controller performance evaluated. Any necessary corrections will be made before the system is allowed to proceed to ground test.

The purpose of the ground test is to identify and correct any installation related difficulties. The testing will be conducted using aircraft power. A comprehensive EMI investigation will be performed. A test program, included in the host program, will exercise the various interfaces.

The flight test program will be performed to demonstrate the capabilities of the system to control the aircraft through the CAS interface and control the engines through the autothrottle. In the initial testing various preprogrammed aircraft and engine transients will be executed. During this testing the uplink will be active, but the output will be used only to evaluate performance of the uplink. Cockpit switches will be used to initiate and terminate the transients. The initial transients will be small and gradual. As confidence in the system grows, progressively more severe maneuvers will be conducted. In the final phase of the testing coordinated propulsion/aircraft maneuvers will be conducted with commands coming up the uplink. The successful completion of the flight testing will demonstrate that the system is satisfactory for the Trajectory Management Phase.

5.2.2 Trajectory Management Phase

The program initially identified for this phase is terrain following. The schedule is presented in figure 5.2-6. The intent of this program is to select two different terrain following algorithms and use a flight evaluation to determine their relative merits. The evaluation would be in terms of ability to follow a simulated terrain and estimated effect on engine life. Two likely candidate algorithms are currently under development or available:

1. Calspan Adlats
2. Boeing Optimal Integrated

The flight testing will be conducted over a simulated terrain with the aircraft flying about 10,000 ft. Aircraft postion relative to a simulated terrain will be determined and the control will be given inputs which simulate the terrain following radar. Thus, the algorithms can be evaluated independently of the radar installation.

The first quarter will be devoted to algorithm selection, definition of the breakdown between on board and ground computation, and detailed definition of the ground and flight software. Coding will take place in the second quarter, followed by integration with existing software and facility. As in the Development Phase the final flight software will be validated with the ground test prior to the start of the flight tests.

5.2.3 Propulsion Control Phase

During this phase the PROFIT system will be modified to provide full authority control of both inlets and the left hand engine. It consists of development of hardware and software, a series of system tests from a closed loop bench test through altitude testing of an engine, and flight testing. This phase is quite similar to the early portion of the development of system A. The following paragraphs duscuss specifics portions of the activity.

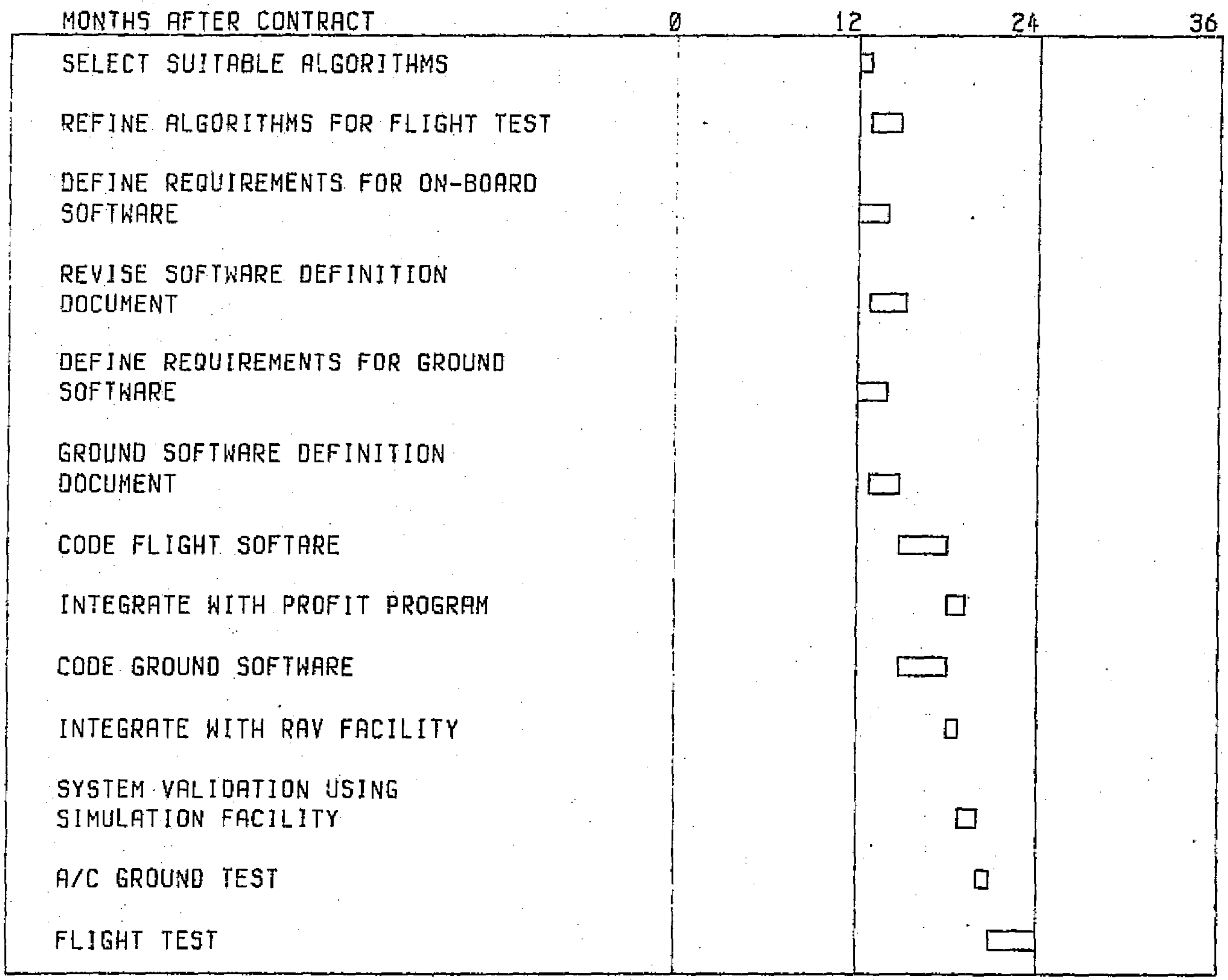

Figure 5.2-6. Trajectory Management Phase Schedule

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5.2.3.1 Design & Documentation

A series of design reviews are conducted to provide timely availability of hardware and software (figure 5.2-7). The hardware preliminary design period will be devoted to system definition, sensor selection, and determination of sample rate requirements. The software FDR is early to provide sufficient coding time and meet the test schedule requirements. The short time is reasonable because the software requirements are well understood and the host program will be developed on earlier program phases. It is anticipated that current NASA simulation activities will have yielded a batch version of an inlet/engine simulation prior to the beginning of the Propulsion Control Phase.

With the exception of the Test Plan, the documents produced in the Development Phase will be updated to reflect the system being built in this phase. Since the testing is relatively different from the previous phases a new test plan will be written for the Propulsion Control Phase. It will cover the system validation, bench test, sea level static test, altitude test, ground test and flight test.

5.2.3.2 Fabrication

Since the DEEC hardware will be developed and tested prior to this program, fabrication can be started at the beginning of the propulsion control phase (figure 5.2-8). The schedule assumes a significant amount of instrumentation will be added to the engine during buildup. Otherwise less time would be required. This schedule would require an engine not on the airplane for the Trajectory Management Phase.

The majority of the electronic hardware changes are associated with interfacing with the engine and inlet. Figure 5.2-8 is based on the use of an external servo box and a data bus. Placing the servo loop closures in the IFU might require a slide of a month or two in the test schedule to accommodate the IFU rework.

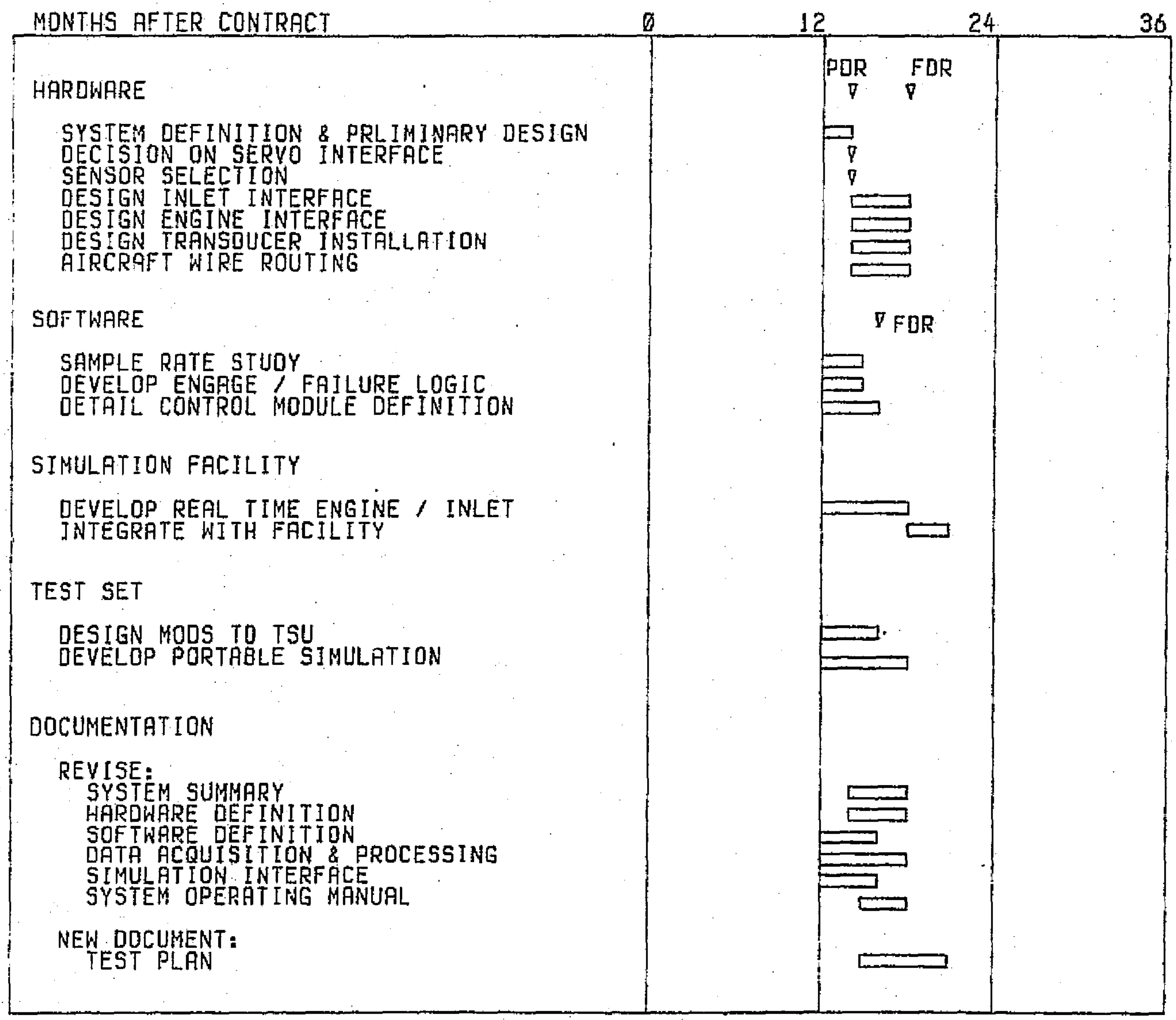

Figure 5.2-7. Propulsion Control Phase Design and Documentation

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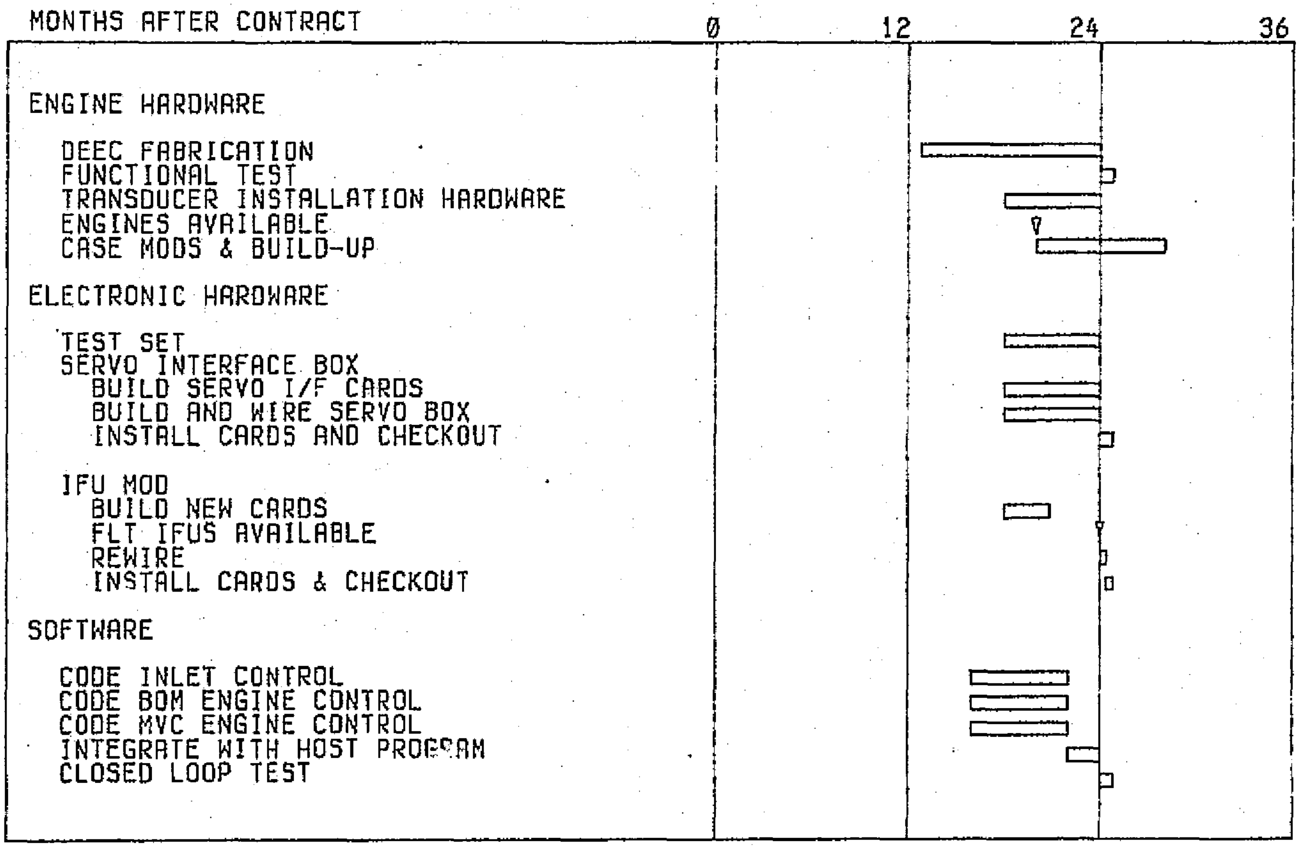

Figure 5.2-8. Propulsion Control Phase Fabrication and Checkout

5.2.3.3 Testing and Aircraft Installation

The system test sequence (figure 5.2-9) is essentially the same as described in paragraph 5.1.7 for system A. The only significant difference is in back to back testing of the BOM and MVC controls. If FADEC is a part of the system, it will be tested in parallel with the other controls.

The sea level test will be conducted on the Air Force test stand at WPAFB. The altitude test will be conducted at NASA/Lewis. The functions of the various tests are the same as those described in paragraph 5.1.7. Thus, the detailed writeups are not repeated in this paragraph.

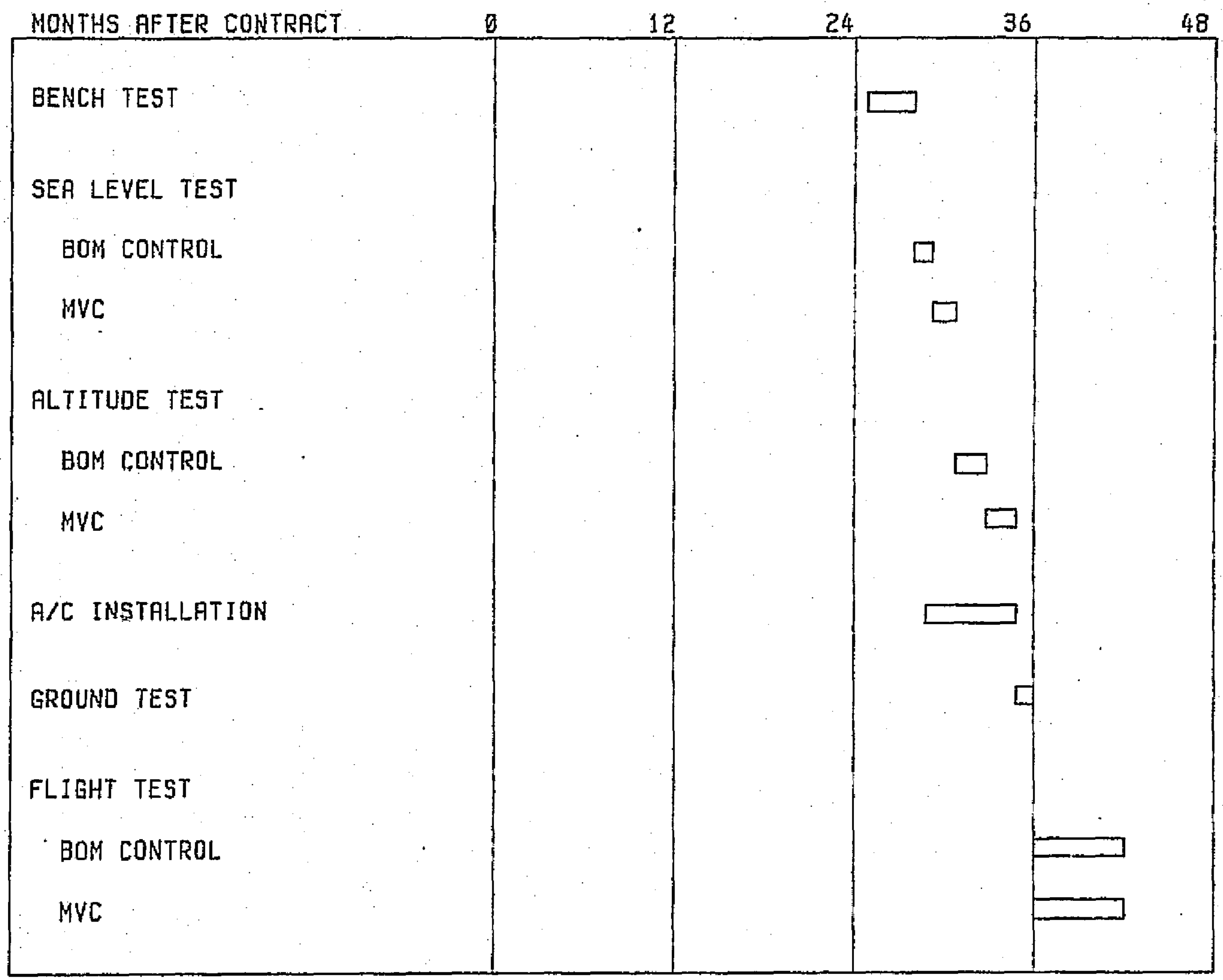

Figure 5.2-9. Testing and Aircraft Installation

6.0 CONCLUSIONS AND RECOMMENDATIONS

The overall conclusion of the design and analysis of the PROFIT system to date is that either system described in this document will provide the necessary flexibility and is feasible to build and operate. Adequate memory and computation time are available for presently planned systems and margin exists for future programs. The following recommendations are made for hardware configuration and future work.

1. A DAP 16 M2 assembler system operational on the CYBER 73 computer, is recommended for the PROFIT PROGRAM.

2. The P&WA Digital Electronic Engine Control (DEEC) hardware is recommended for the actuation, interface, and backup hydromechanical system.

3. It is strongly recommended that during engine tests the test set be configured with a spare DPCU and simulation for software checkout and the data display capability described in Section 4.5.

4. Continuing simulation studies are recommended. These should include analysis of reversion to the backup hydromechanical control, evaluation of the inlet control requirements, and study of candidate trajectory management modes.

5. Both uplink and central computer interface electronics have been defined. Packaging for these elements requires further review before a final design recommendation is made. It is recommended that any elements of these interfaces not housed in the DPCU boxes be designed and assembled at DFRC to reduce system cost.

6. Further development, optimization, and organization of the basic system cabling arrangement presented in this document is strongly recommended since it affects both hardware and software configuration decisions.

7.0 REFERENCES

1. "Integrated Propulsion Control System (IPCS) Final Report, Volume II, Technical Description," AFAPL-TR-76-61, August 1976.

2. "PROFIT Software System Definition", NASA CR144876, July 1978.

3. "Dynamic Simulation of the F100 Engine," PWA Advanced Systems Coordination Memo No. 1587, 29 November 1976.

4. "Dynamic Description of the FJ-A2 Unified Control System for the F100 Engine Lot 3," Bendix Report No. ECD-863-17682R, 1 December 1970.

5. Letter from C. P. Balderson to C. M. Carlin transmitting the Lot VII schedules dated 17 May 1977.

6. "F100 Multivariable Control System Engine Models/Design Criteria," AFAPL-TR-76-74, November 1974.

7. "Electronic Air Inlet Controller," McDonnell Aircraft Company Procurement Specification 68-870045, Rev. C, 20 February 1975.

8. "Computer Program Product Specification for the F-15 Electronic Air Inlet Controller," Hamilton Standard Report E-77-003, Rev. B, 29 April 1974.

9. Letter from H. C. Rechtien to F. W. Burcham transmitting the computer assembly language listings for the Schedule L, Rev. J, EAIC.

10. "Technical Review of the F100 Multivariable Control Program," Meeting at AFAPL, Wright-Patterson AFB, 18 January 1977.

11. "Interface of Fighter Throttle/Energy Management Functions with DAIS," AFFDL-TR-75-60, June 1975.

12. "Energy Management Techniques for Fuel Conservation in Military Transport Aircraft," AFFDL-TR-75-156, February 1976.

13. NASA Flight Research Center Process Specification No. 21-2, Flight Assurance Testing (Environmental) Electronic and Electromechanical Equipment, 24 July 1972.

14. "Technical Support of NASA F-15 Propulsion and Flight Control Studies," letter from H. C. Rechtien to T. Putnam, 15 June 1977.

15. "Operation and Maintenance Manual with Parts List for the Universal Digital Command Receiver-Decoder BCRD-31," Esterline Electronics BEC-BCRD-31-OMPL, Change 1, 9 February 1972.

16. "Technical Manual for HDC-601C Digital Computer (Operation and Maintenance)," Honeywell Aerospace Division Report 0573-11643, 16 May 1973.

17. "F-15 Digital Interface Design Specification," McDonnel Aircraft Corporation Report H009, Rev. C, 1 February 1970.

18. "Central Computer System Logic Diagrams, USAF Series F15A 73-085 and up, TF15A 73-108 and up Aircraft," TO 1F-15A-2-16-2, June 1975.

19. "Development and Verification of Real-Time, Hybrid Computer Simulation of F100-PW-100(3) Turbofan Engine," J. R. Szuch, K. Seldner, D. S. Cwynar, NASA TP 1034, September 1977.

APPENDIX A
COMPUTATION RATE STUDY PLOTS

This appendix contains plots for the dynamic simulation runs identified in Section 3.2. Table A-1 defines the plot nomenclature. With the exception of the compensated fan turbine inlet temperature and power lever angle all variables are from the engine calculations and do not include any sensor dynamics.

cf

TABLE A-1 PLOT NOMENCLATURE

VARIABLE	DEFINITION	UNITS
A/B Fuel	Afterburner fuel flow	PPH
AJ	Nozzle Area	FT^2
CIVV	Variable fan inlet guide vane position	DEG
COMP FTIT	Lead/lag compensated fan turbine inlet temperature	^oF
FAN SPEED	Fan rotor speed	RPM
FAN WCOR	Fan inlet corrected airflow	LB/SEC
FUEL FLOW GG FUEL	Gas generator fuel flow	PPH
HPC SPEED	High pressure compressor rotor speed	RPM
NET THRUST	Gross thrust - ram drag	LB_f
PLA	Power lever angle	DEG
PT4	Burner pressure	PSIA
PT6M	Compressor total pressure at the afterburner entrance	PSIA
RCVV	Compressor variable vane position	DEG
SMAF	Fan surge margin	-
SMAC	High compressor surge margin	-

METRIC CONVERSIONS

Deg F = 9/5(Deg C) +32

1 Foot = 0.3048 Meter

1 Pound Mass = 0.4536 Kilogram

1 PSI = 6.8948 Kilopascals

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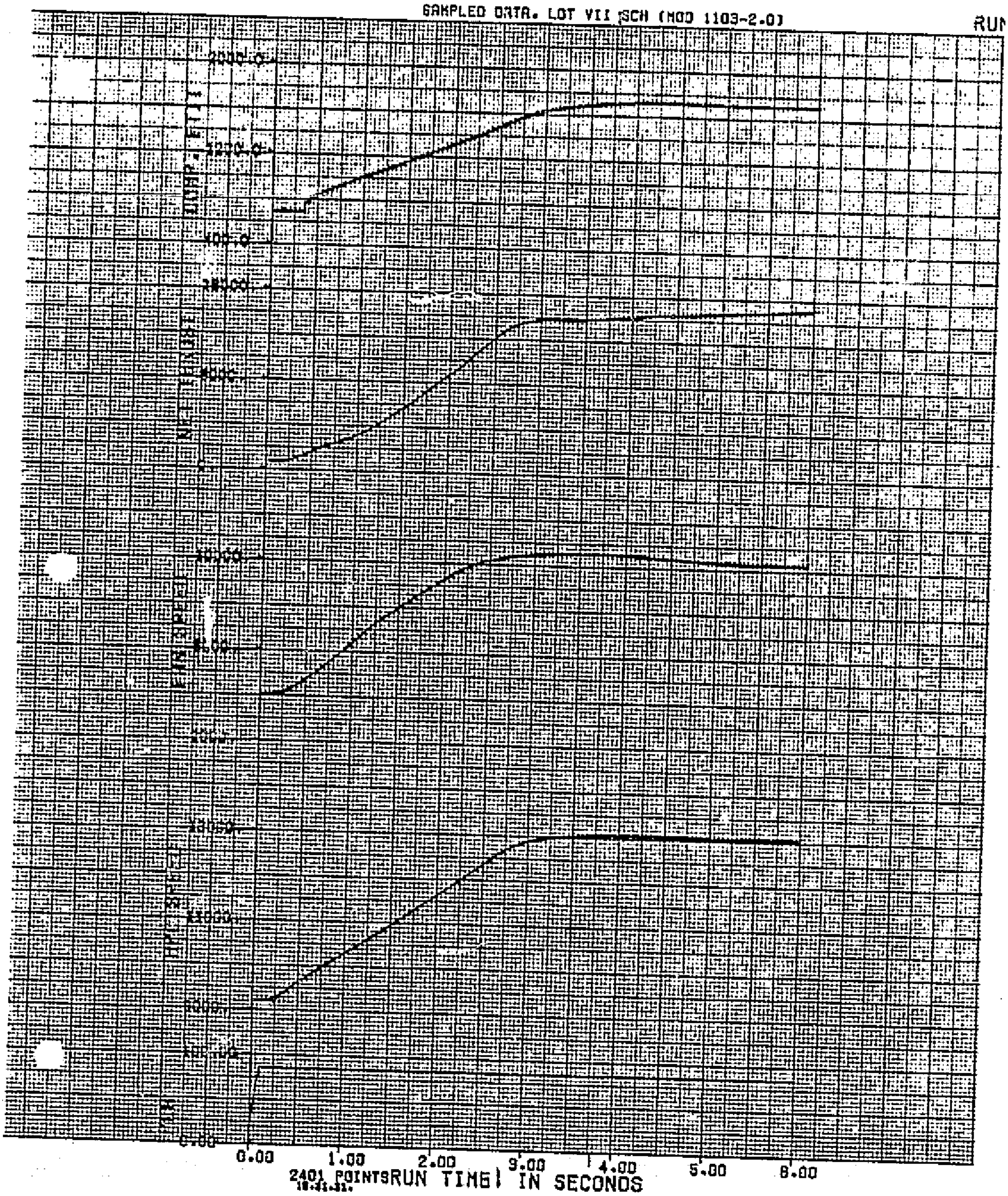

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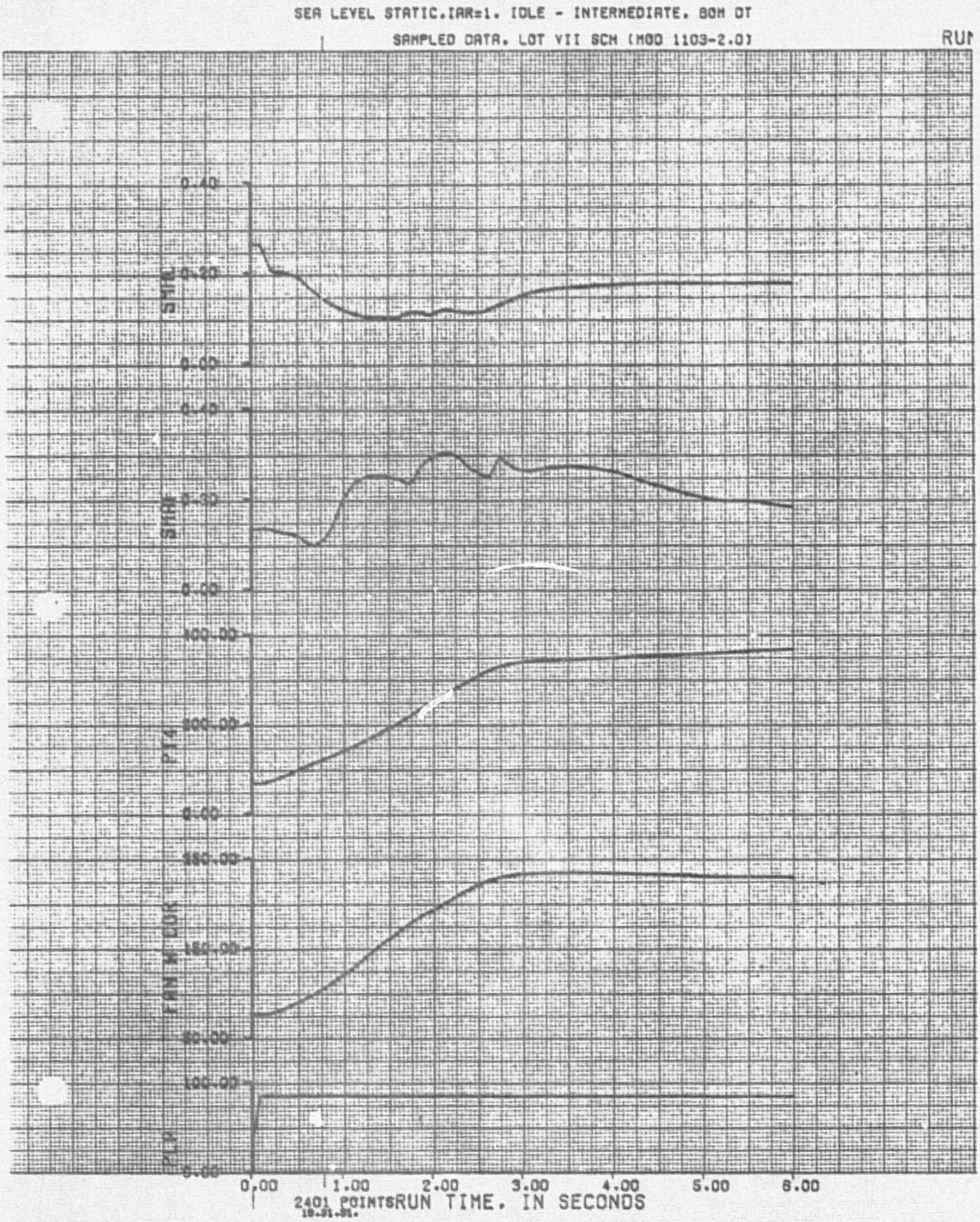

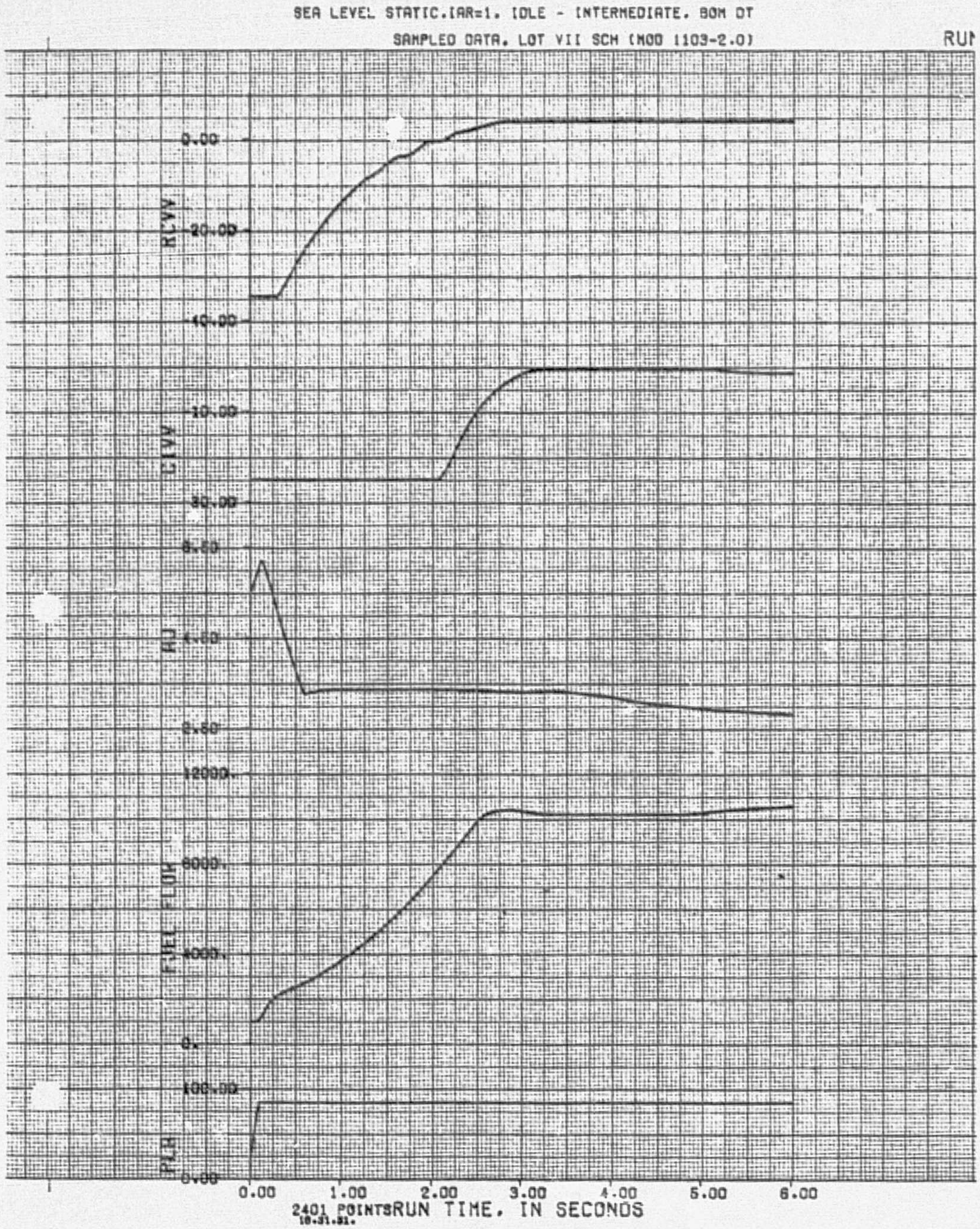
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-40.00
CIVV
10.00
30.00
6.60
AJ
4.60
2.60
12000.
FUEL FLOW
8000.
4000.
0.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

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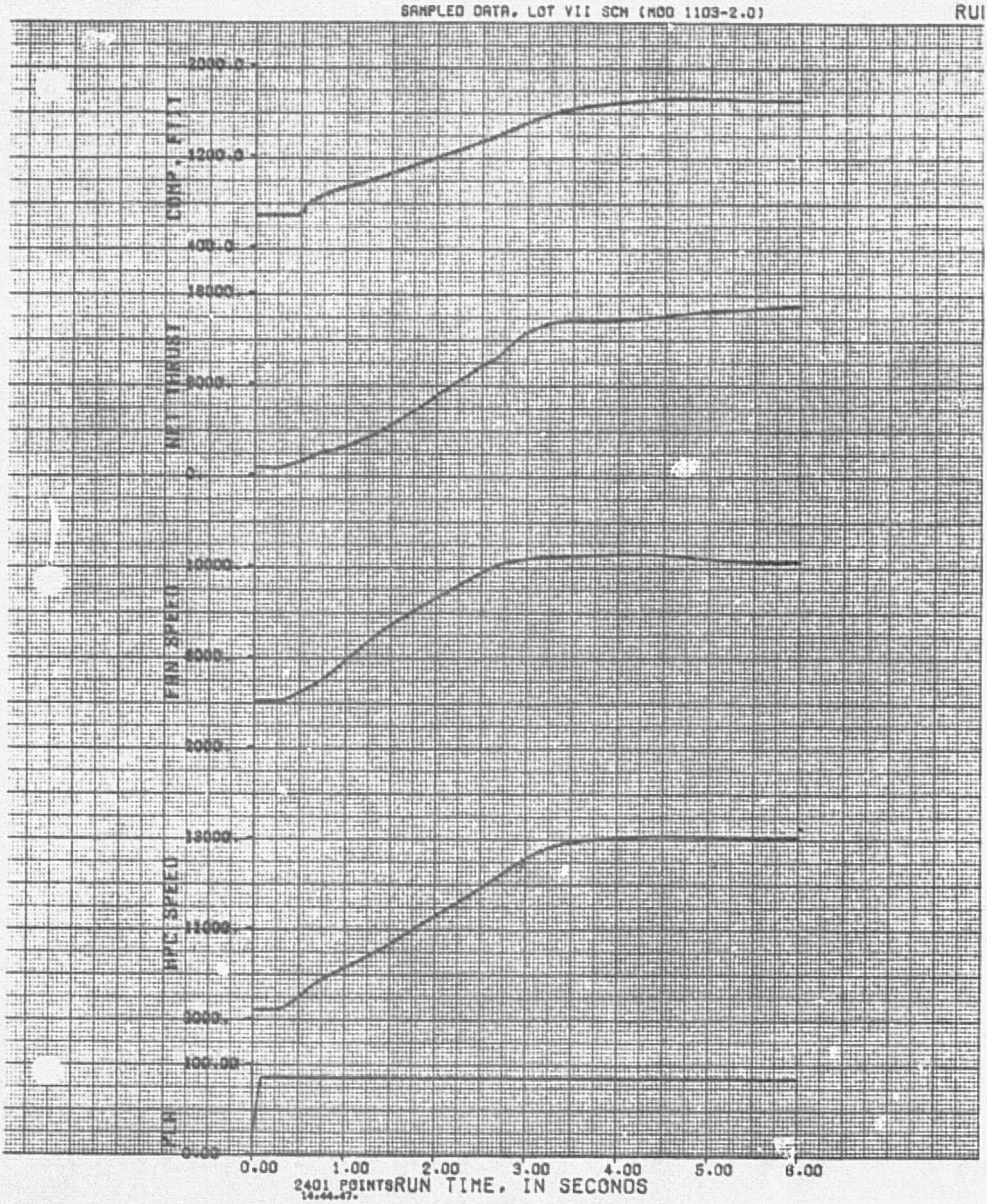

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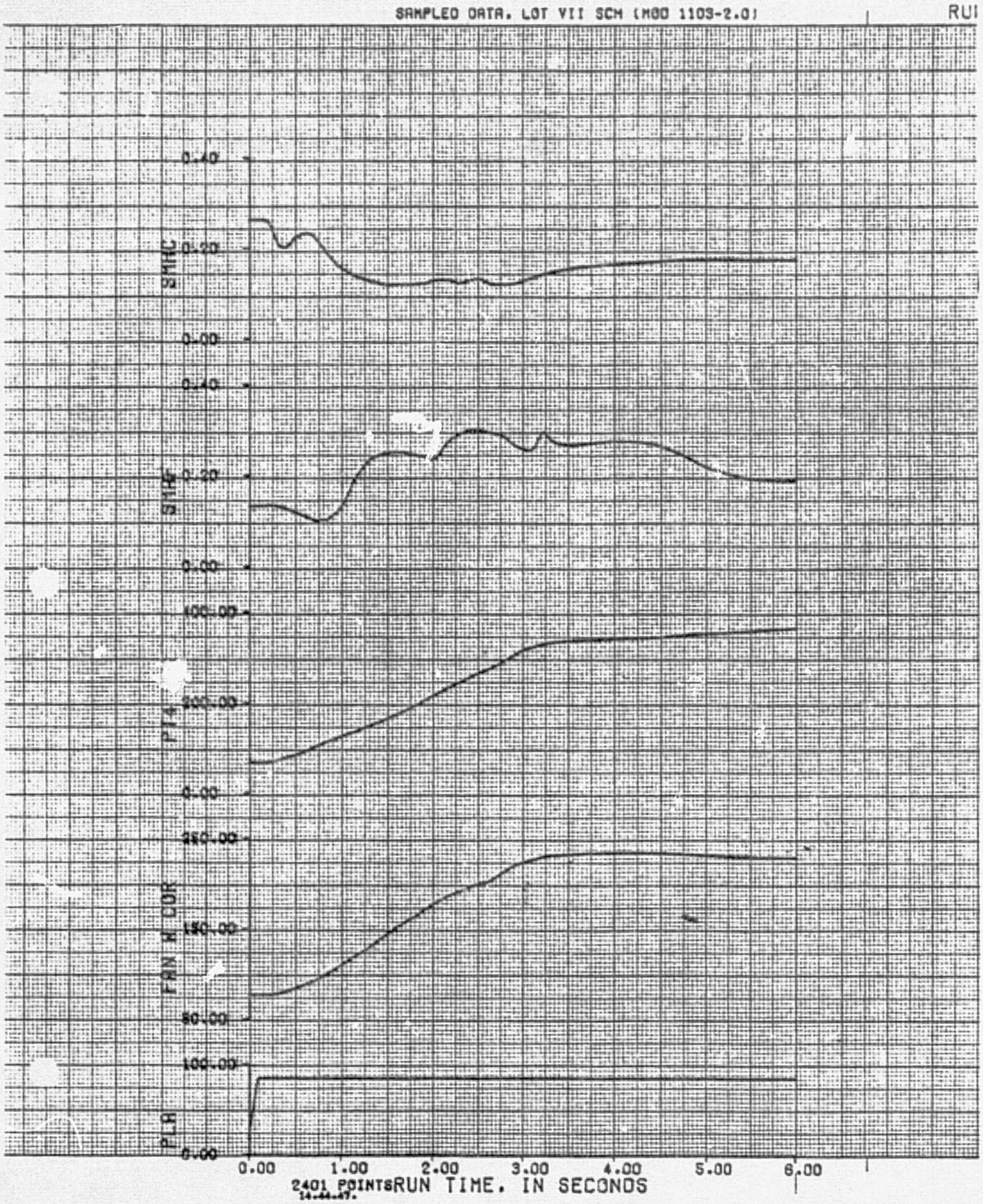

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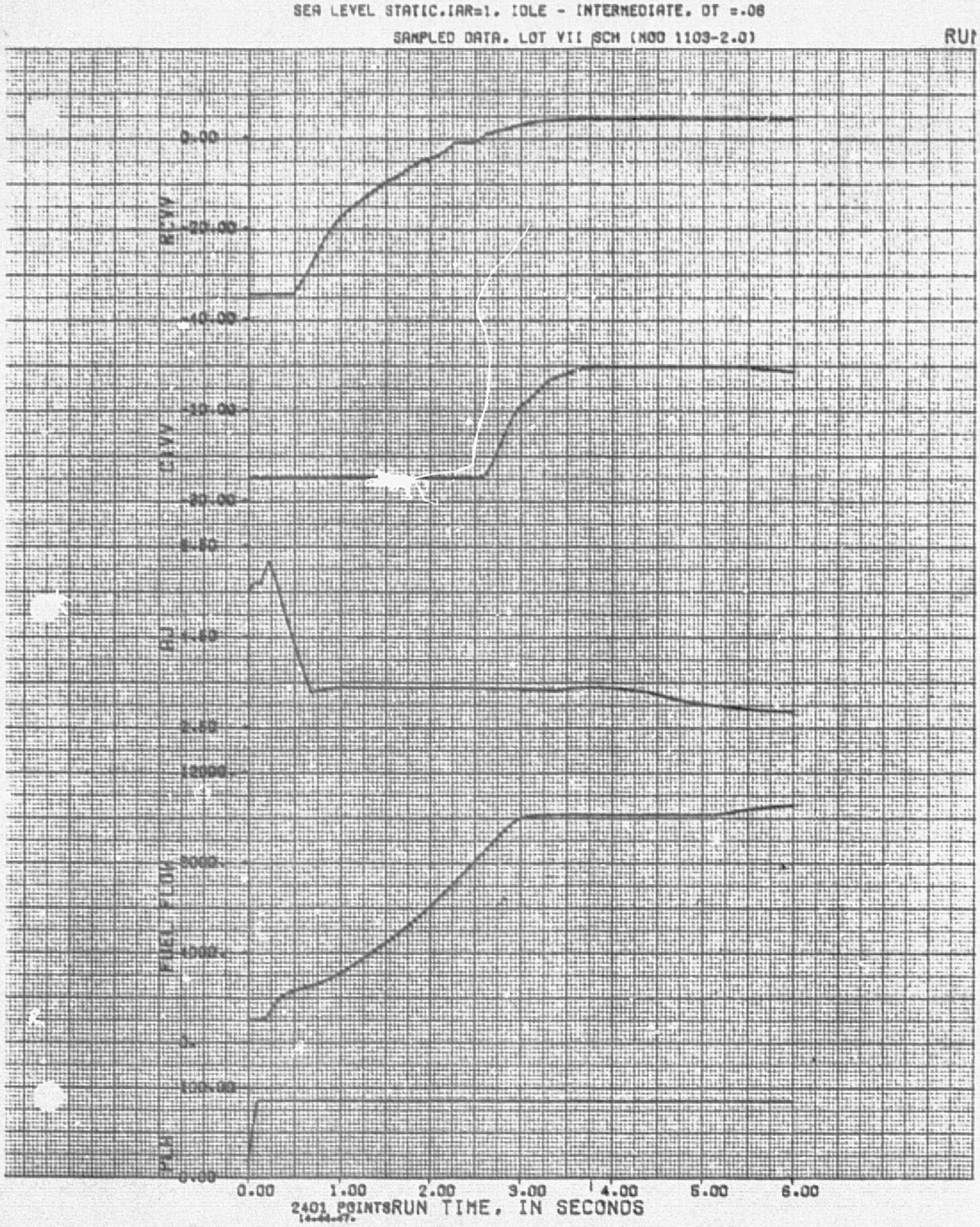

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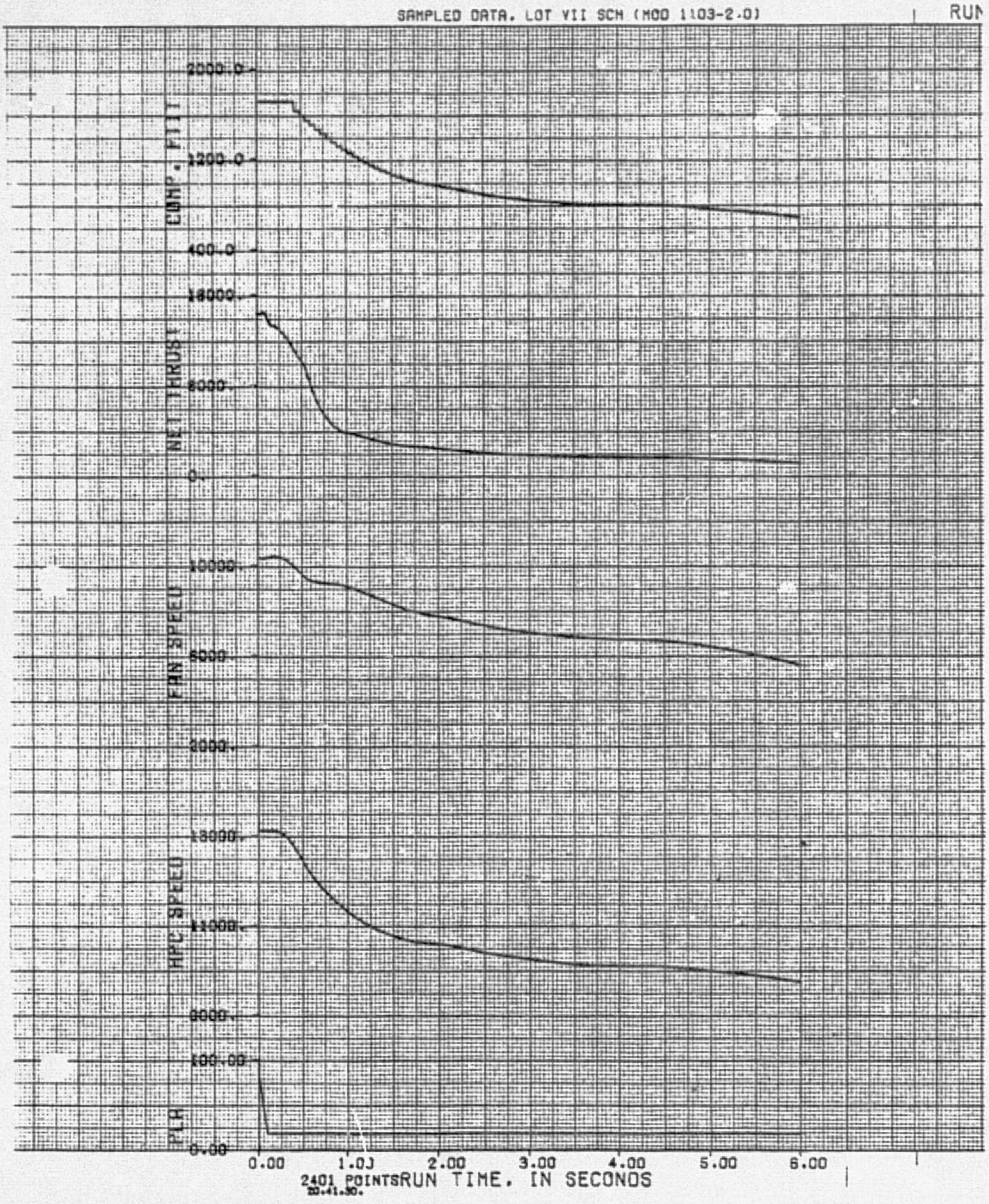

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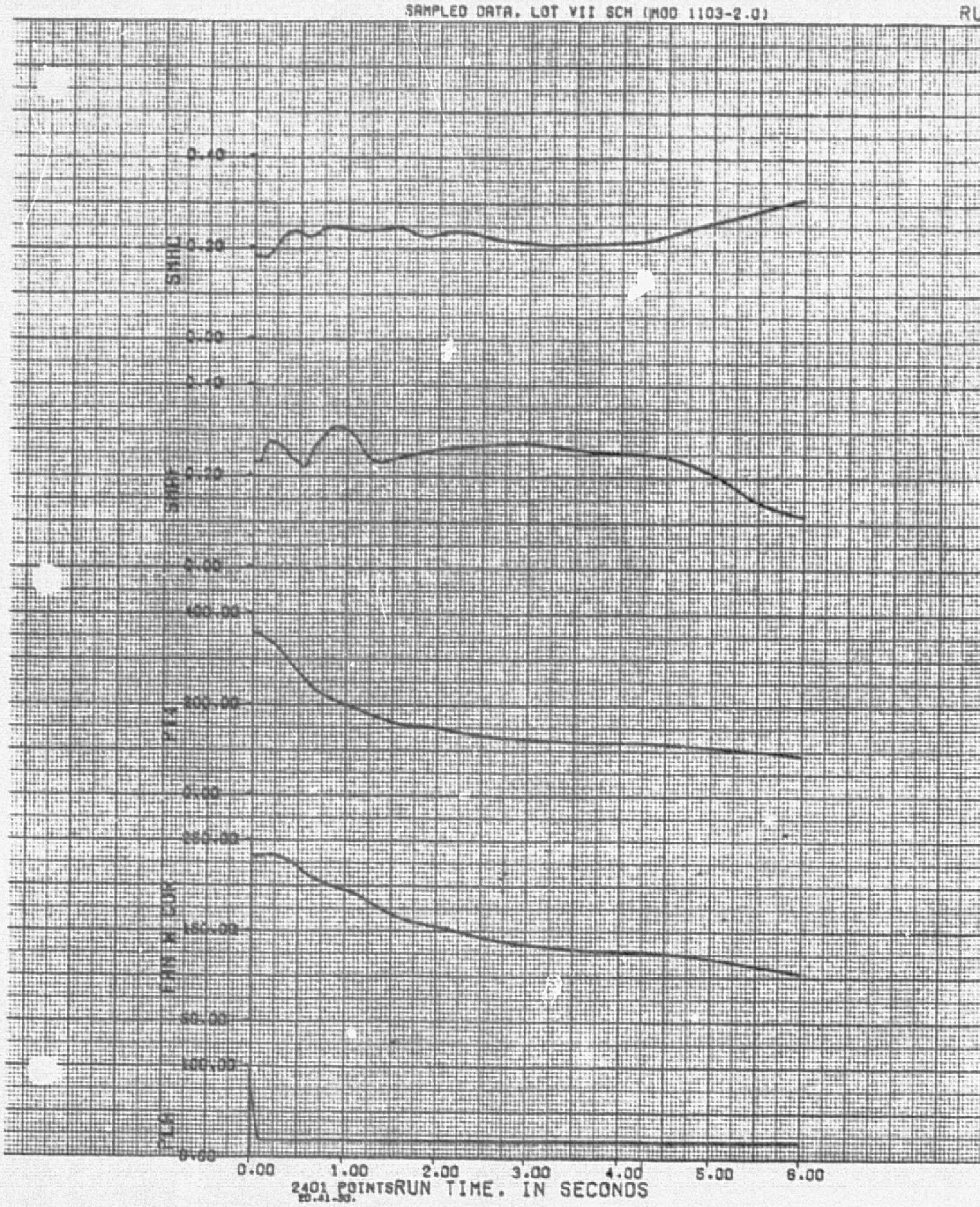

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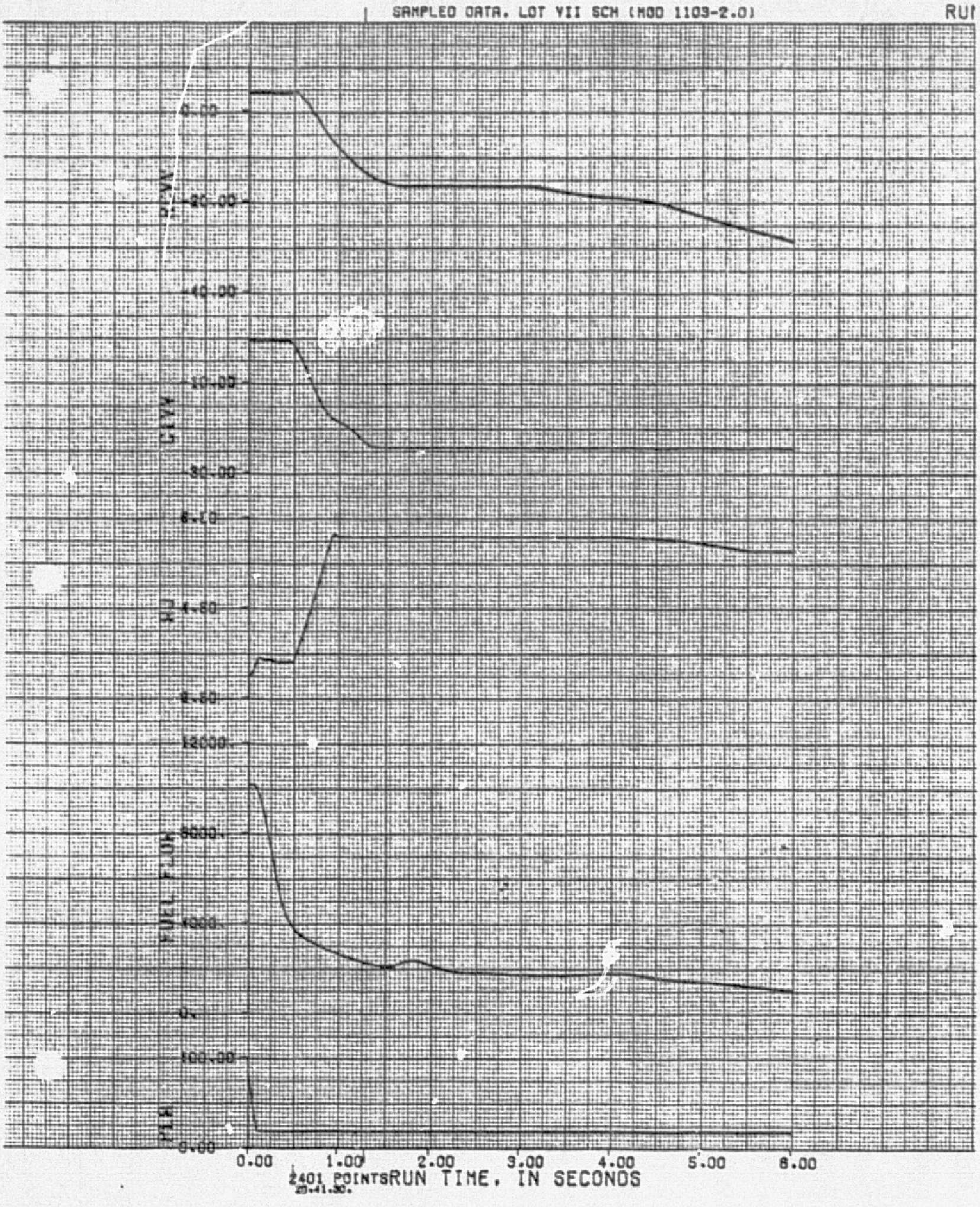

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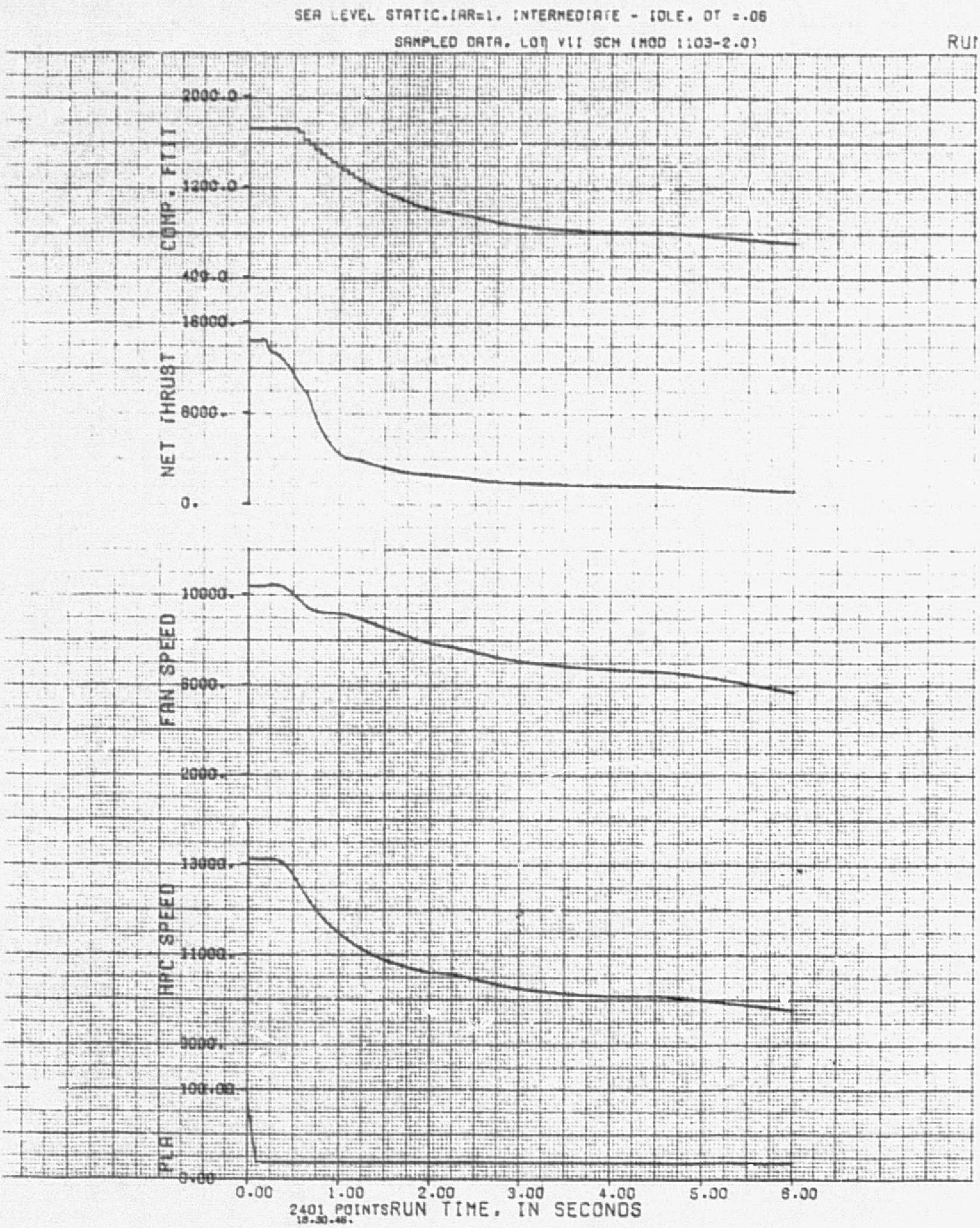

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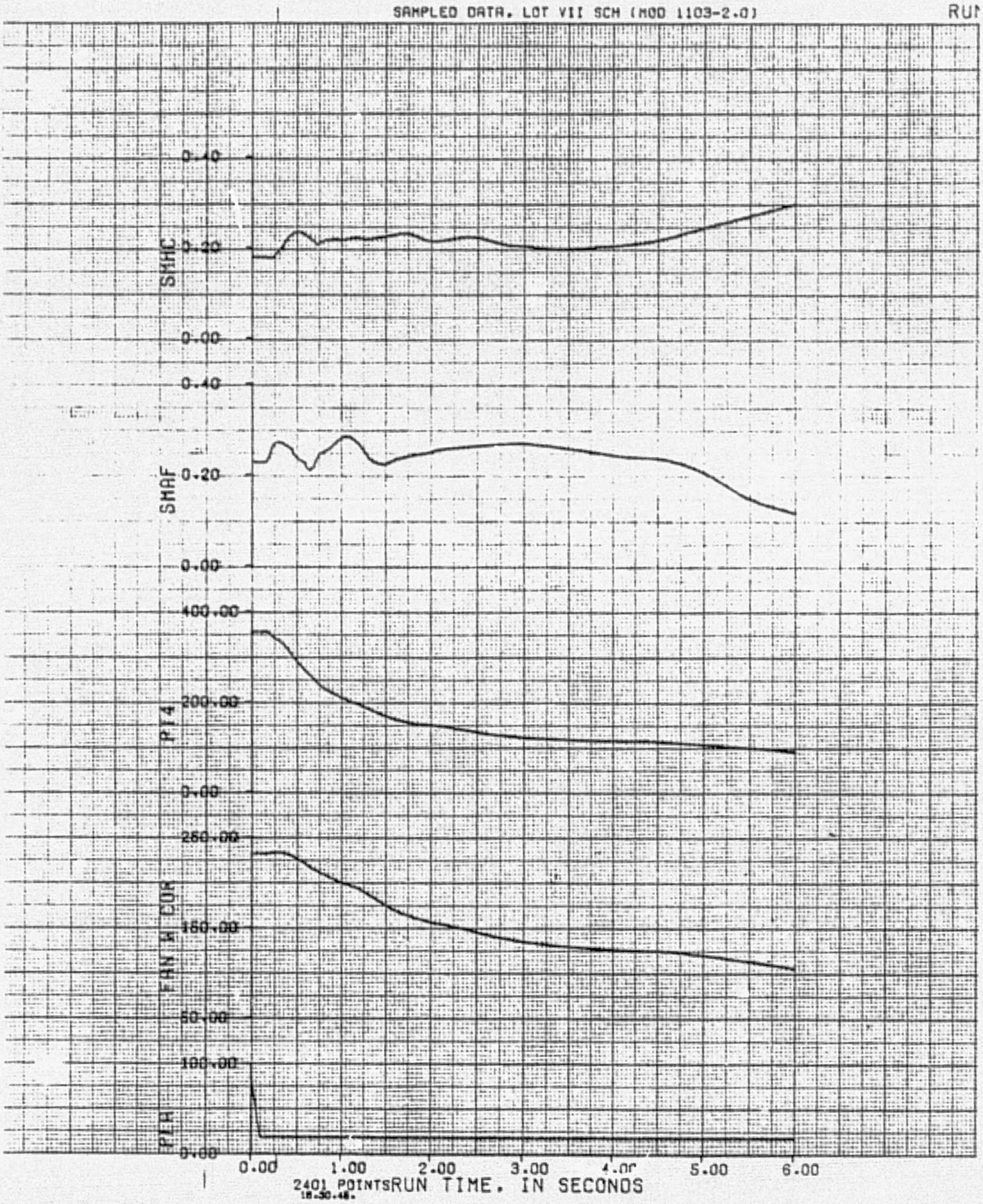

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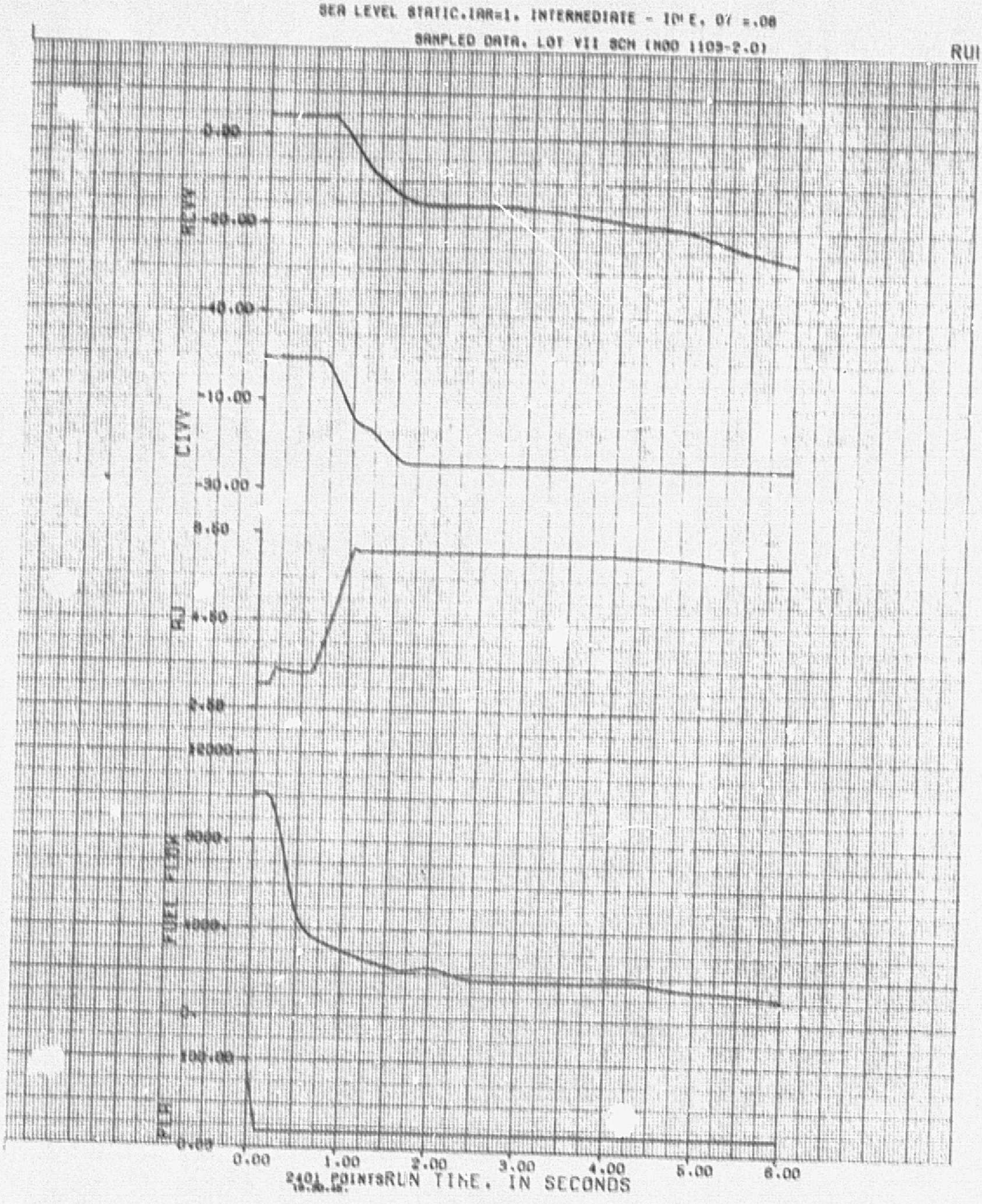

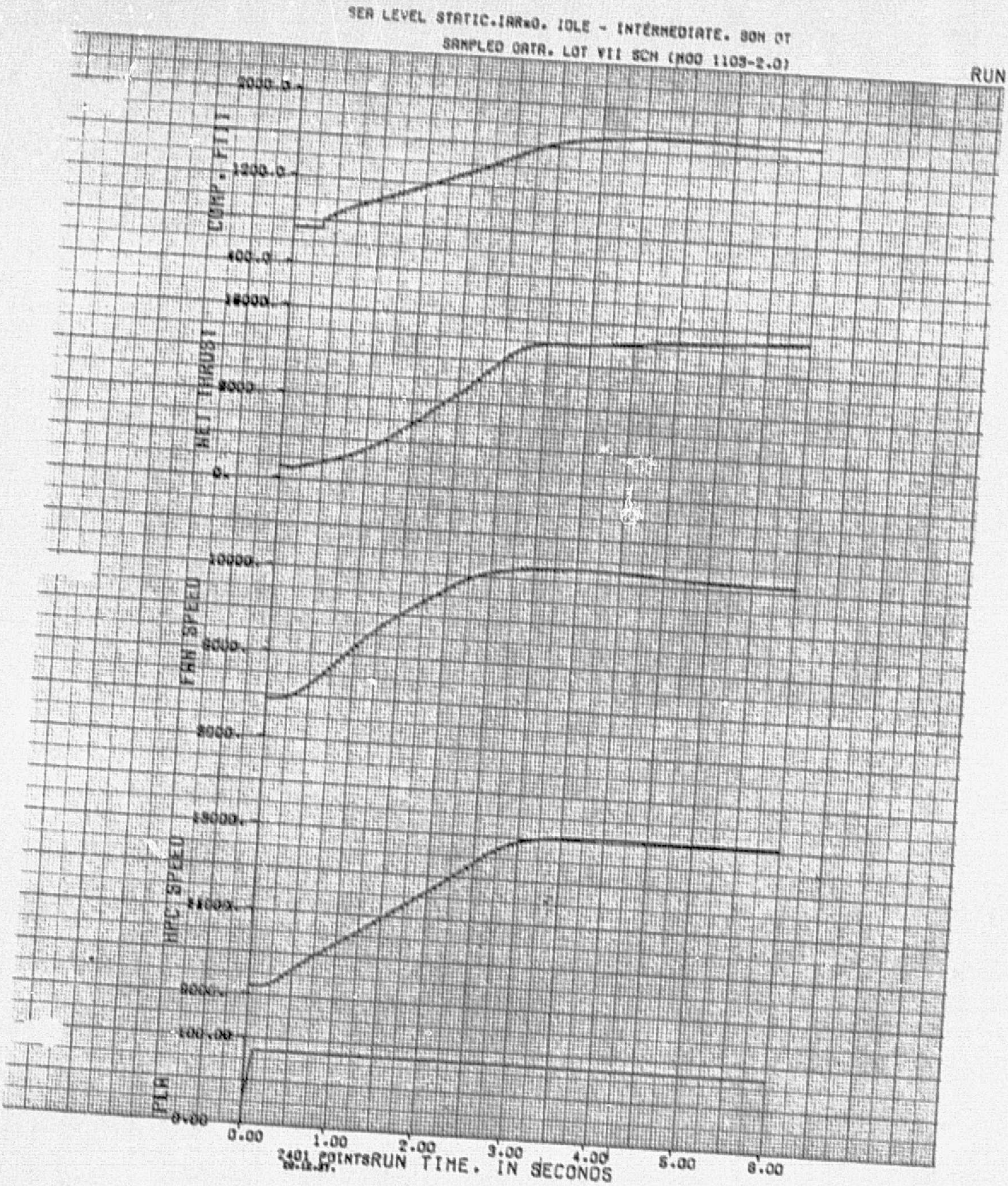
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8000.
0.
FAN SPEED
10000.
8000.
6000.
HPC SPEED
15000.
12000.
9000.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

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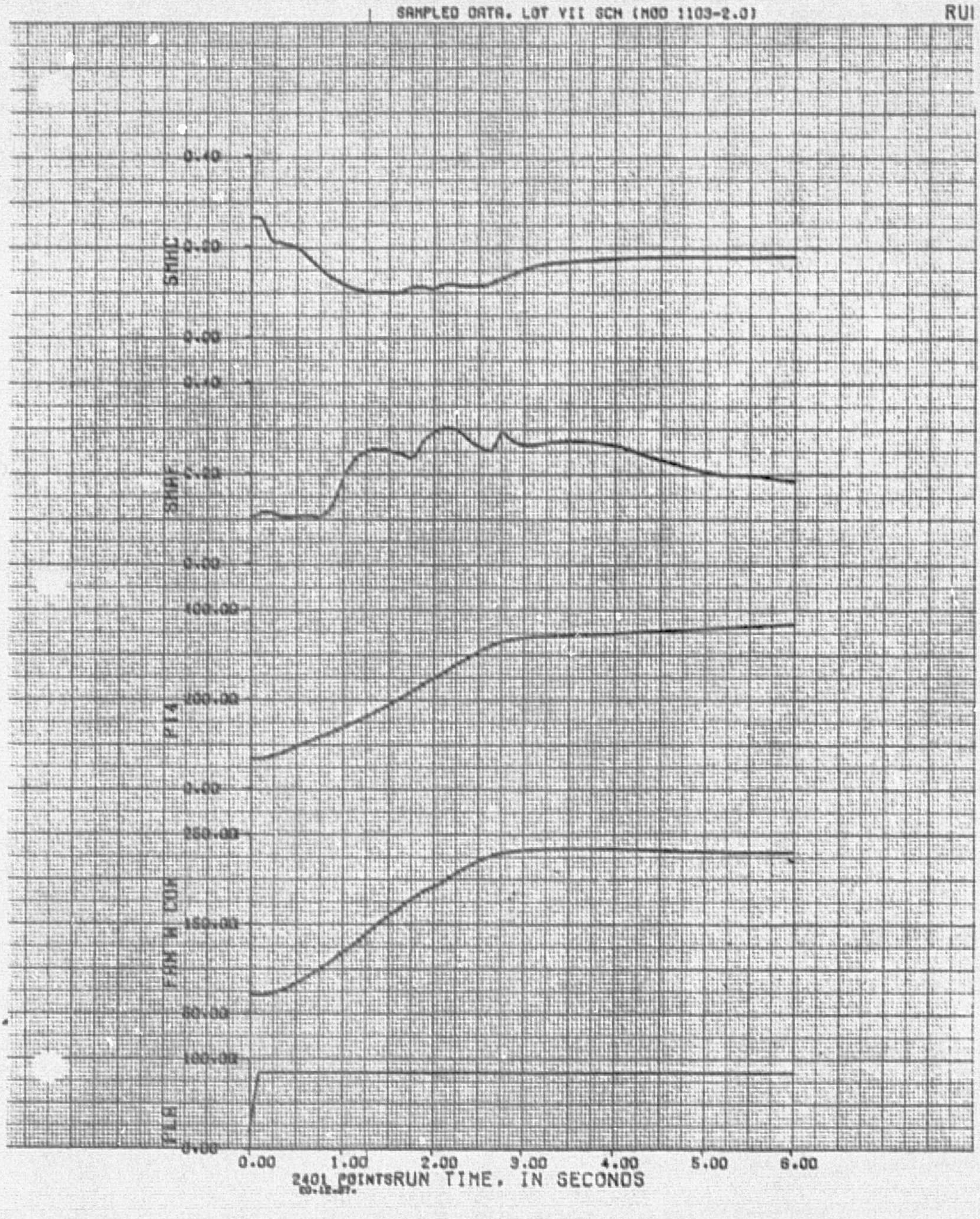

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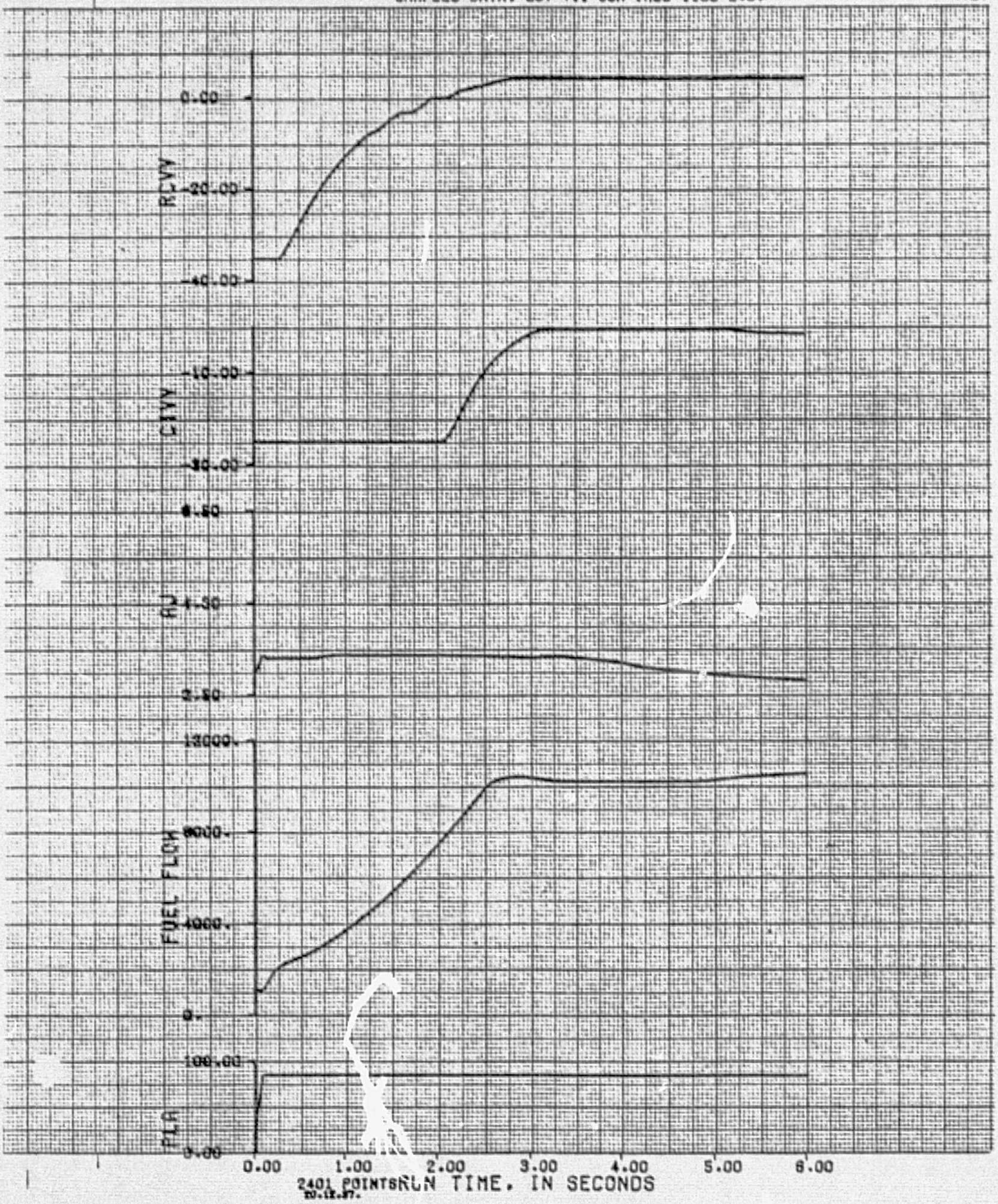

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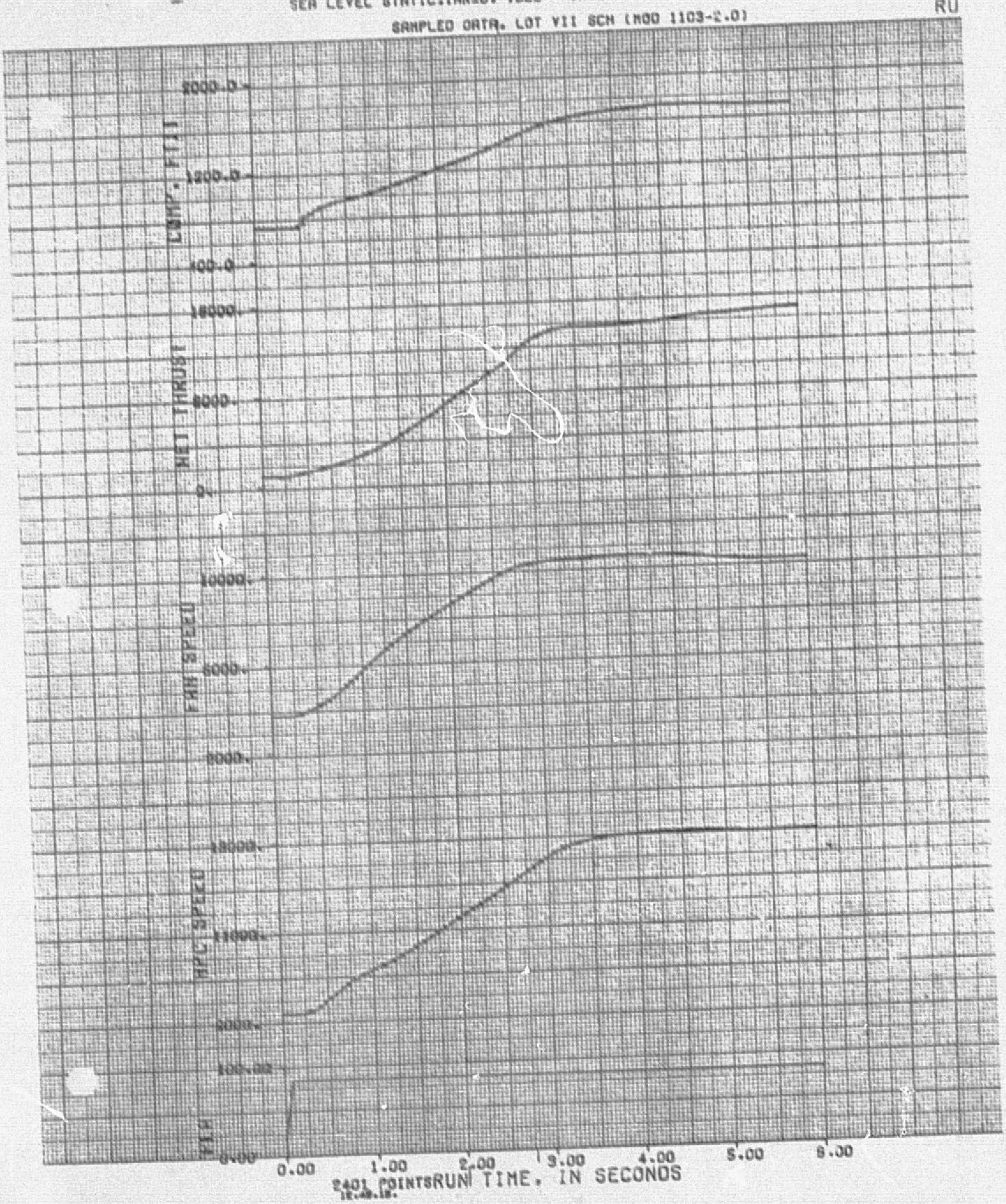

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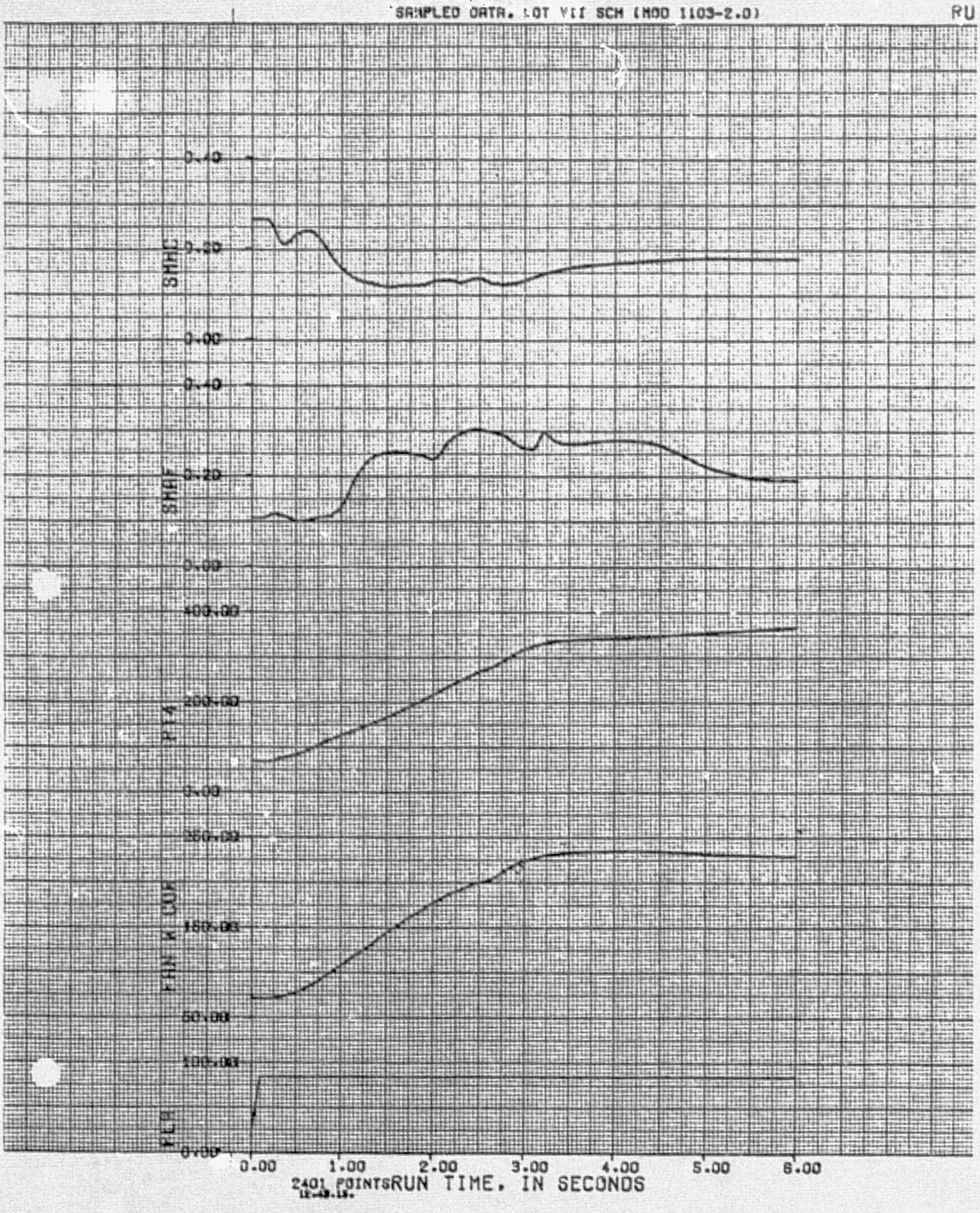

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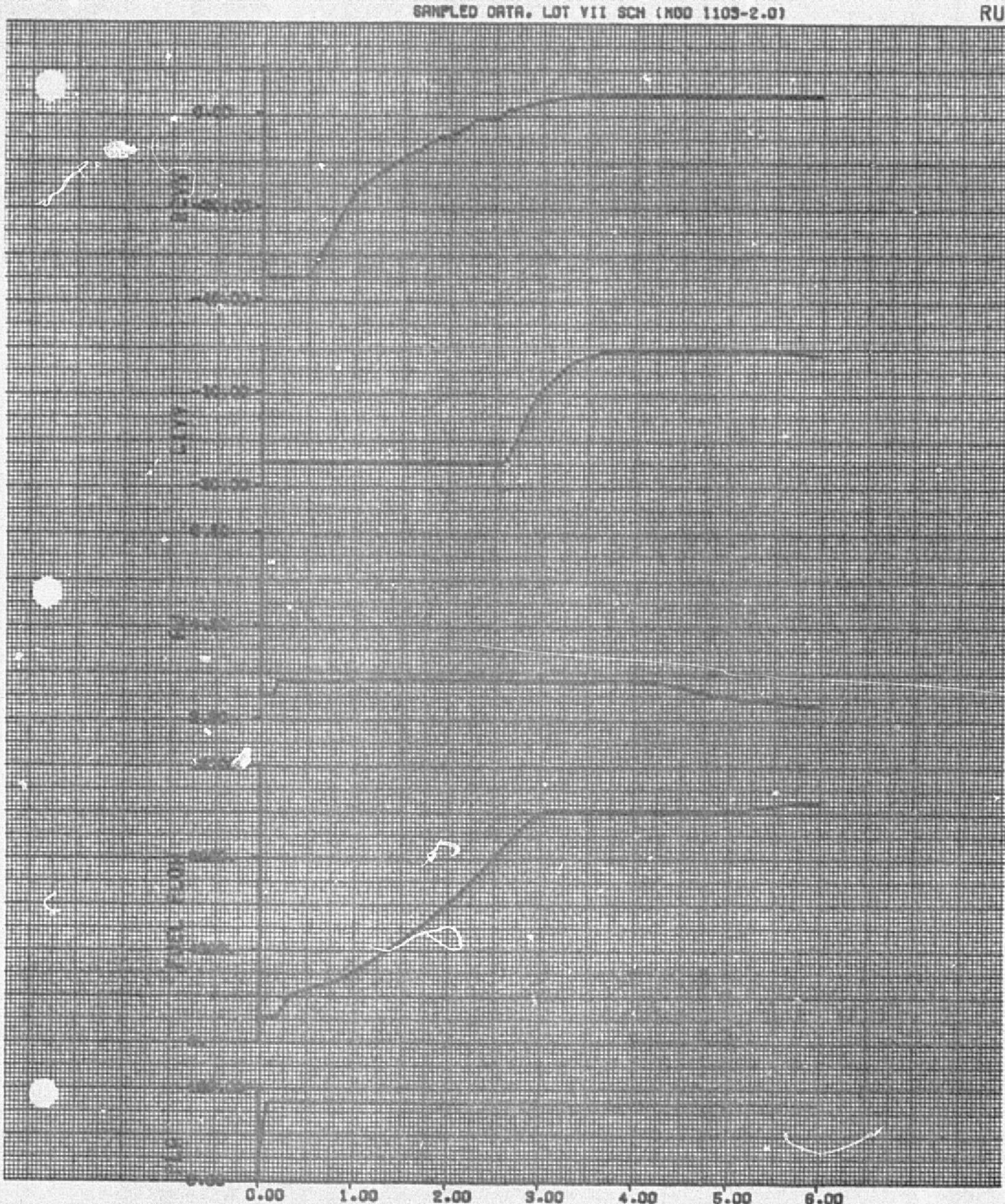

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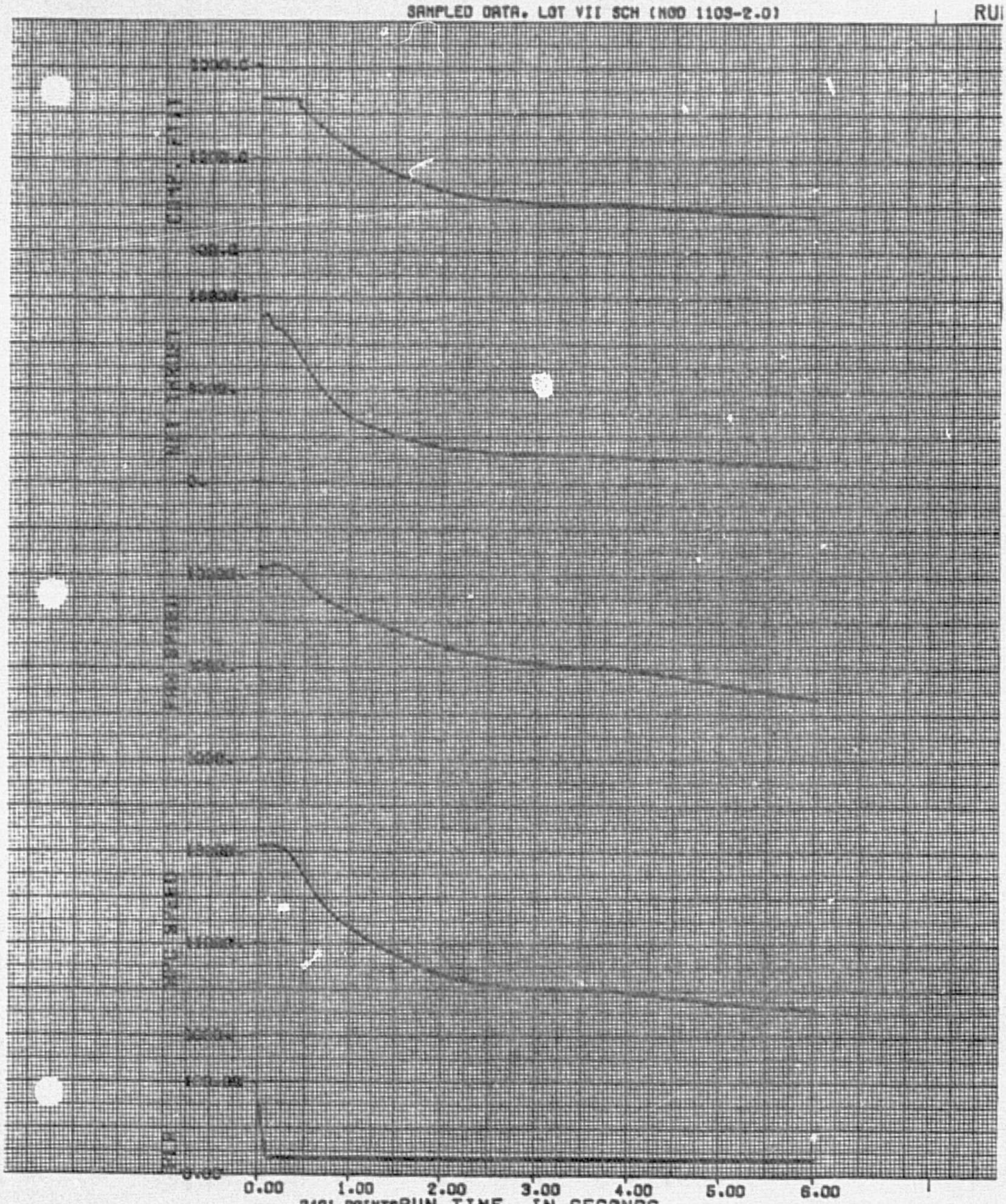

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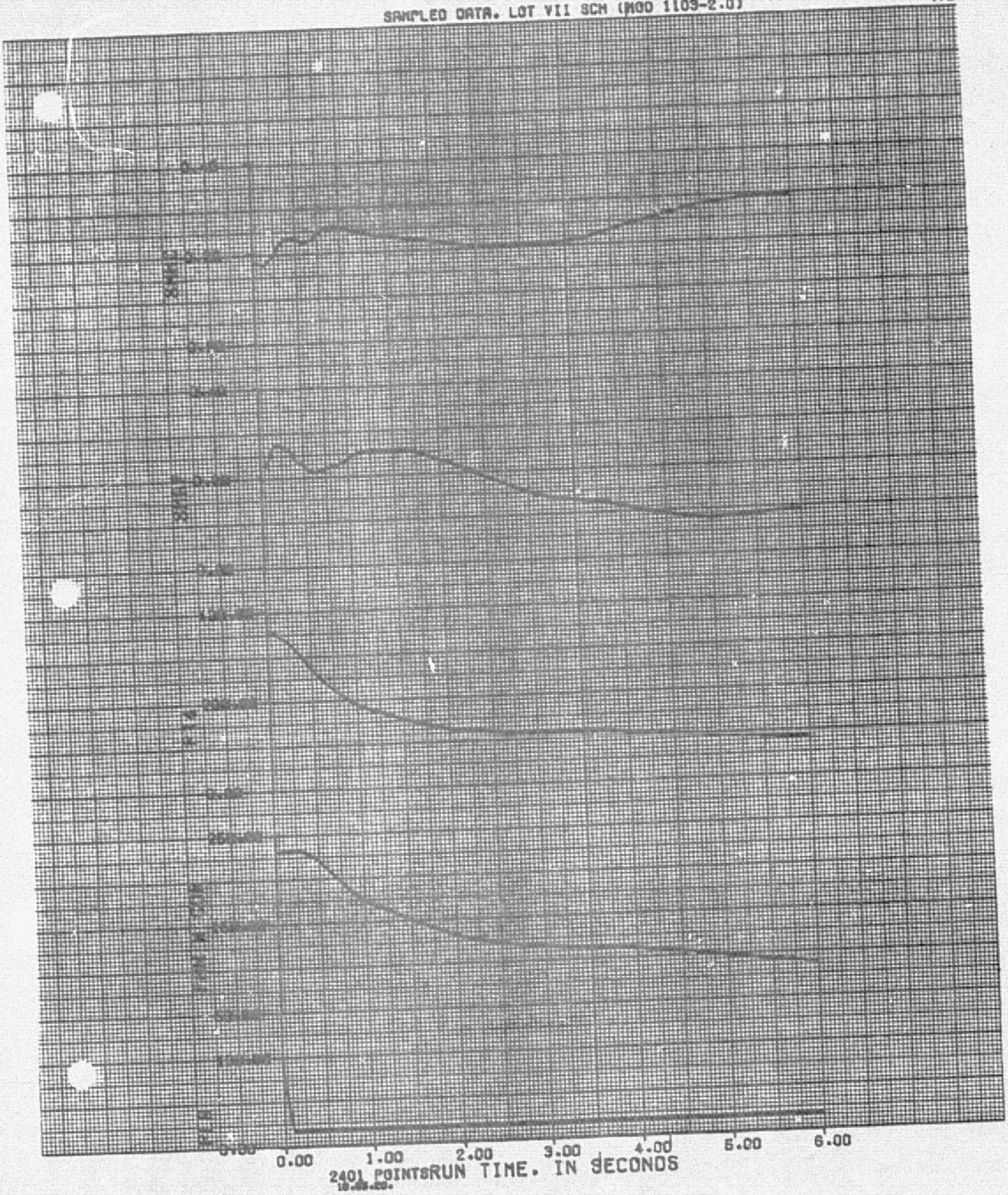

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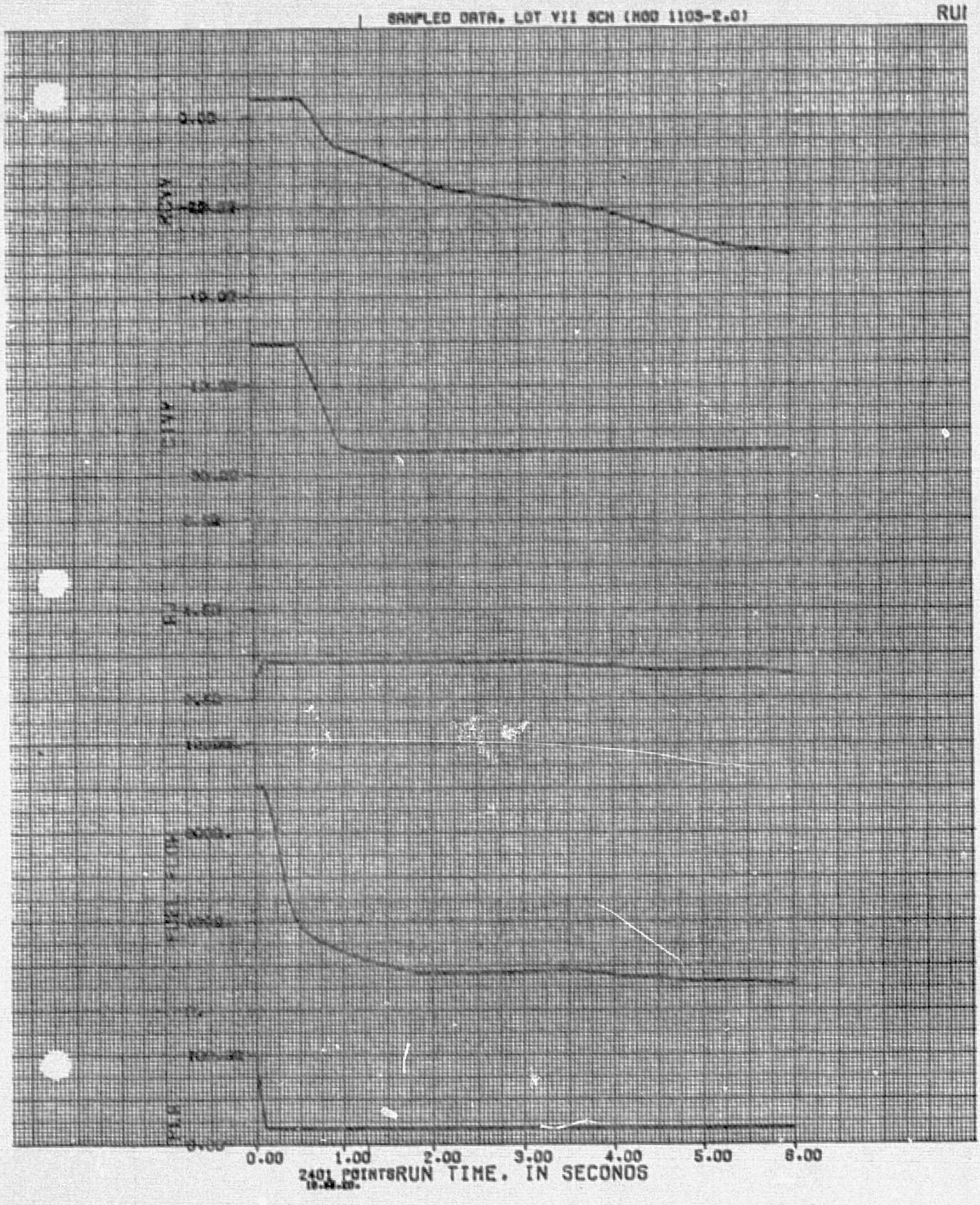

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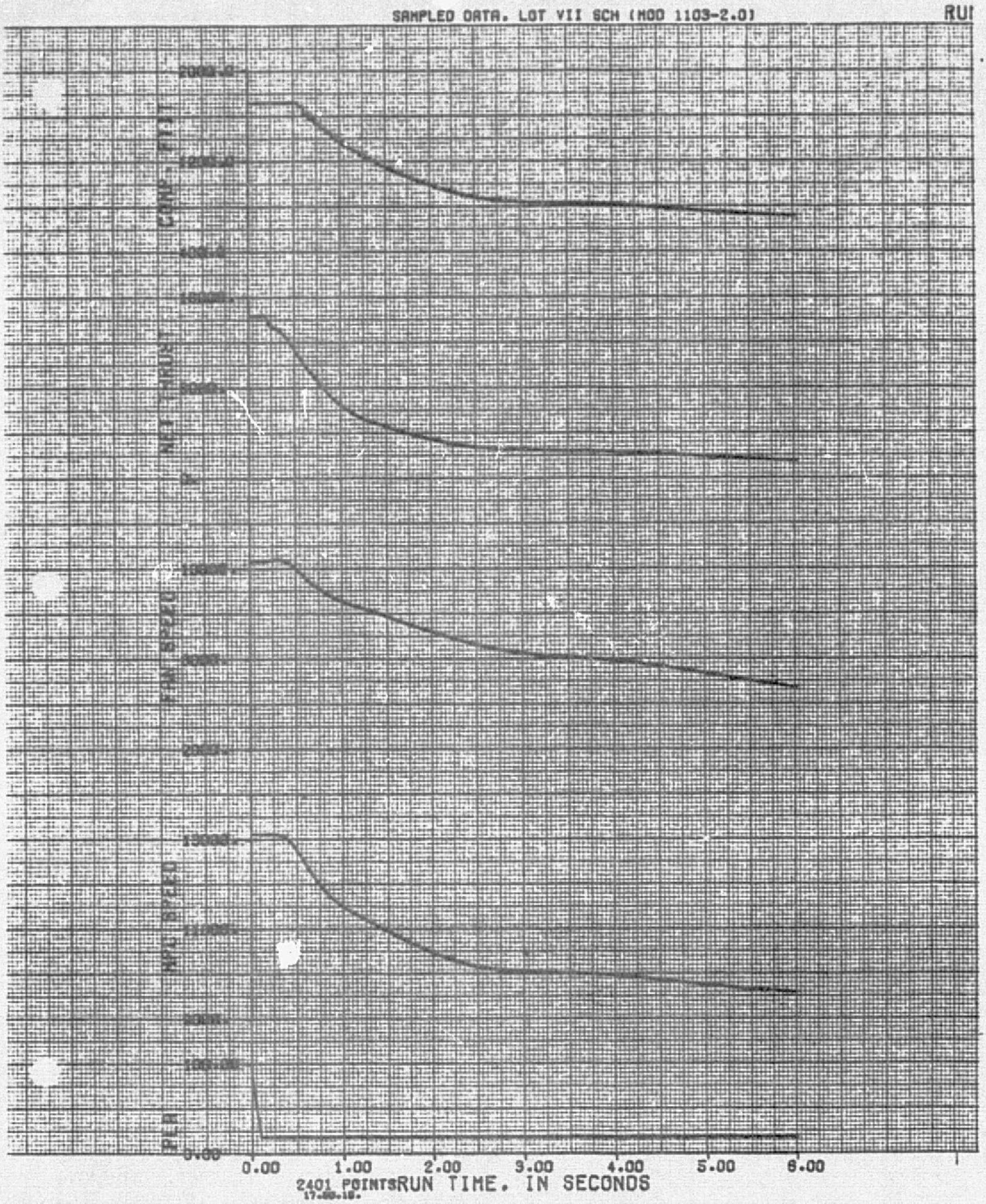

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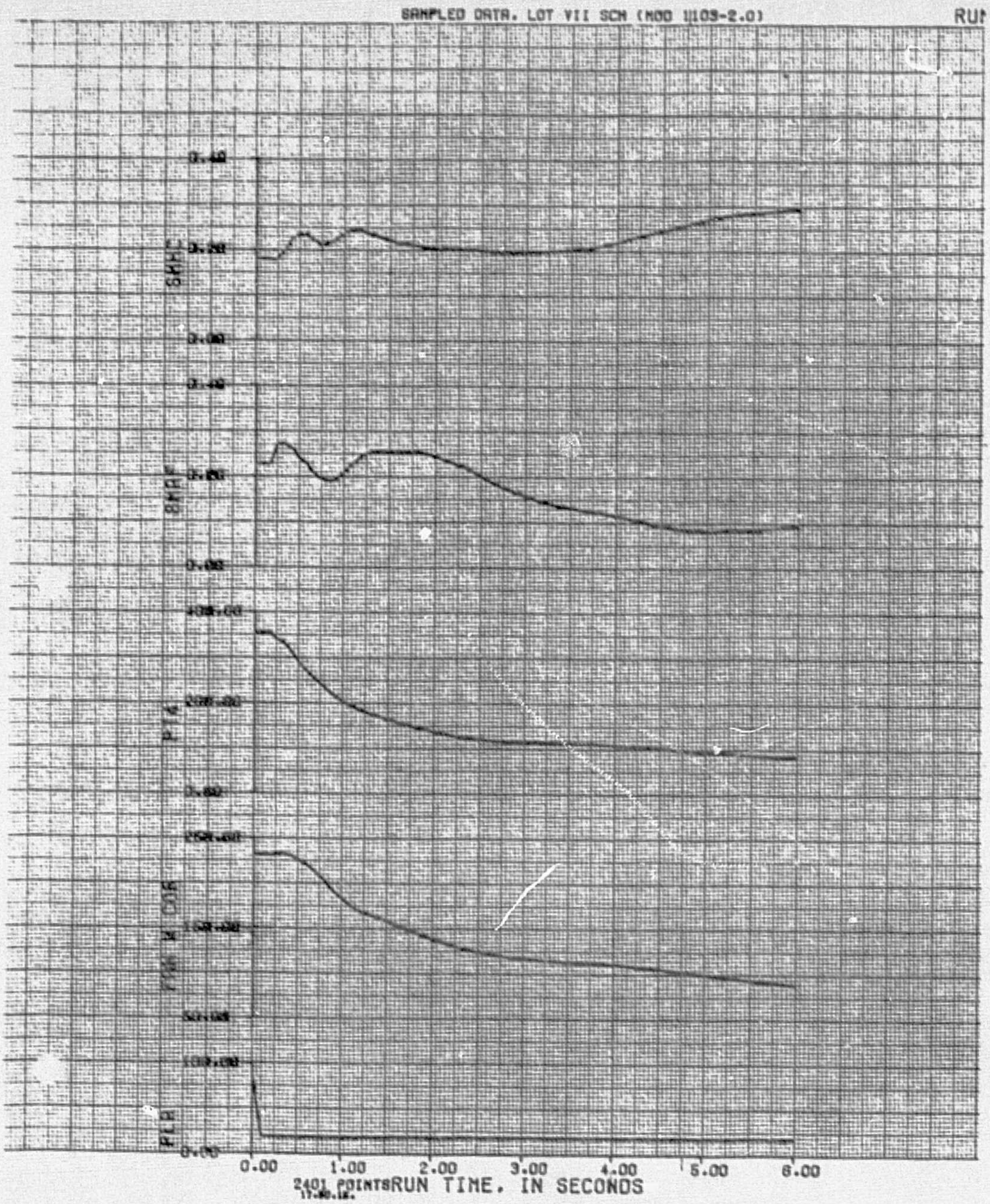

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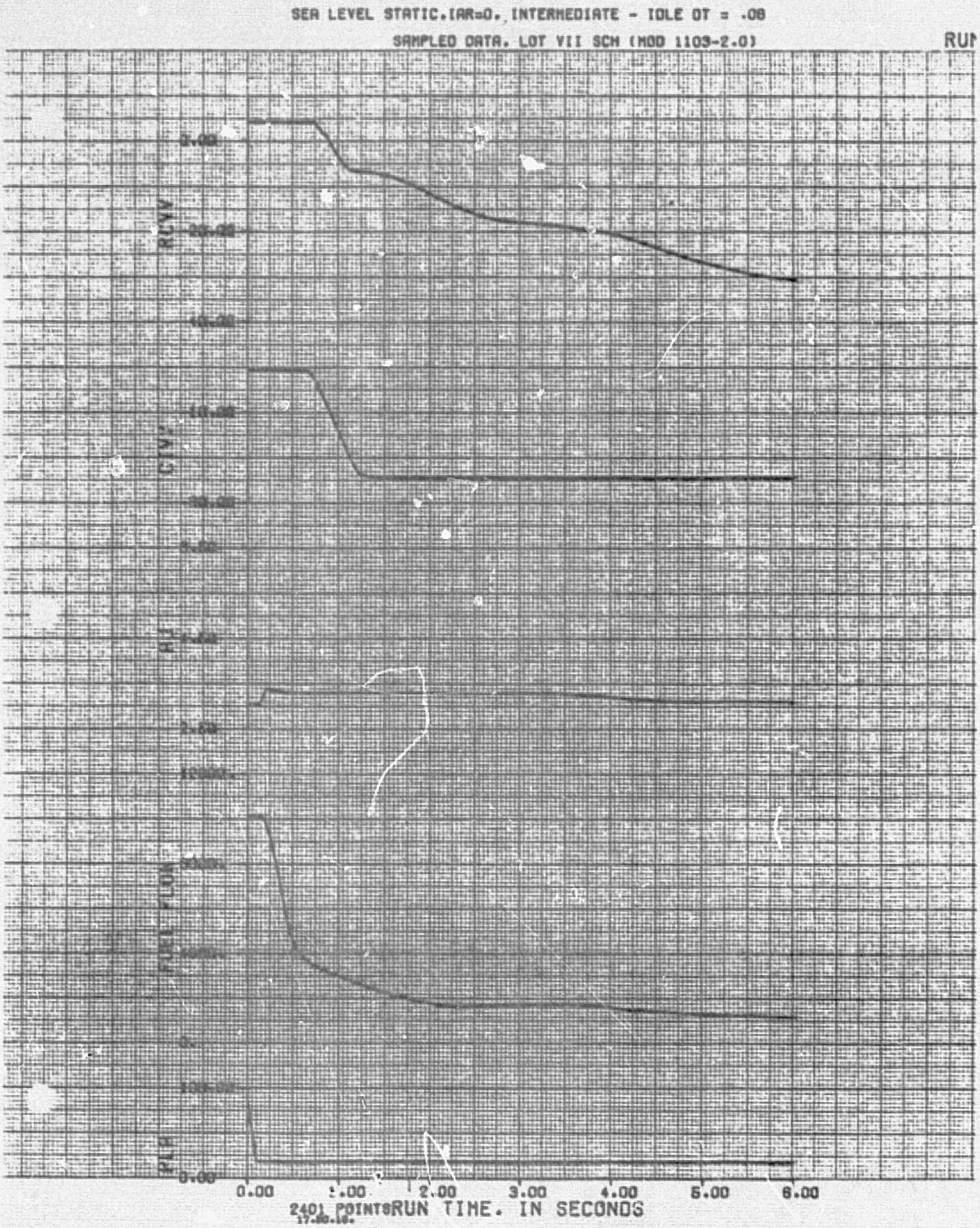

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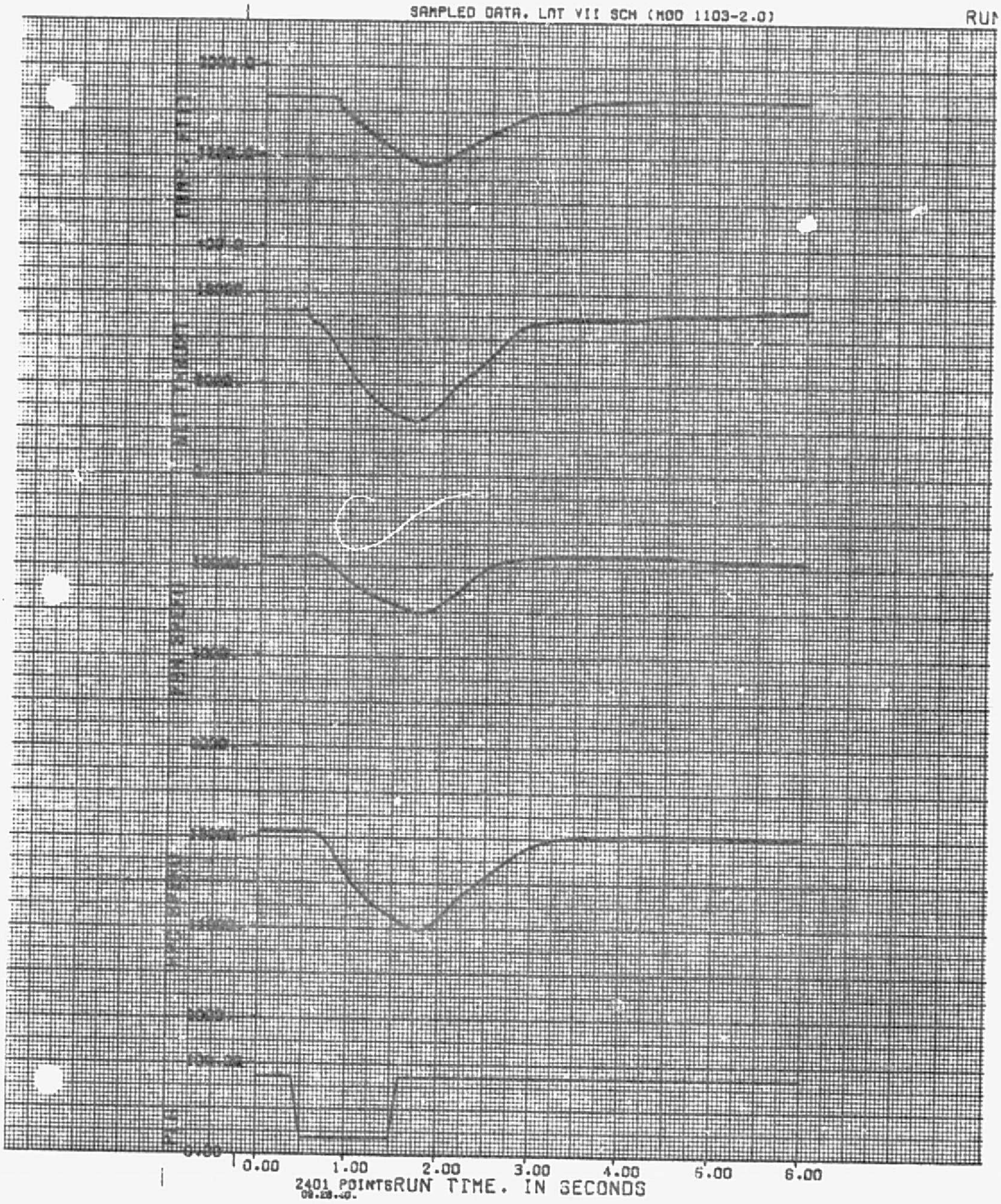

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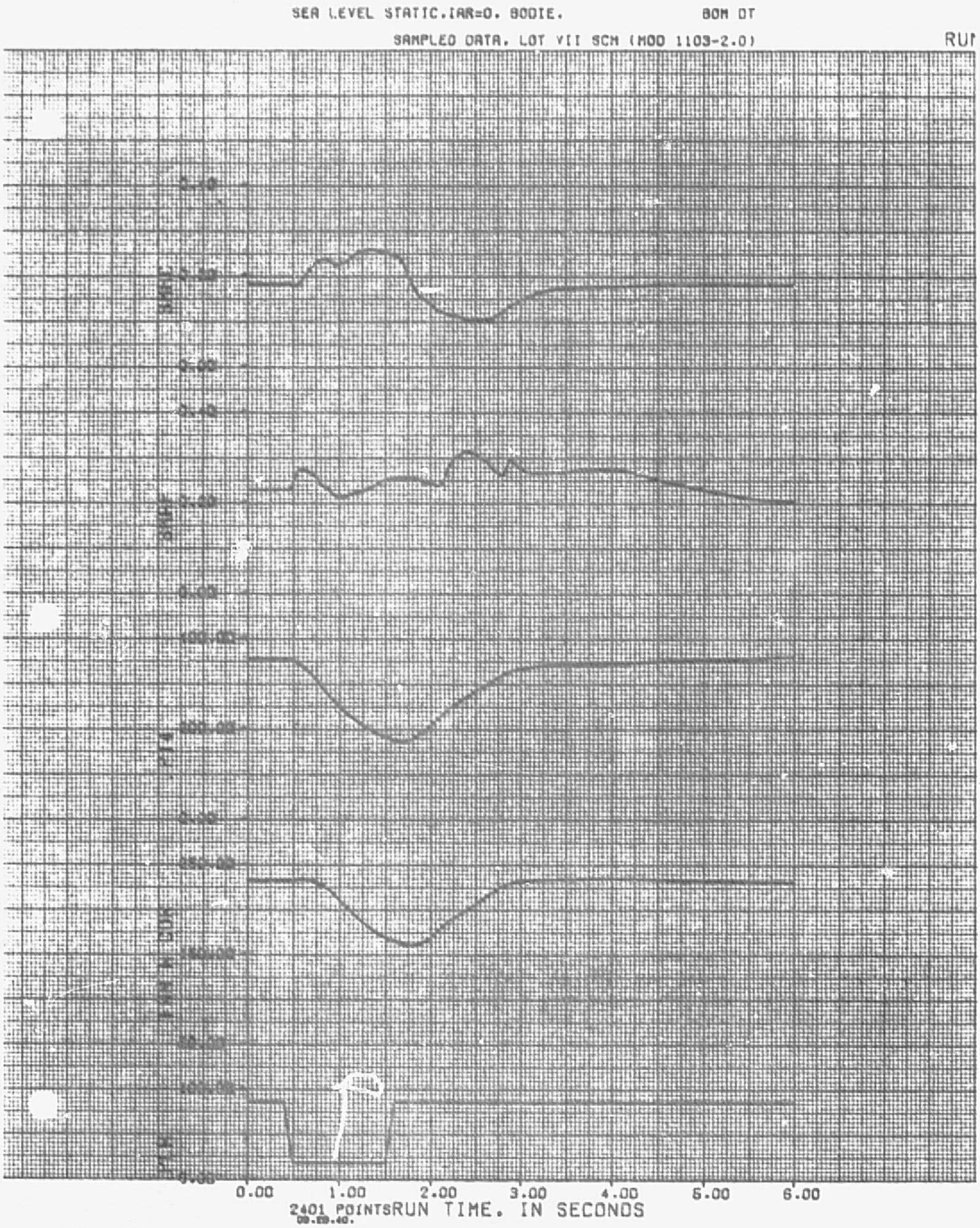

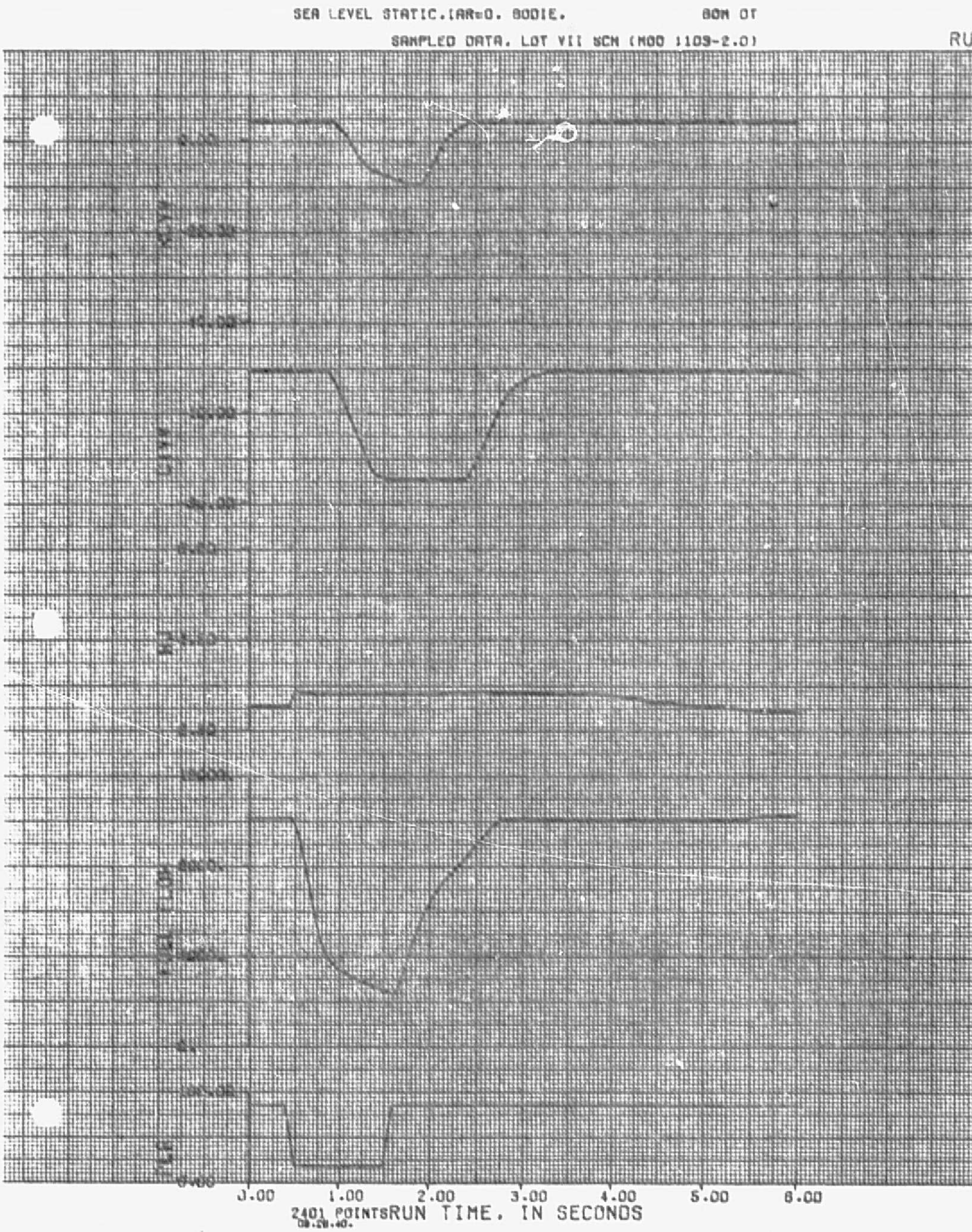
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6.00
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RUN TIME. IN SECONDS

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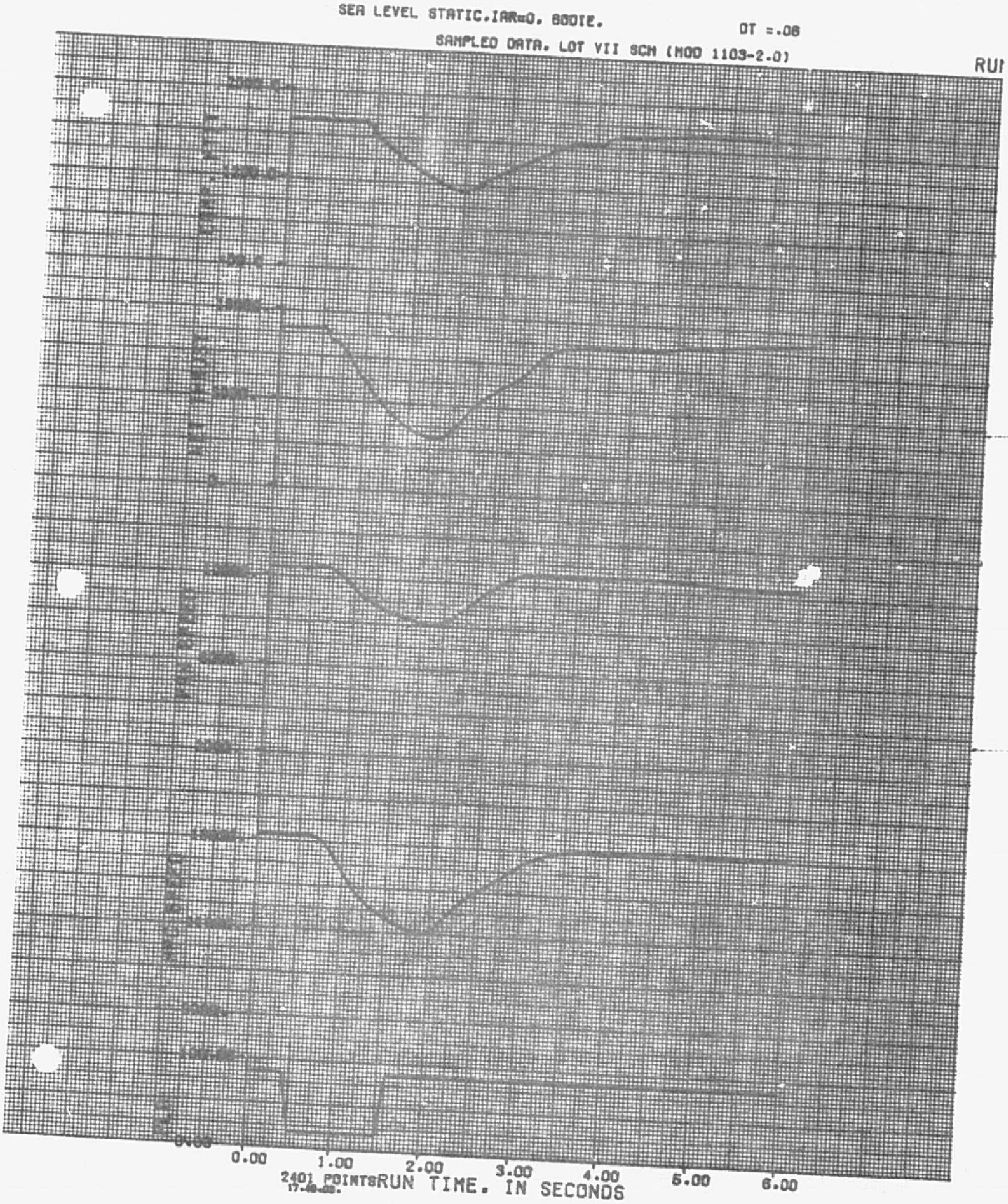

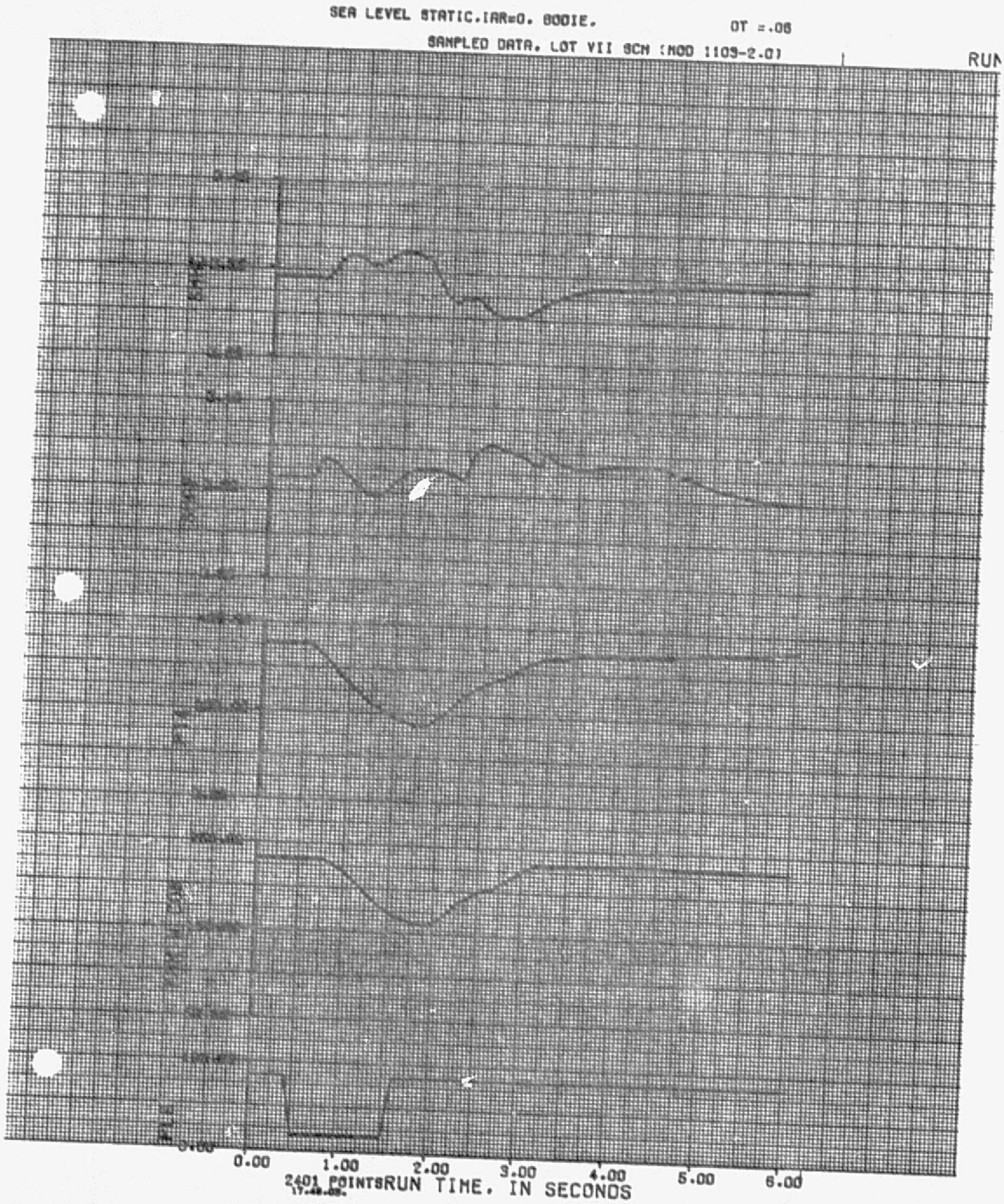
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3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME. IN SECONDS

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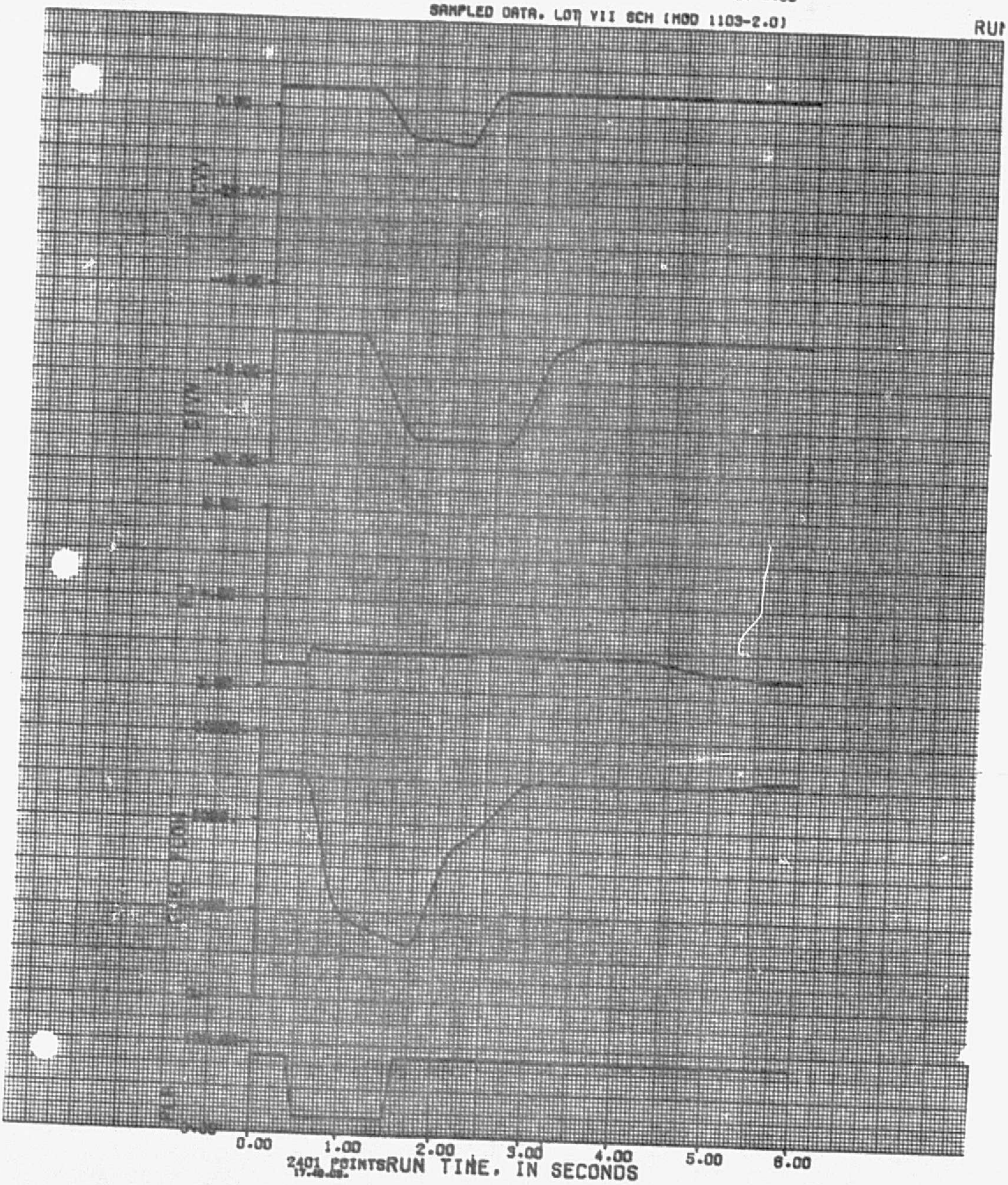

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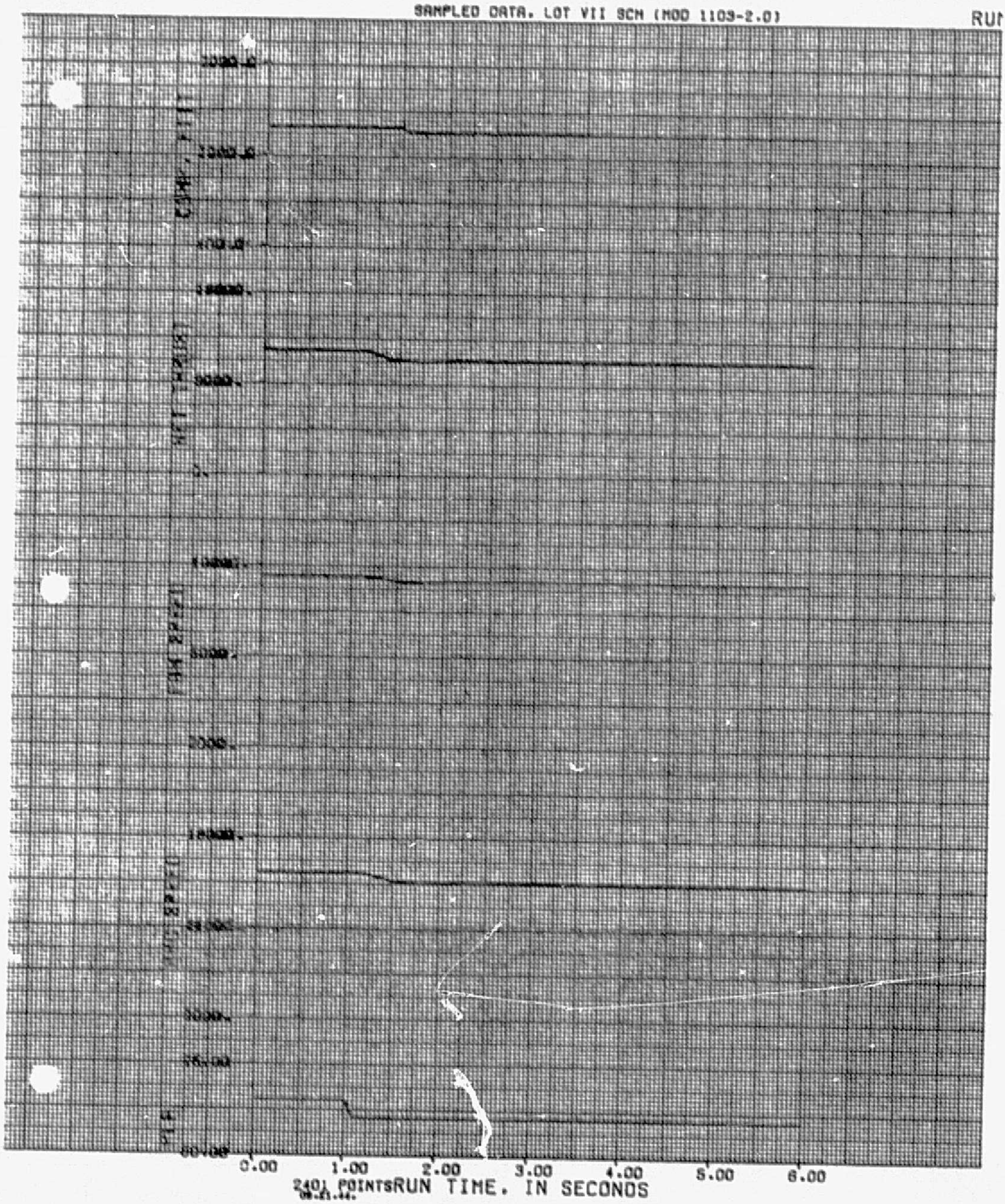

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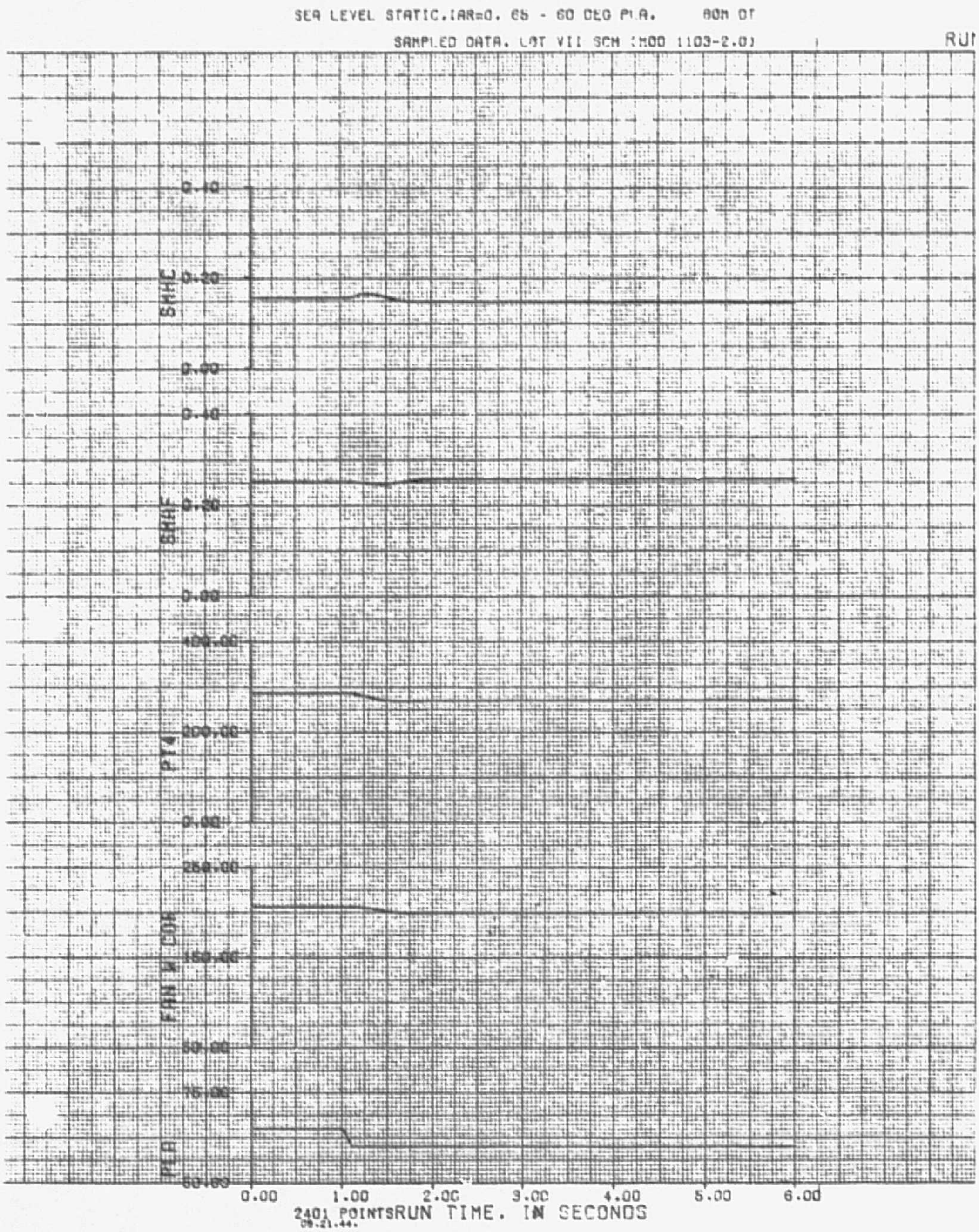

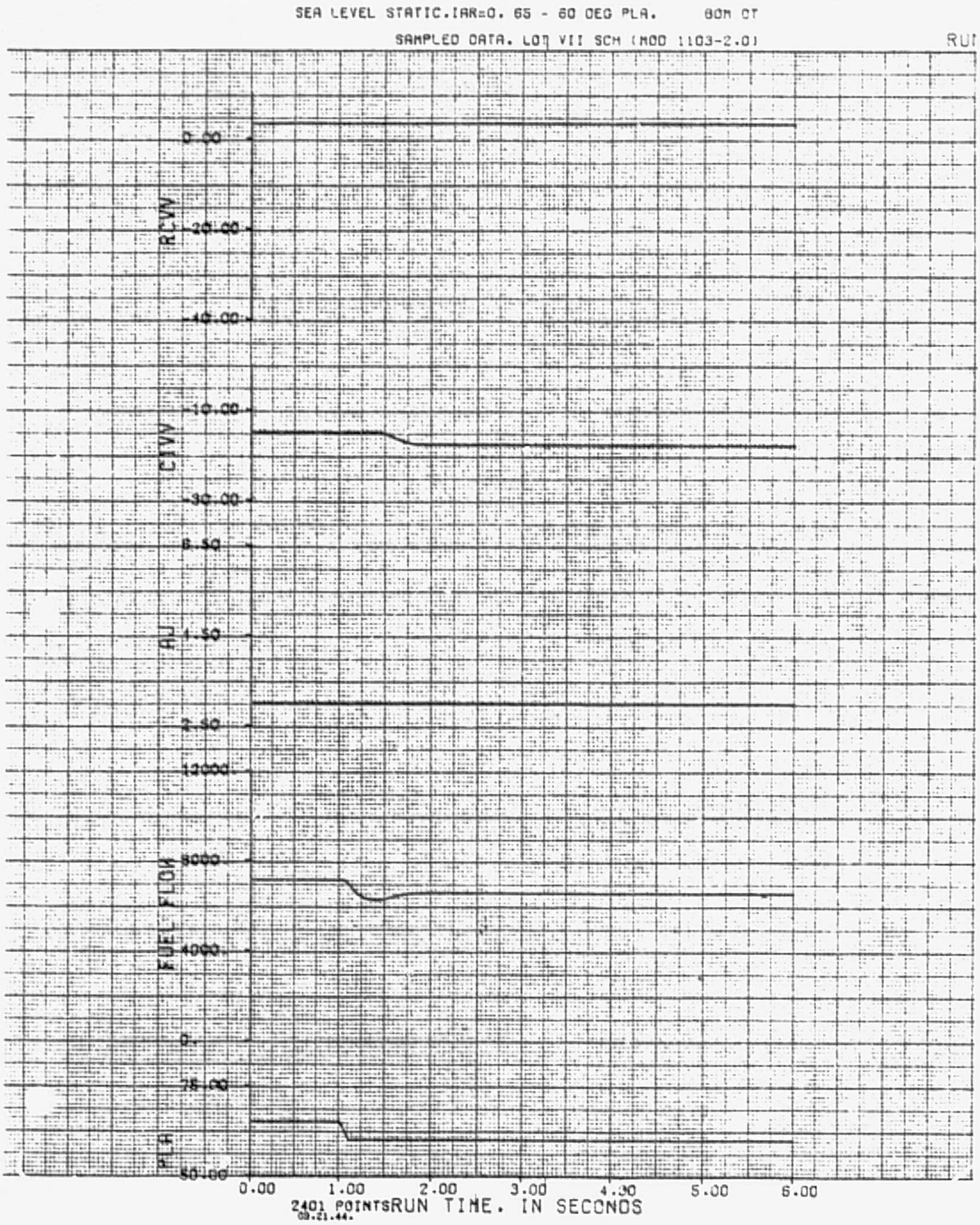
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1.50
2.50
12000.
8000.
4000.
0.
75.00
60.00
0.00
1.00
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4.00
5.00
6.00
2401 POINTS
RUN TIME. IN SECONDS

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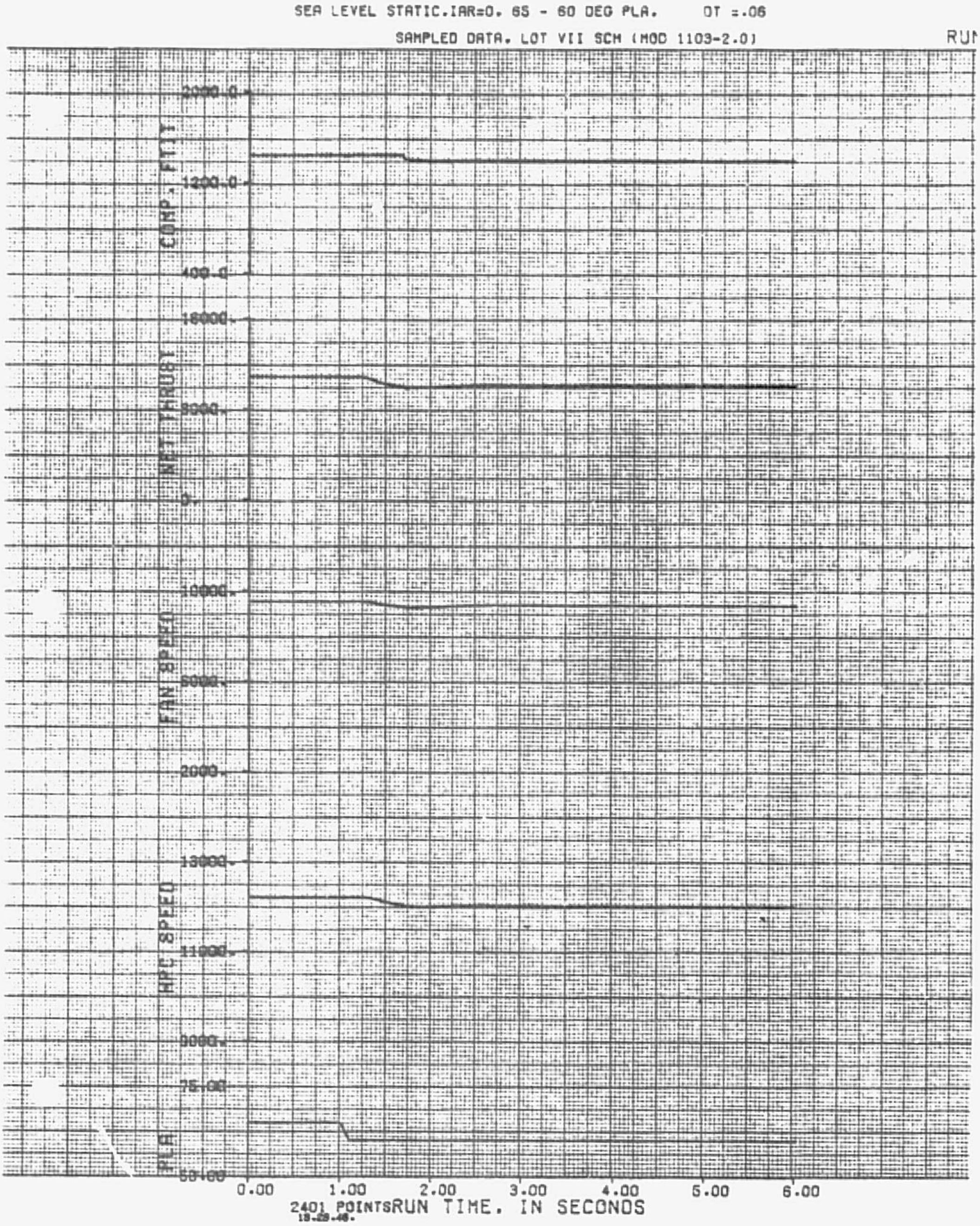

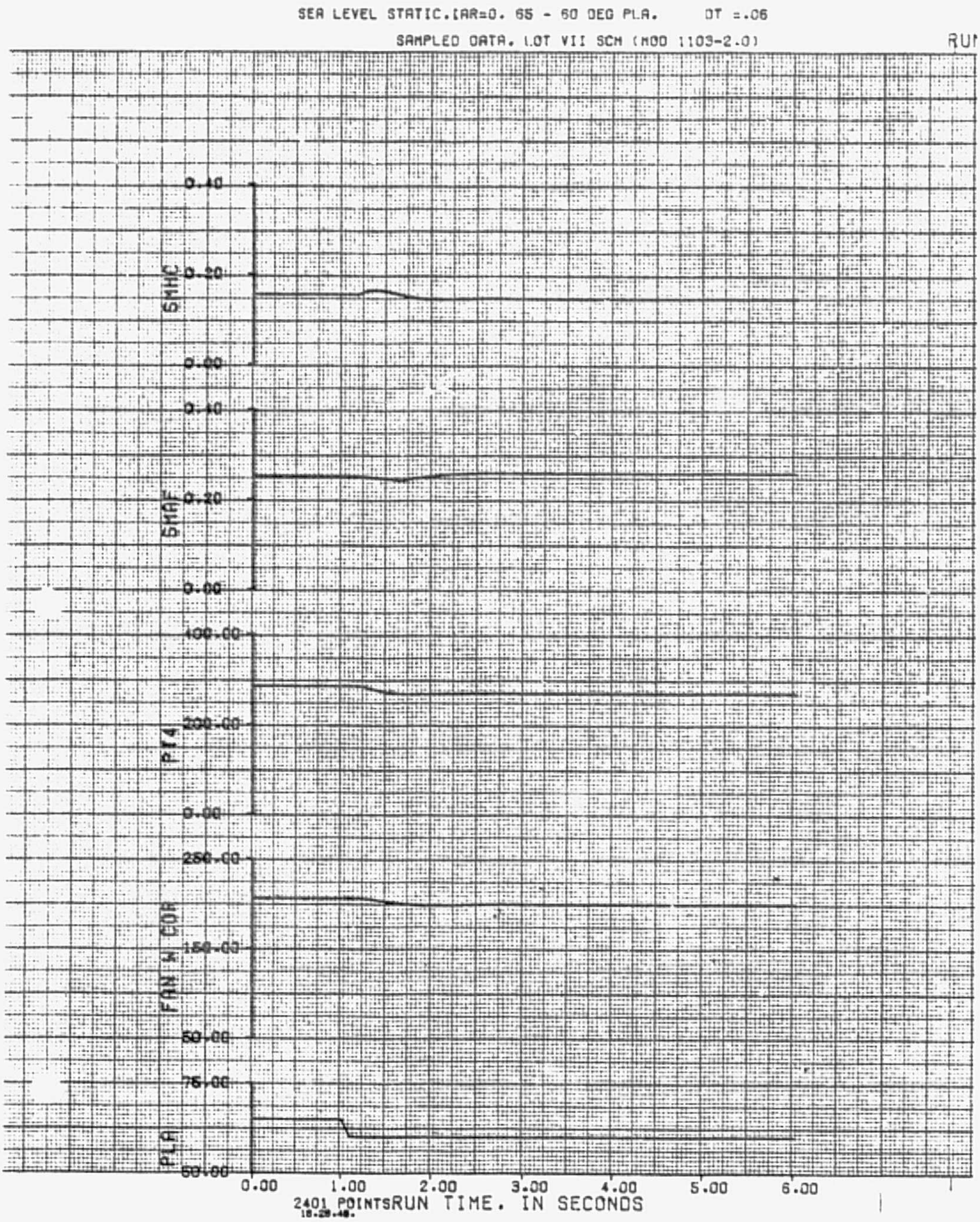
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PT4
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200.00
0.00
FAN W COR
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150.00
50.00
PLA
75.00
50.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME. IN SECONDS

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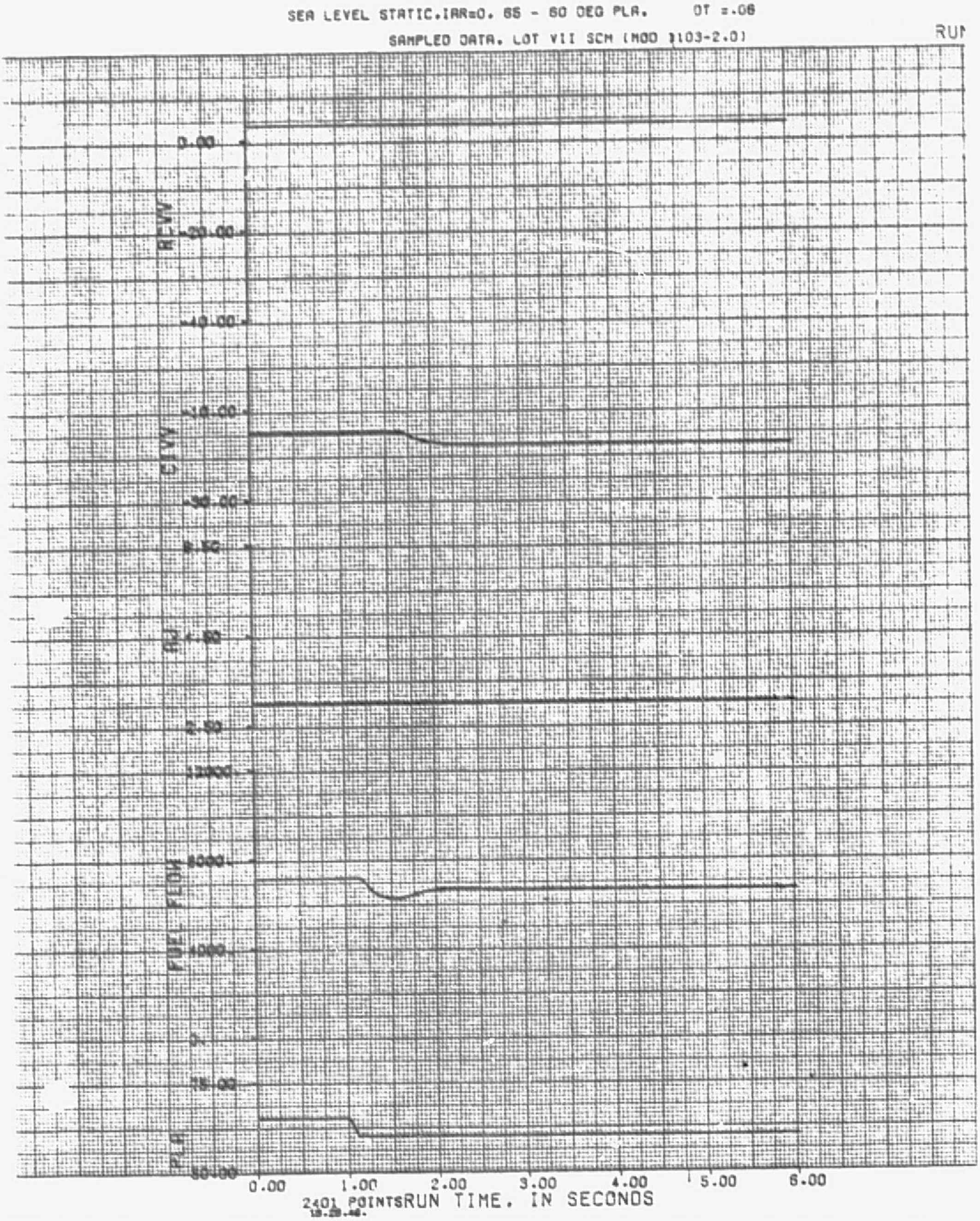
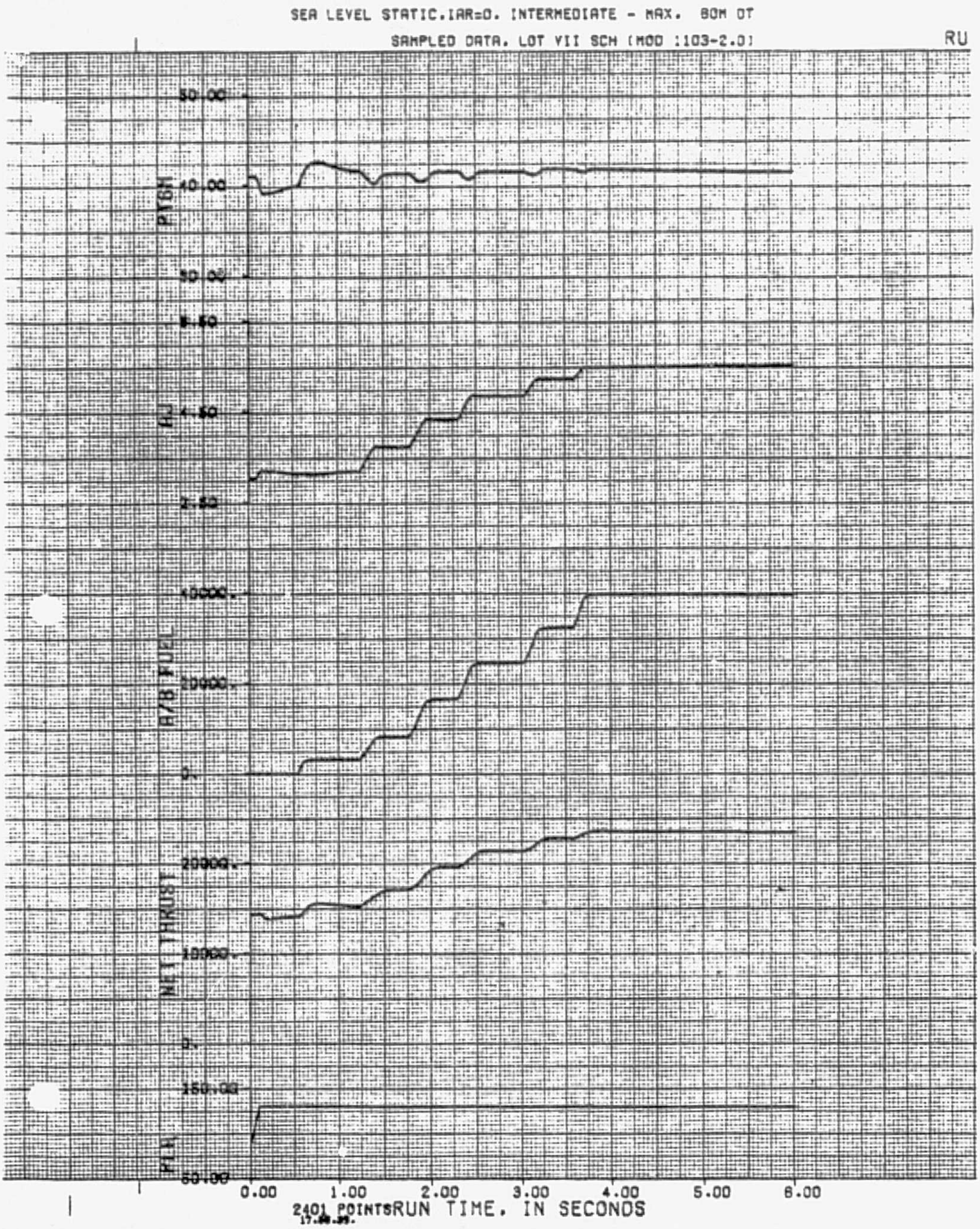
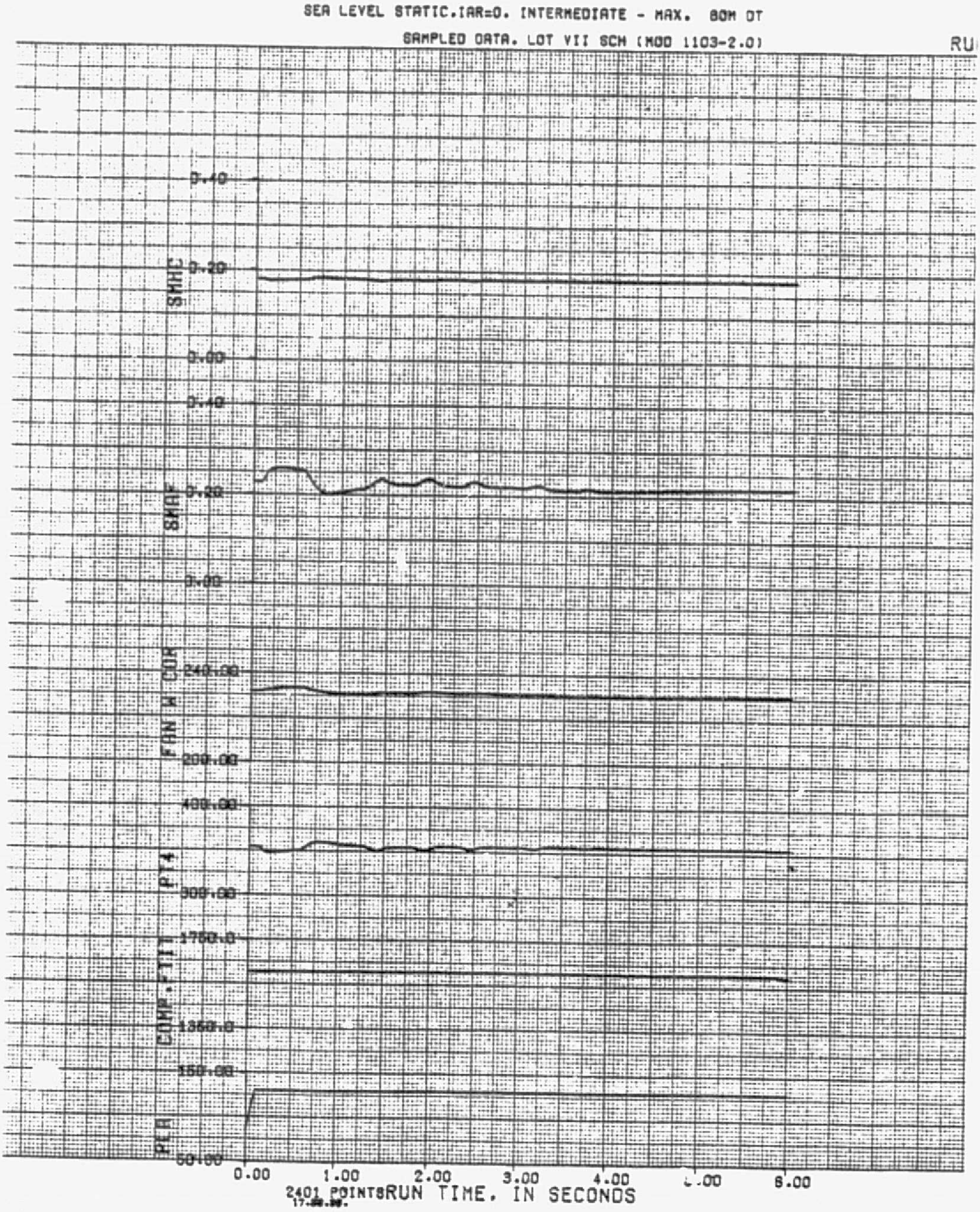
SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)

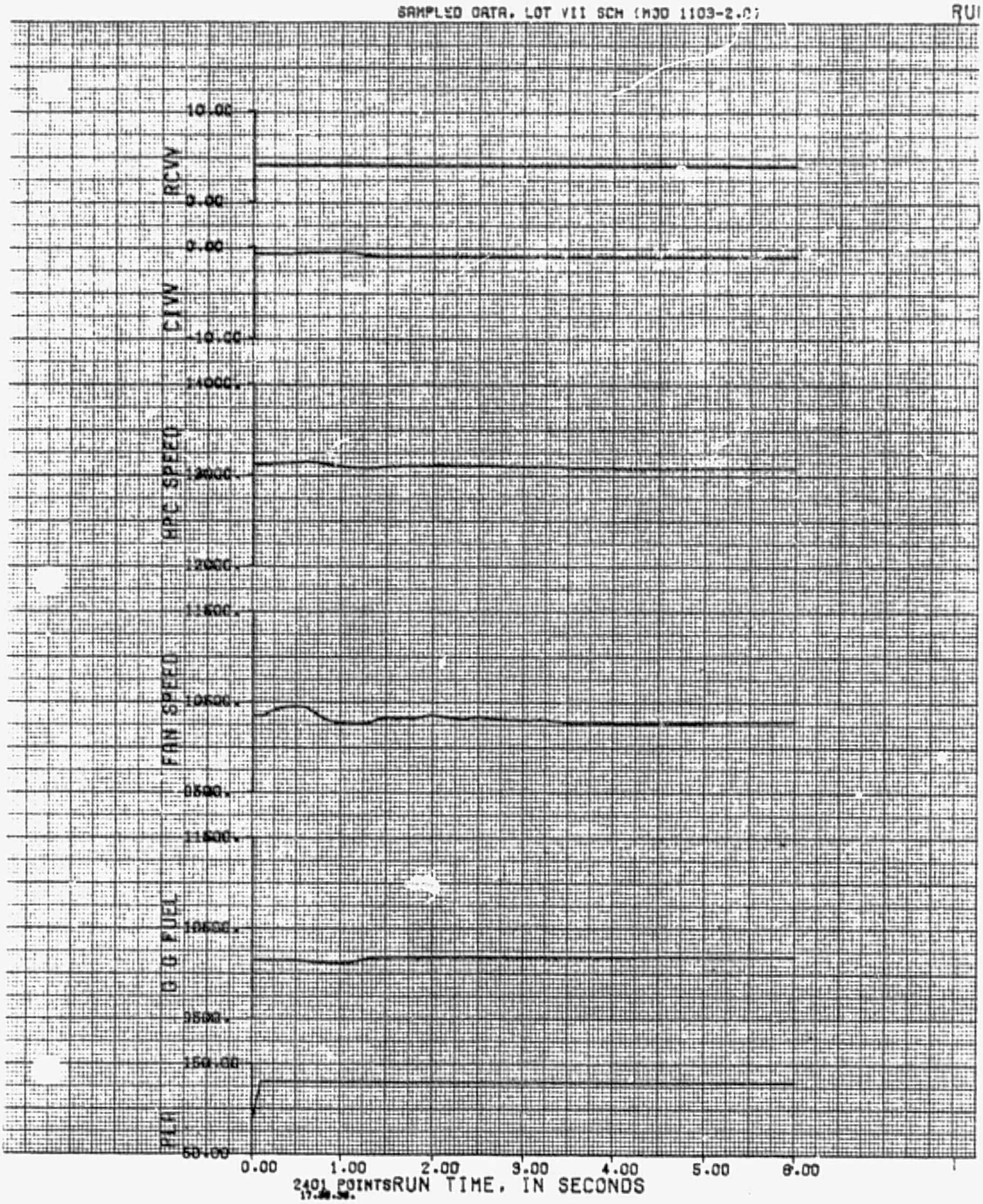



SEA LEVEL STATIC.IAR=0. INTERMEDIATE - MAX. 80M DT
SAMPLED DATA. LOT VII SCH (MOD :103-2.0)
RU
PT6M
50.00
40.00
30.00
AJ
5.50
4.50
3.50
A/B FUEL
40000.
20000.
0.
NET THRUST
20000.
10000.
0.
P1H
150.00
50.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



SEA LEVEL STATIC.IAR=0. INTERMEDIATE - MAX. 80M DT
SAMPLED DATA. LOT VII SCH (MJD 1103-2.0)



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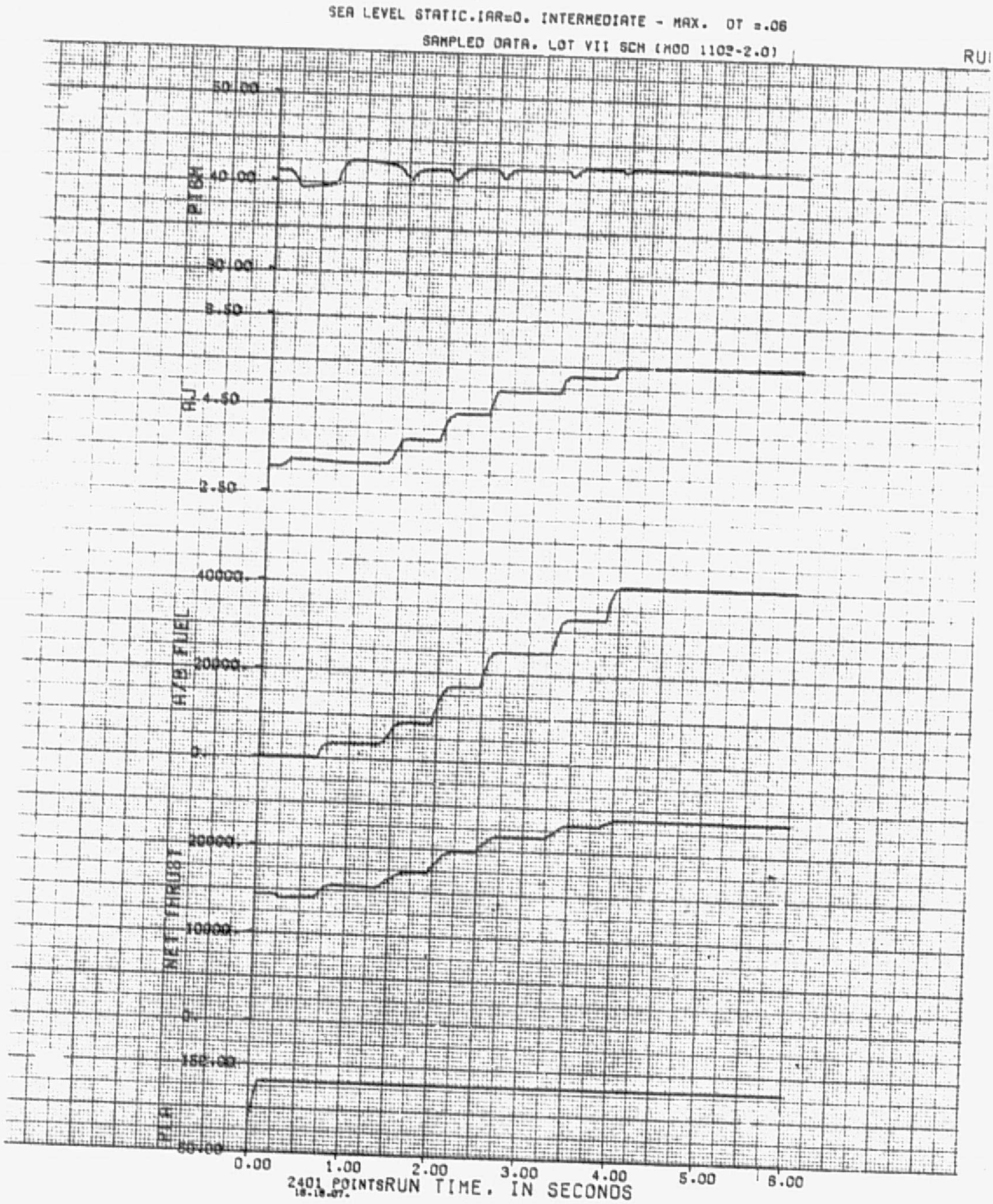
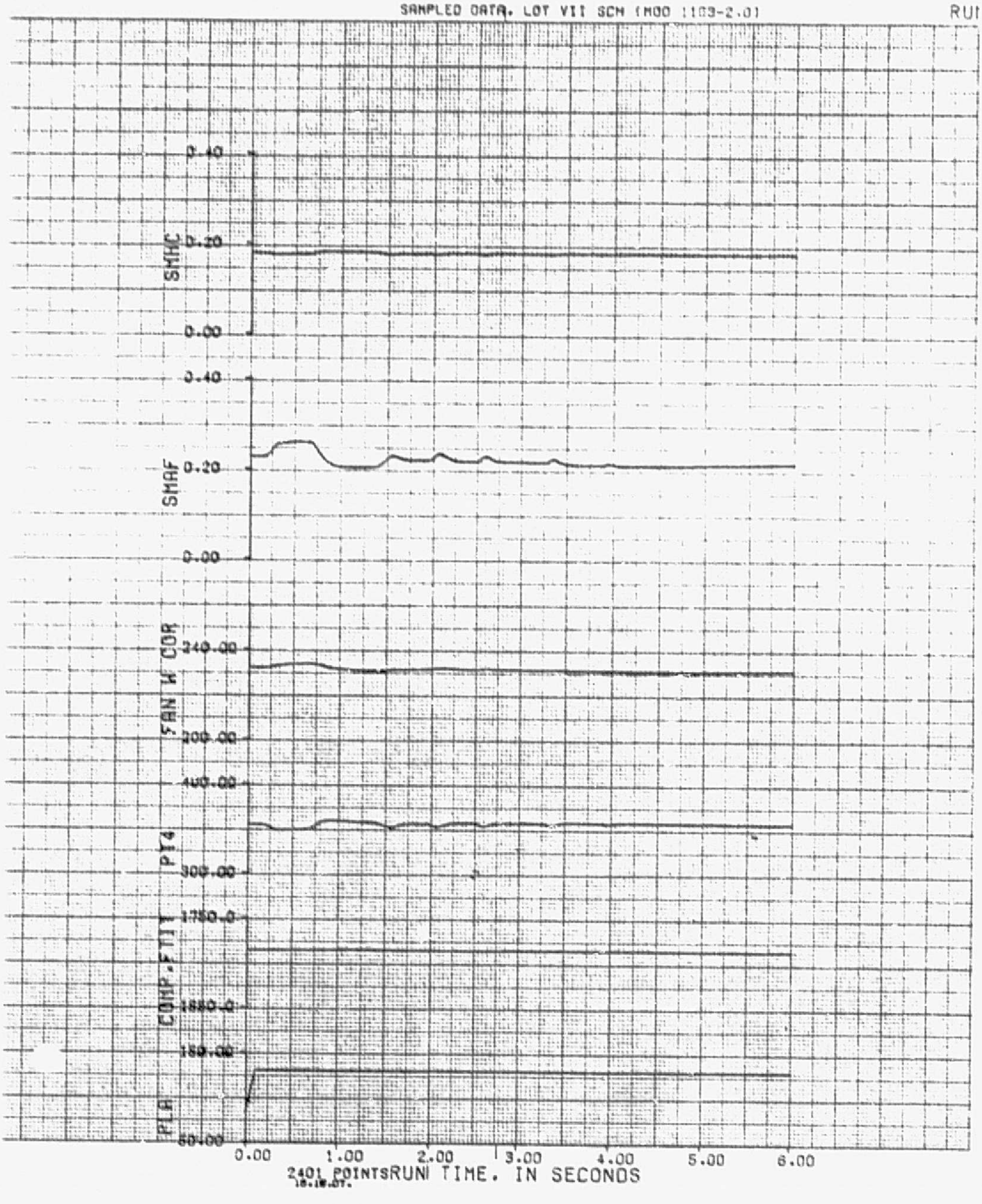


SEA LEVEL STATIC.IAR=0. INTERMEDIATE - MAX.

SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)



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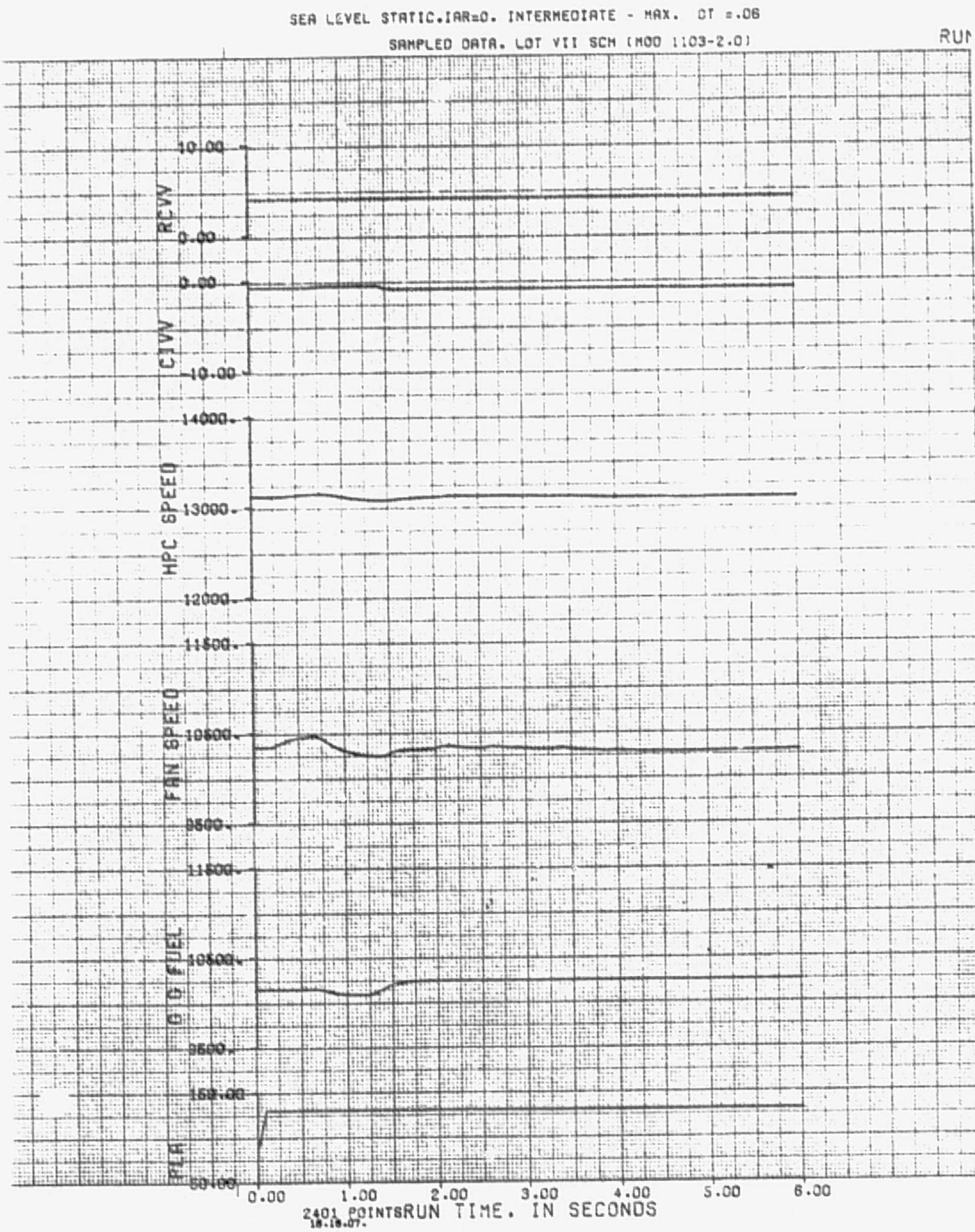
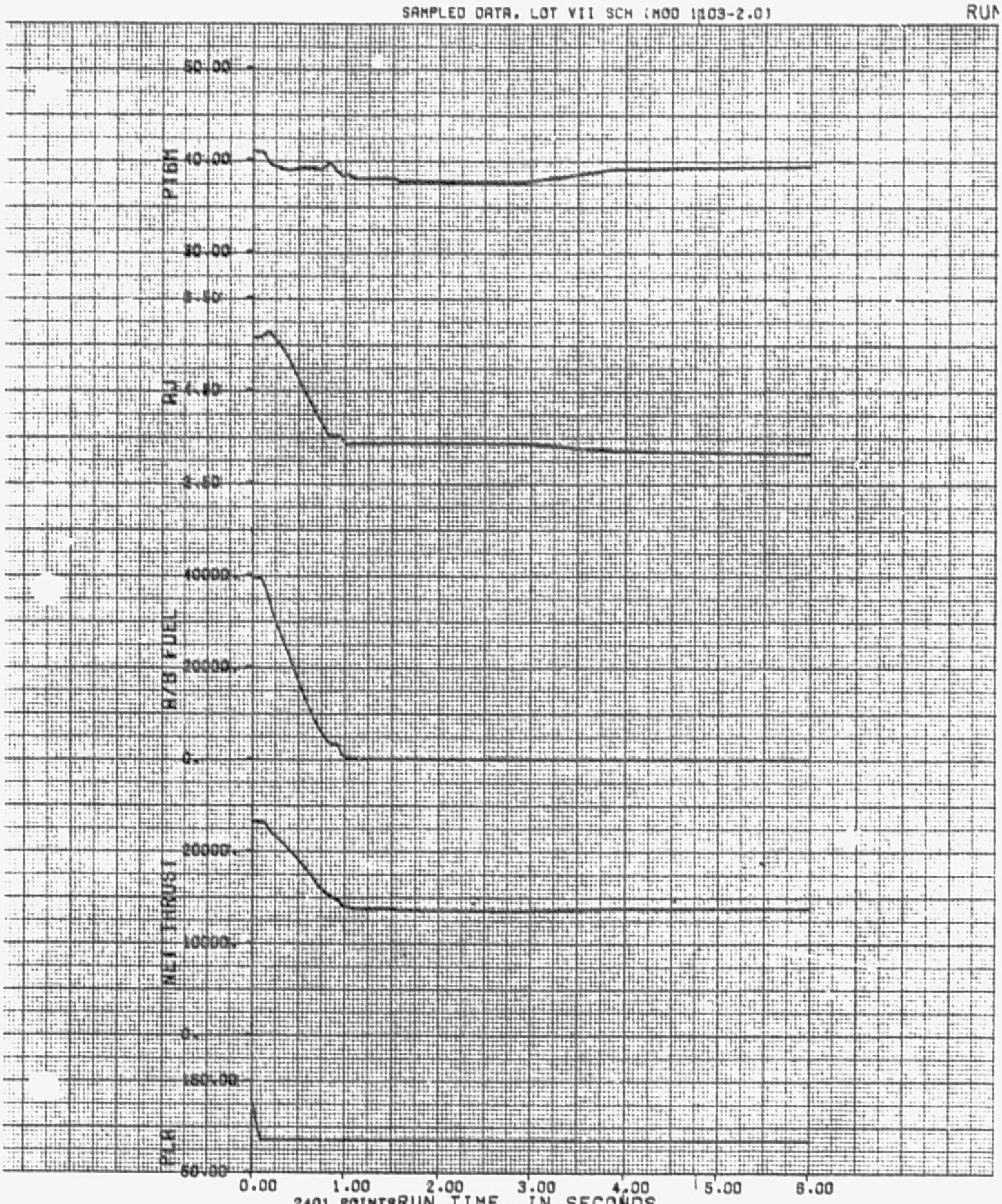


SEA LEVEL STATIC.IAR=0. MAX - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0) RUN



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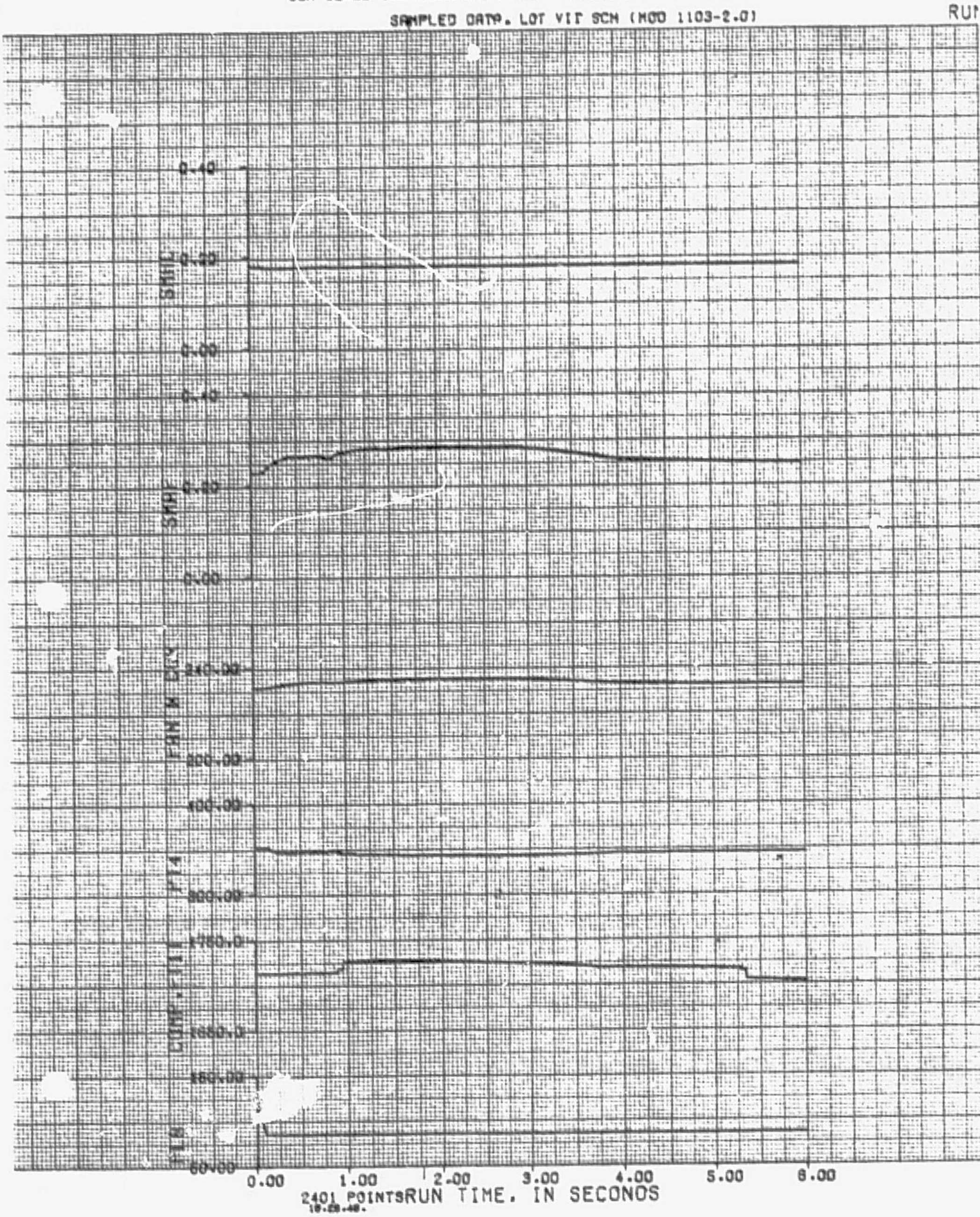
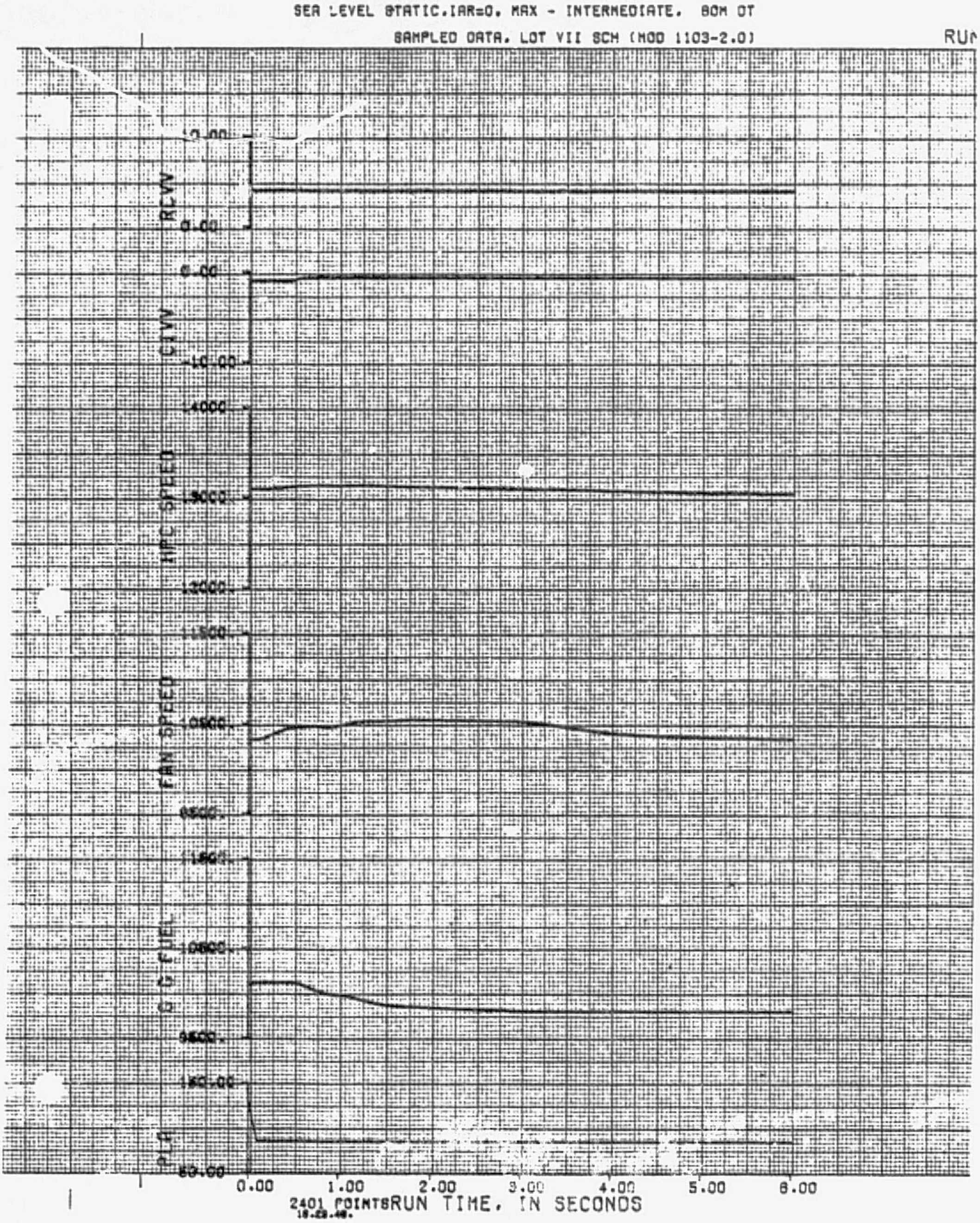
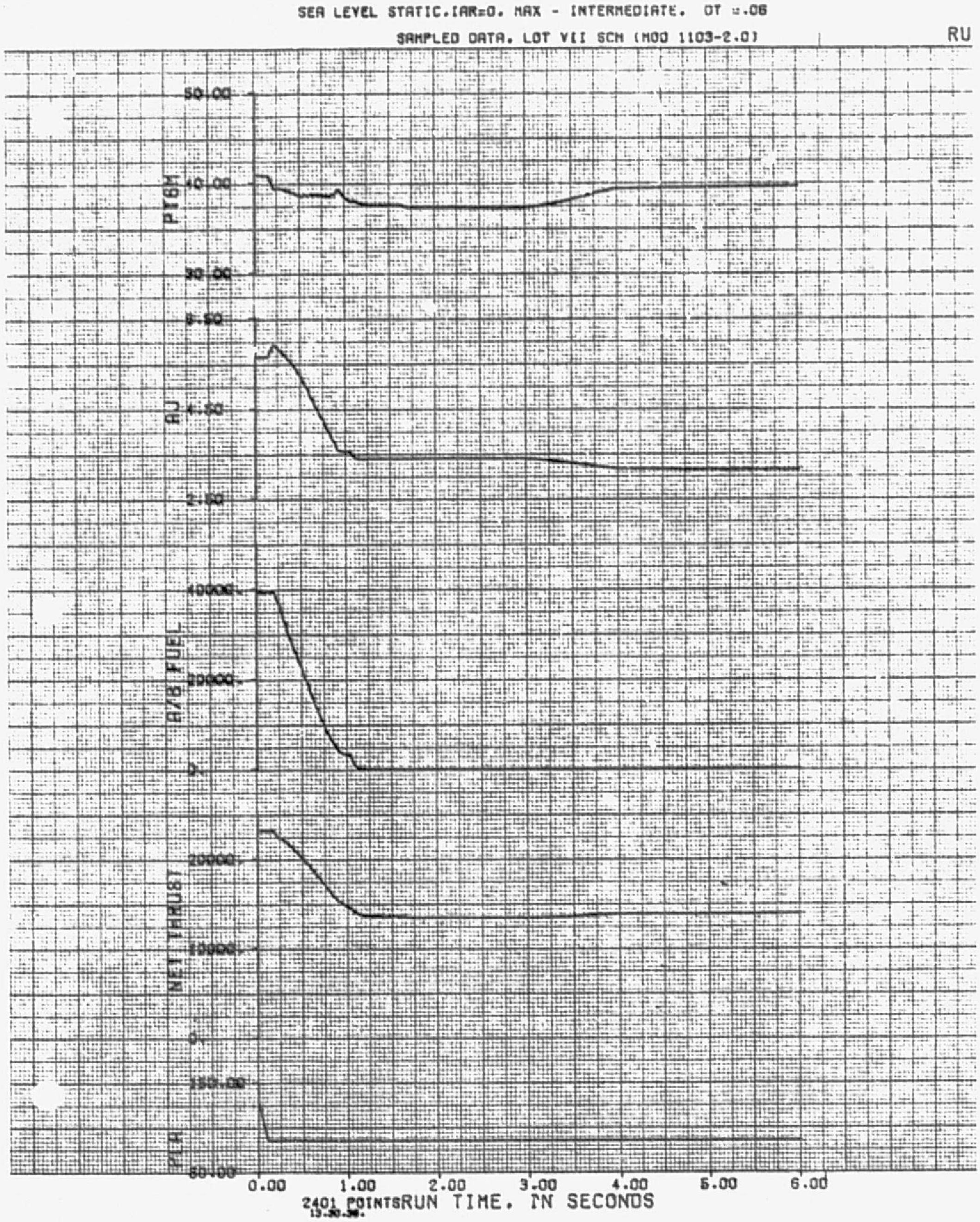
SEA LEVEL STATIC.IAR=0. MAX - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)



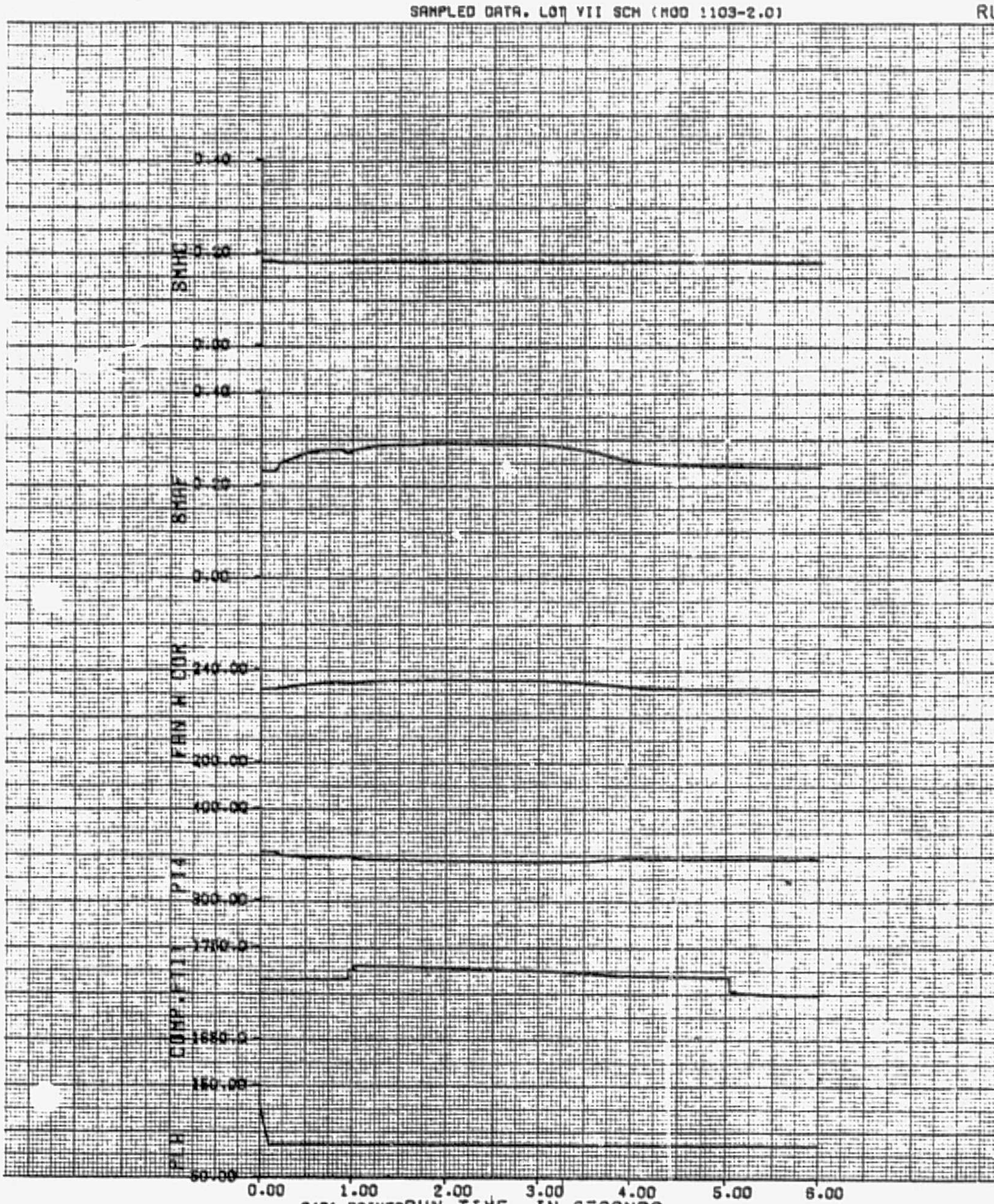

SEA LEVEL STATIC.IAR=0. MAX - INTERMEDIATE. 80M OT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
RLVV
CIVV
HPC SPEED
FAN SPEED
G G FUEL
PLA
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



SEA LEVEL STATIC.IAR=0. MAX - INTERMEDIATE. DT =.06

SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)



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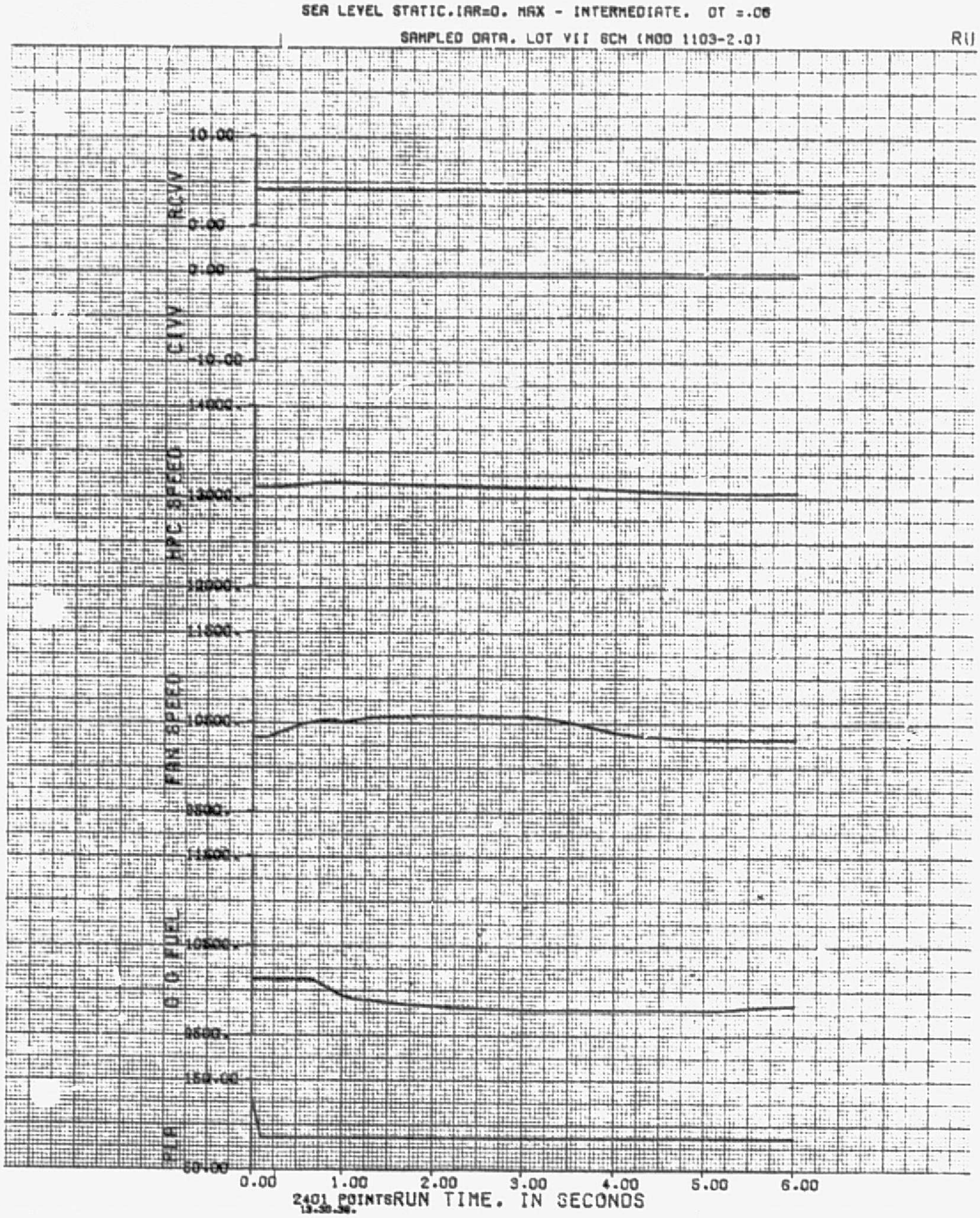
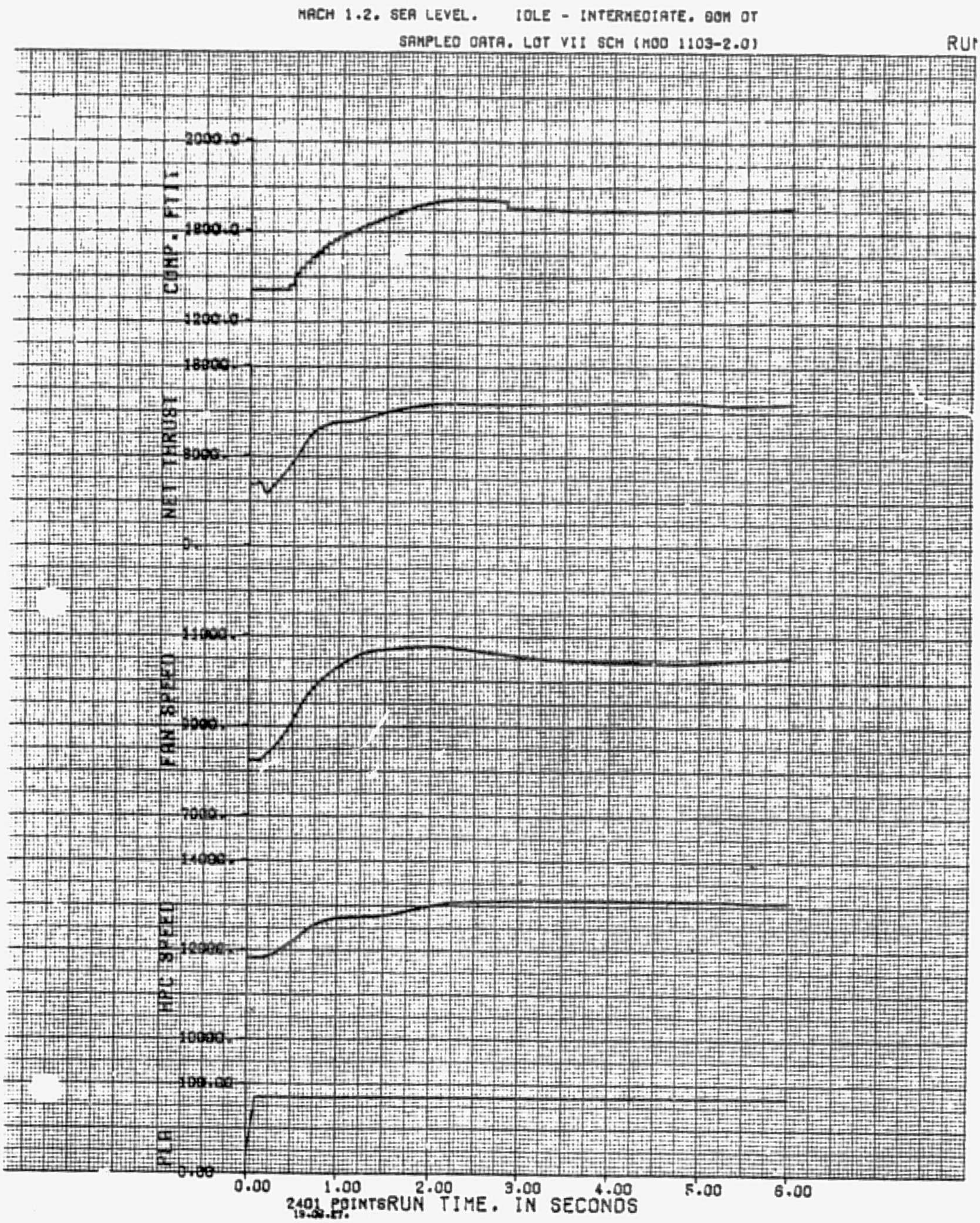
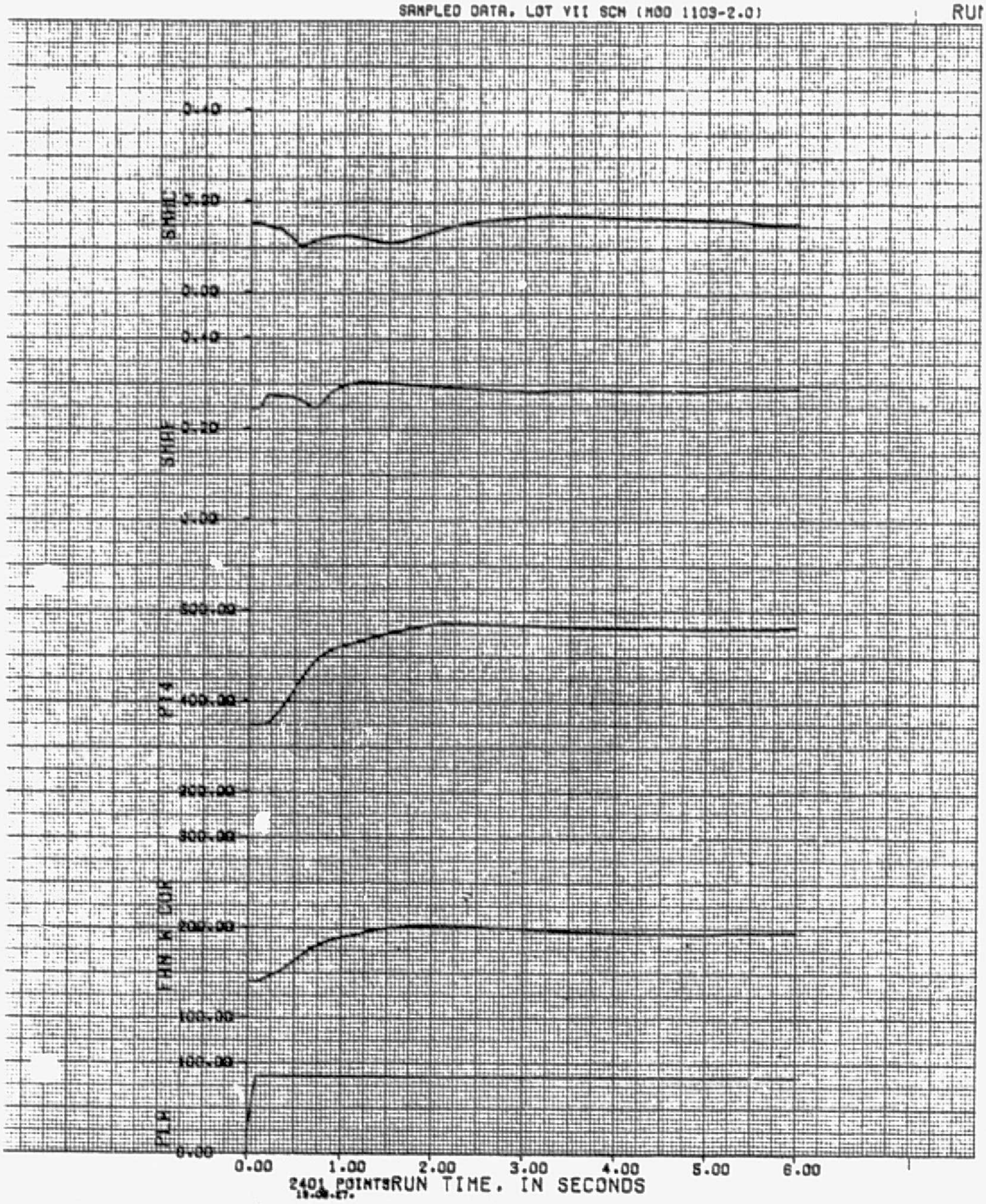



MACH 1.2. SEA LEVEL. IDLE - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
COMP. FTIT
2000.0
1600.0
1200.0
NET THRUST
16000.
8000.
0.
FAN SPEED
11000.
9000.
7000.
HPC SPEED
14000.
12000.
10000.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

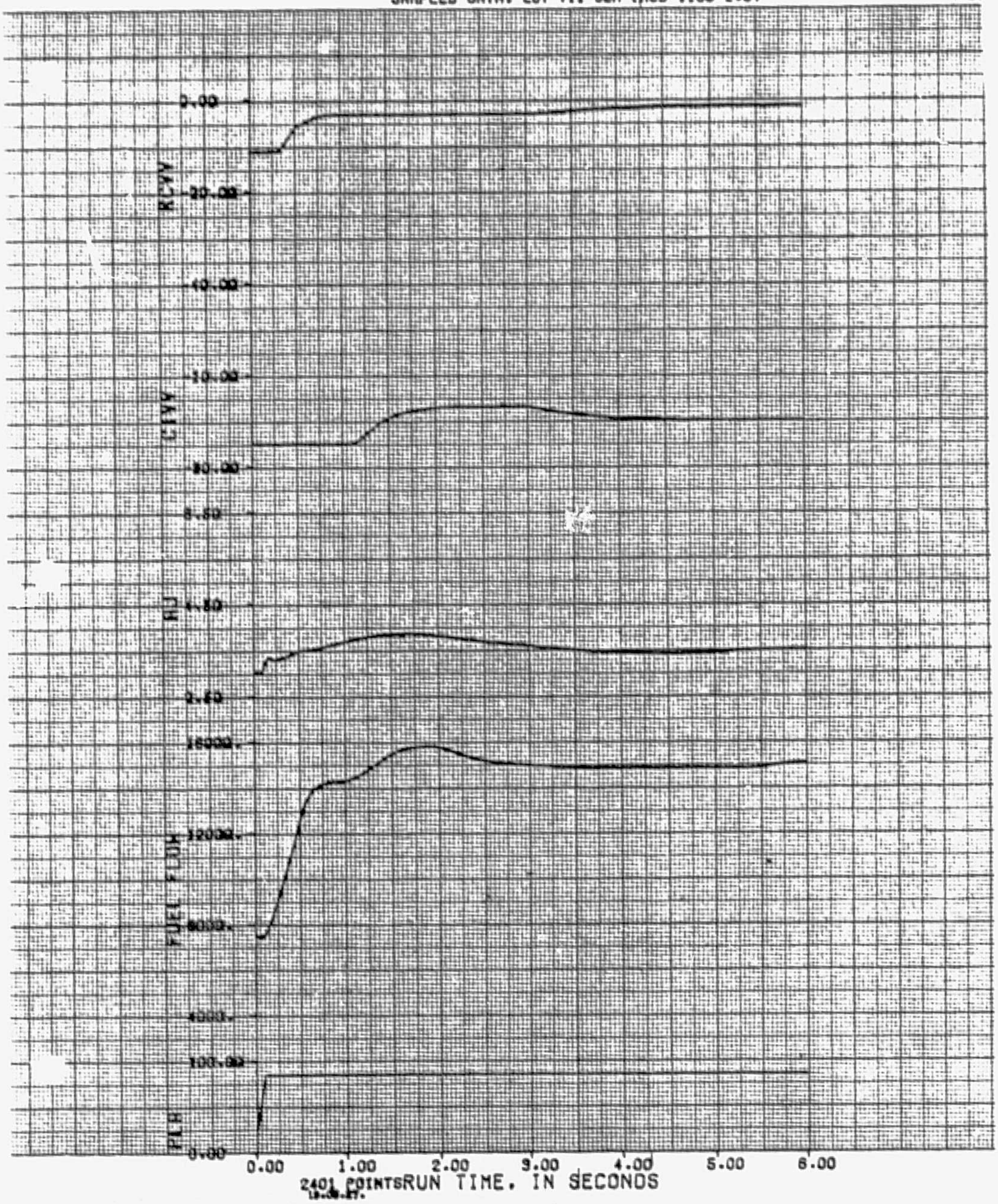
ORIGINAL PAGE IS
OF POOR QUALITY

MACH 1.2. SEA LEVEL. IDLE - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)



MACH 1.2, SEA LEVEL.   IDLE - INTERMEDIATE, 80M DT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)   RUI



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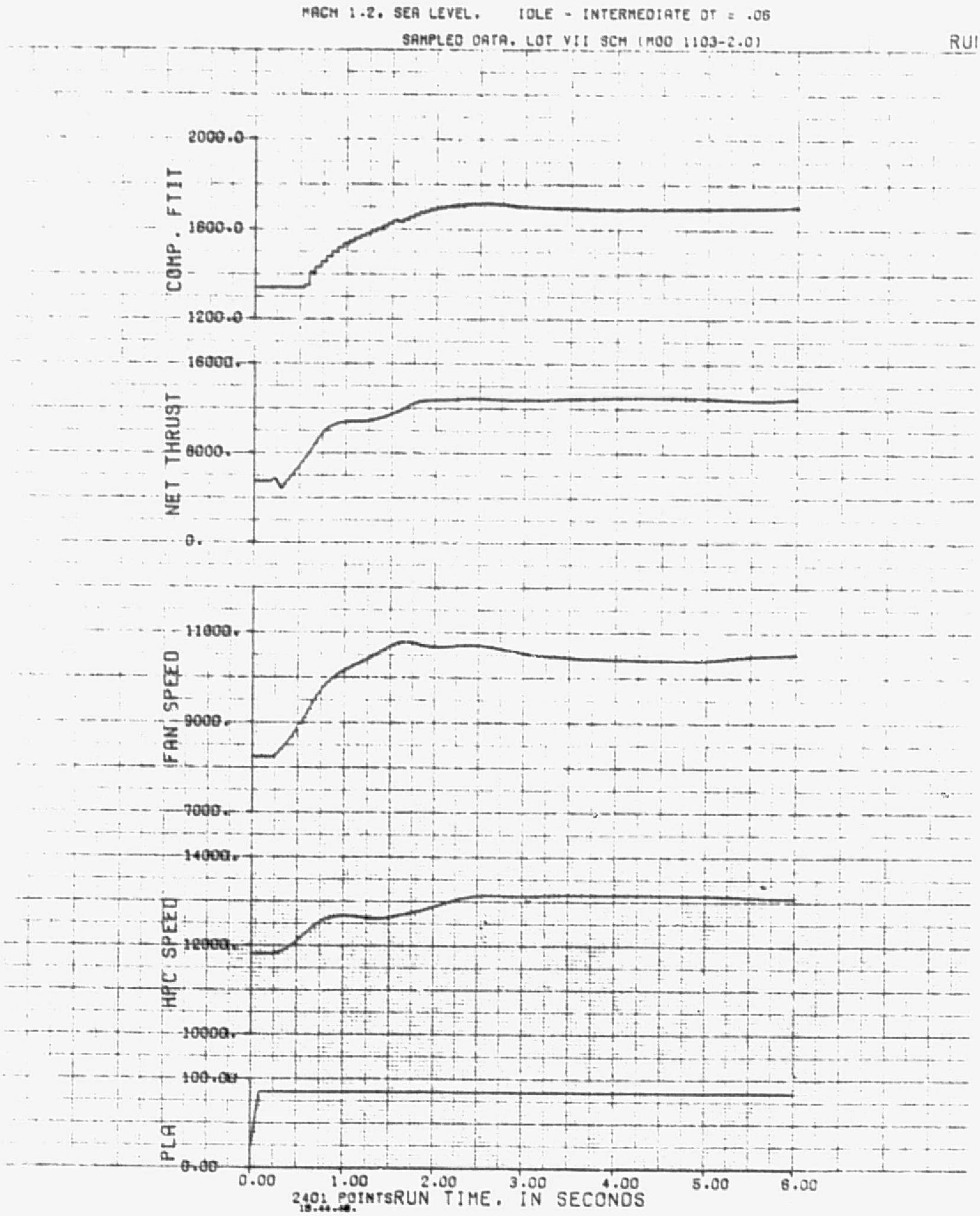
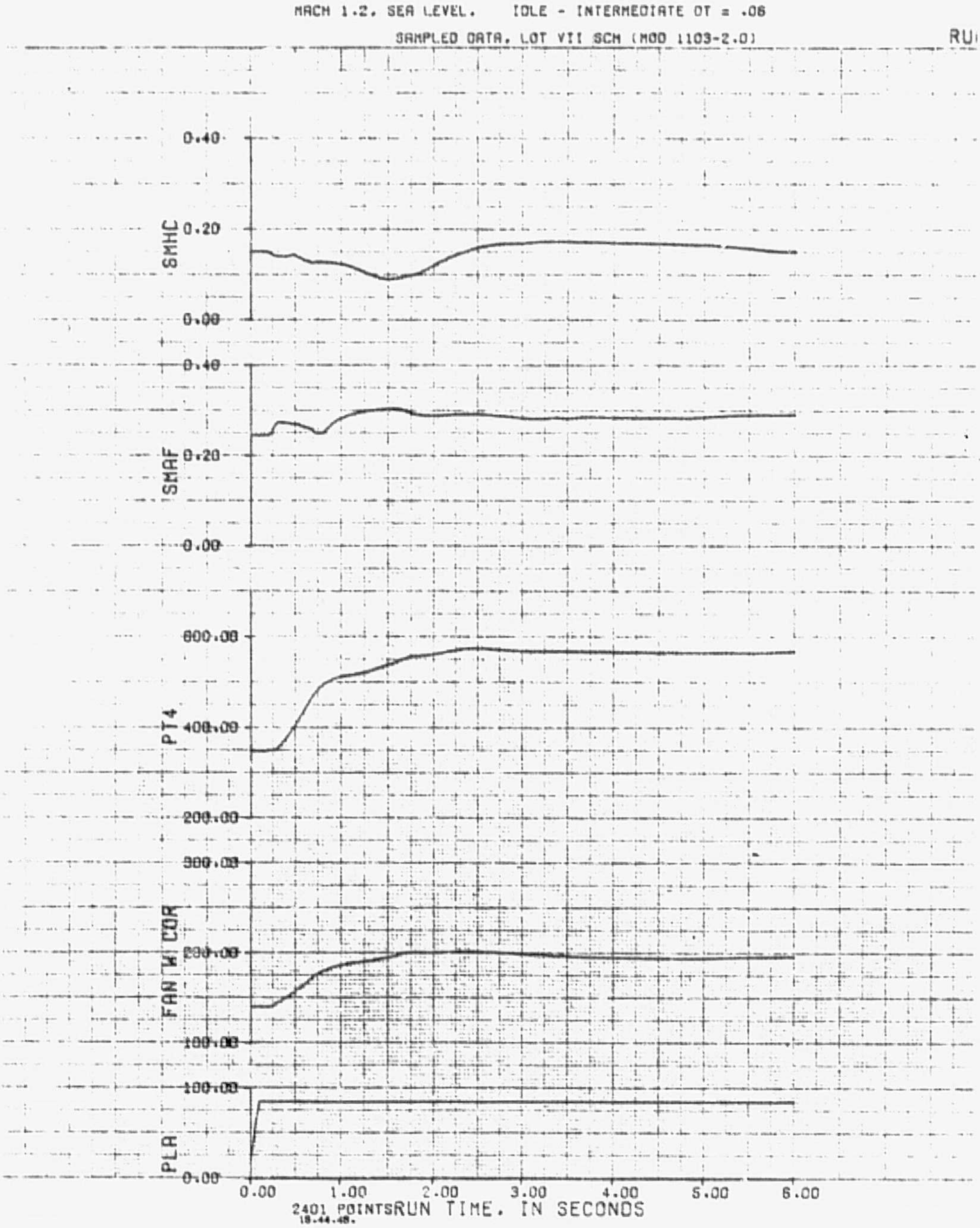
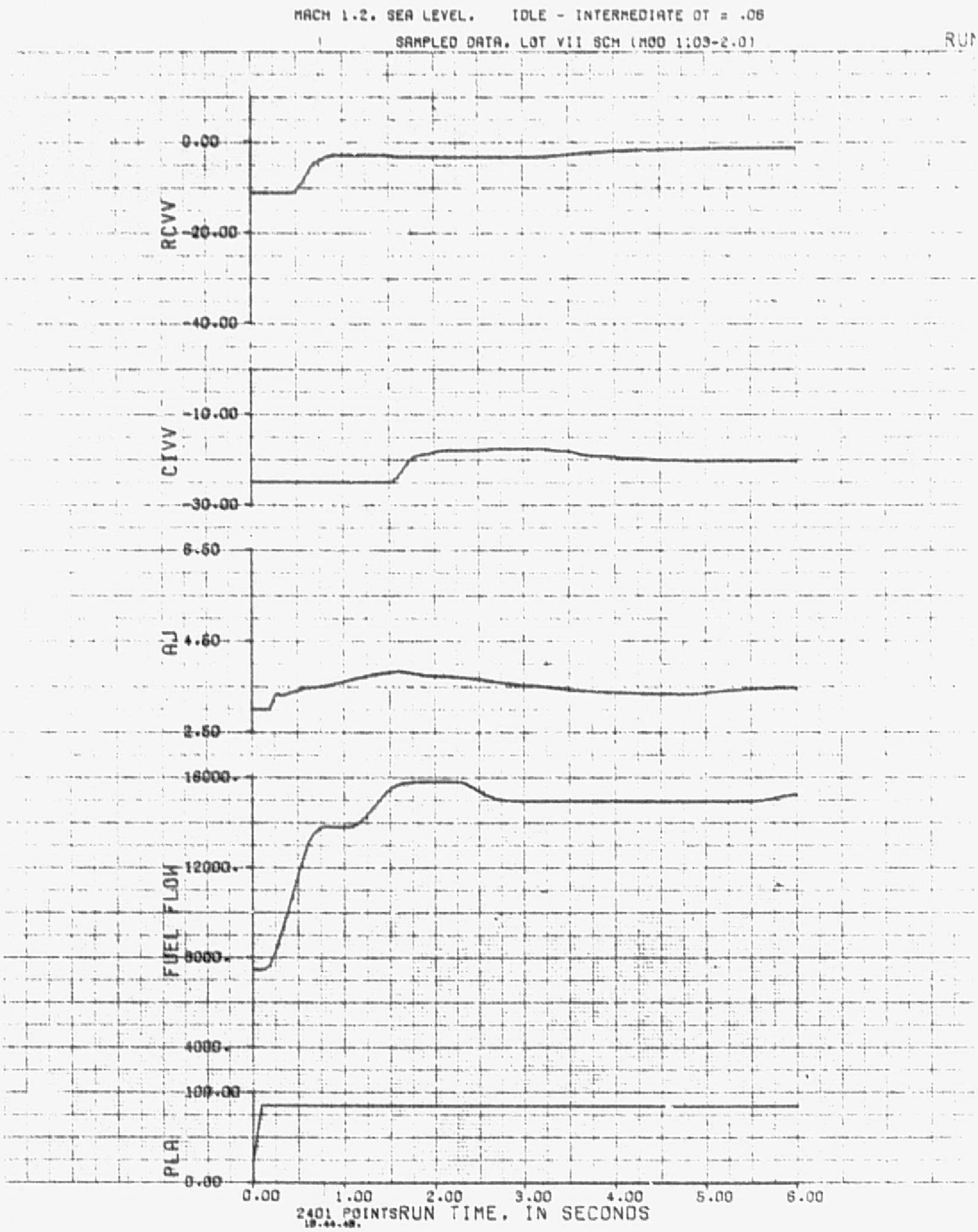


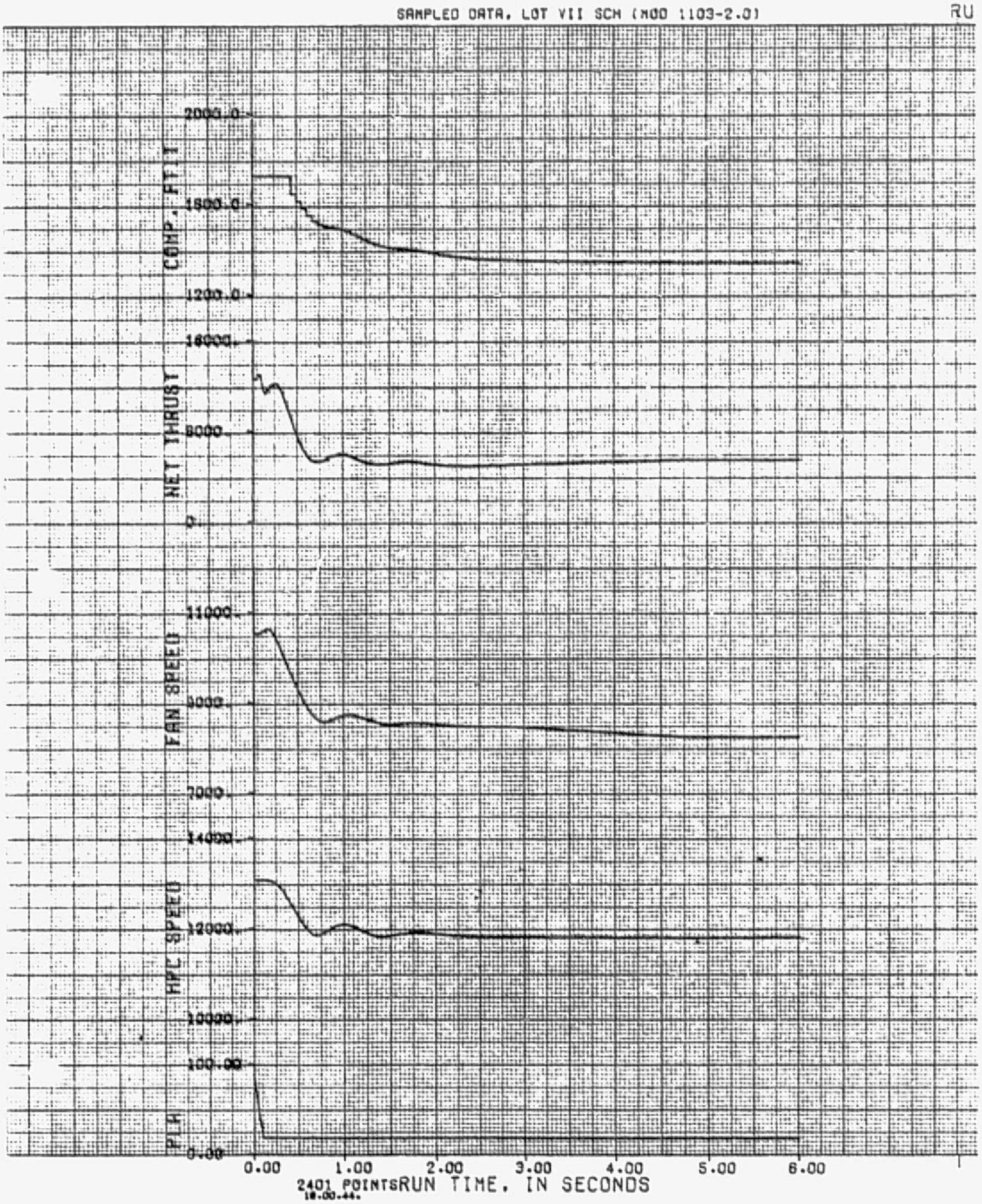

MACH 1.2. SEA LEVEL. IDLE - INTERMEDIATE DT = .06
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RU
SMHC
SMAF
PT4
FAN W COR
PLA
0.40
0.20
0.00
600.00
400.00
200.00
300.00
100.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME. IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



MACH 1.2. SEA LEVEL.   INTERMEDIATE - IDLE. 80M DT

SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)



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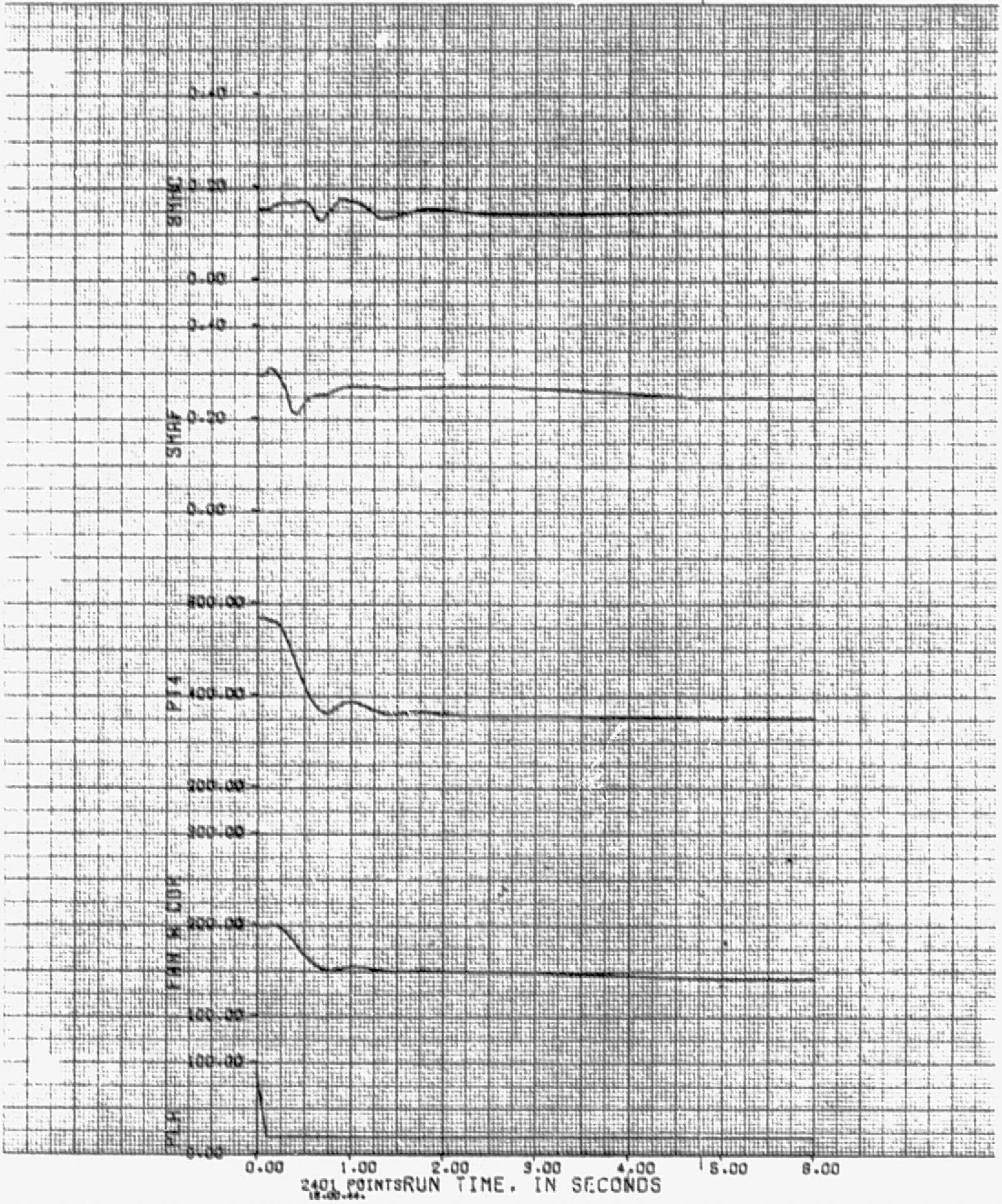
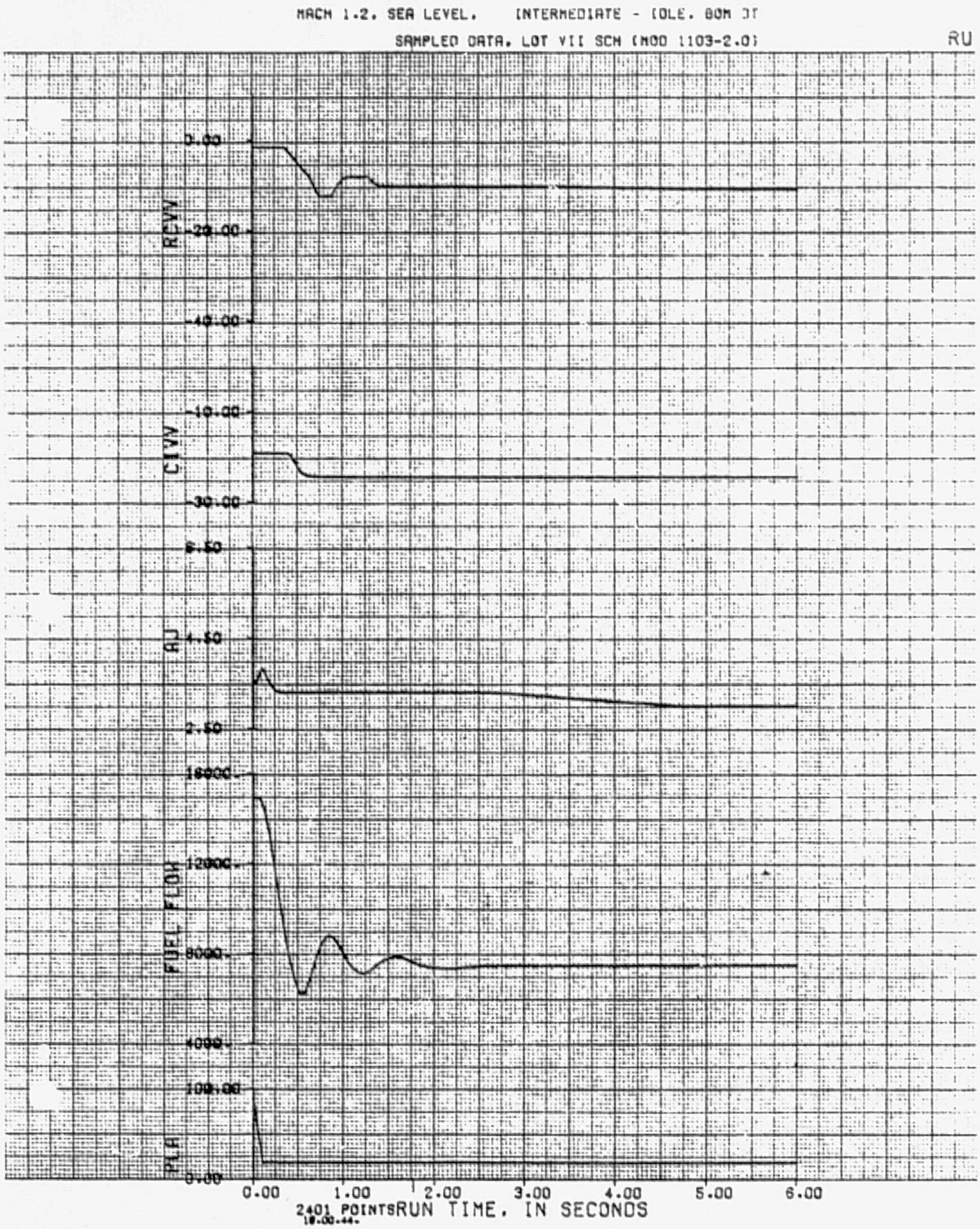
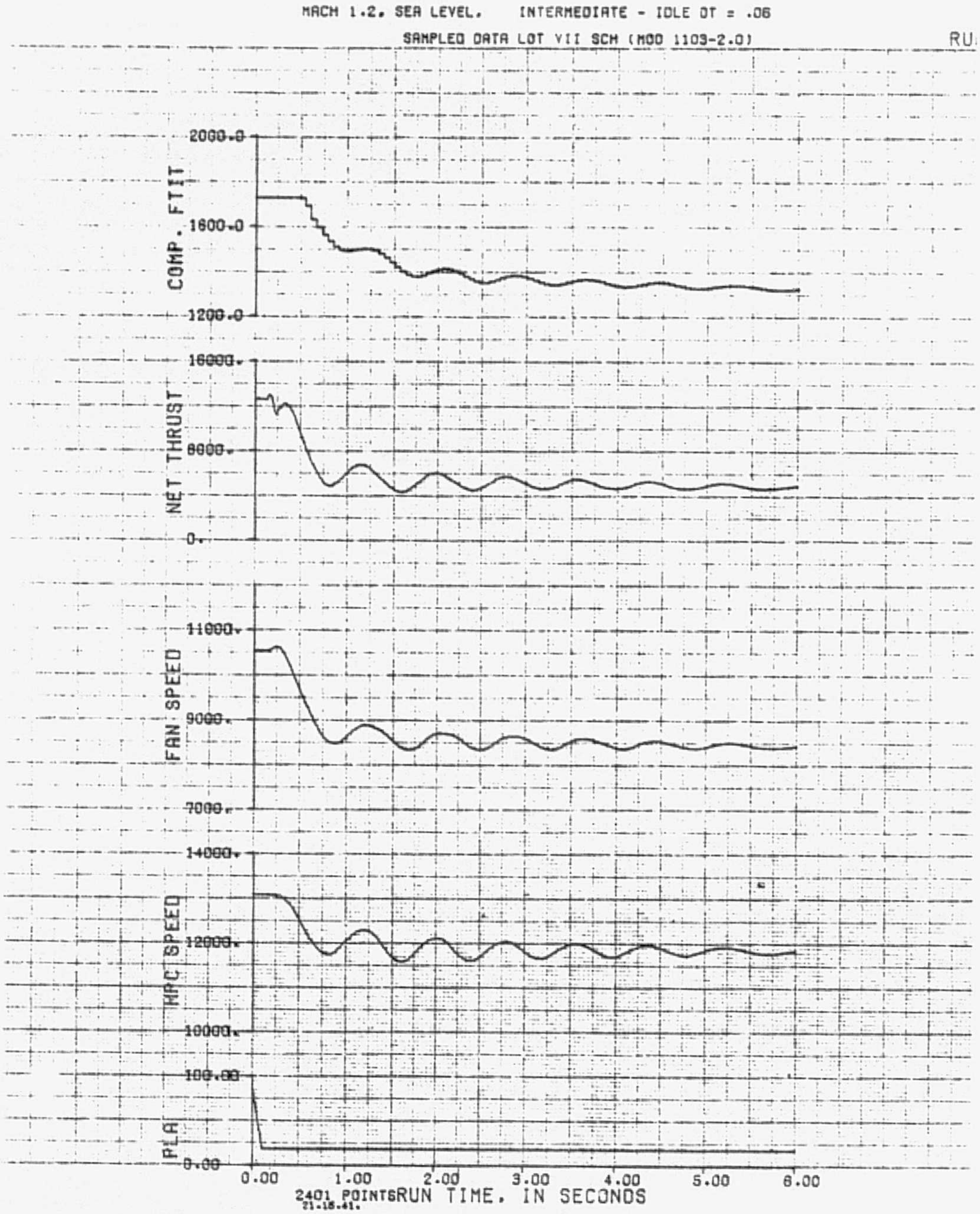
MACH 1.2, SEA LEVEL, INTERMEDIATE - IDLE, 80N OT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0) RU



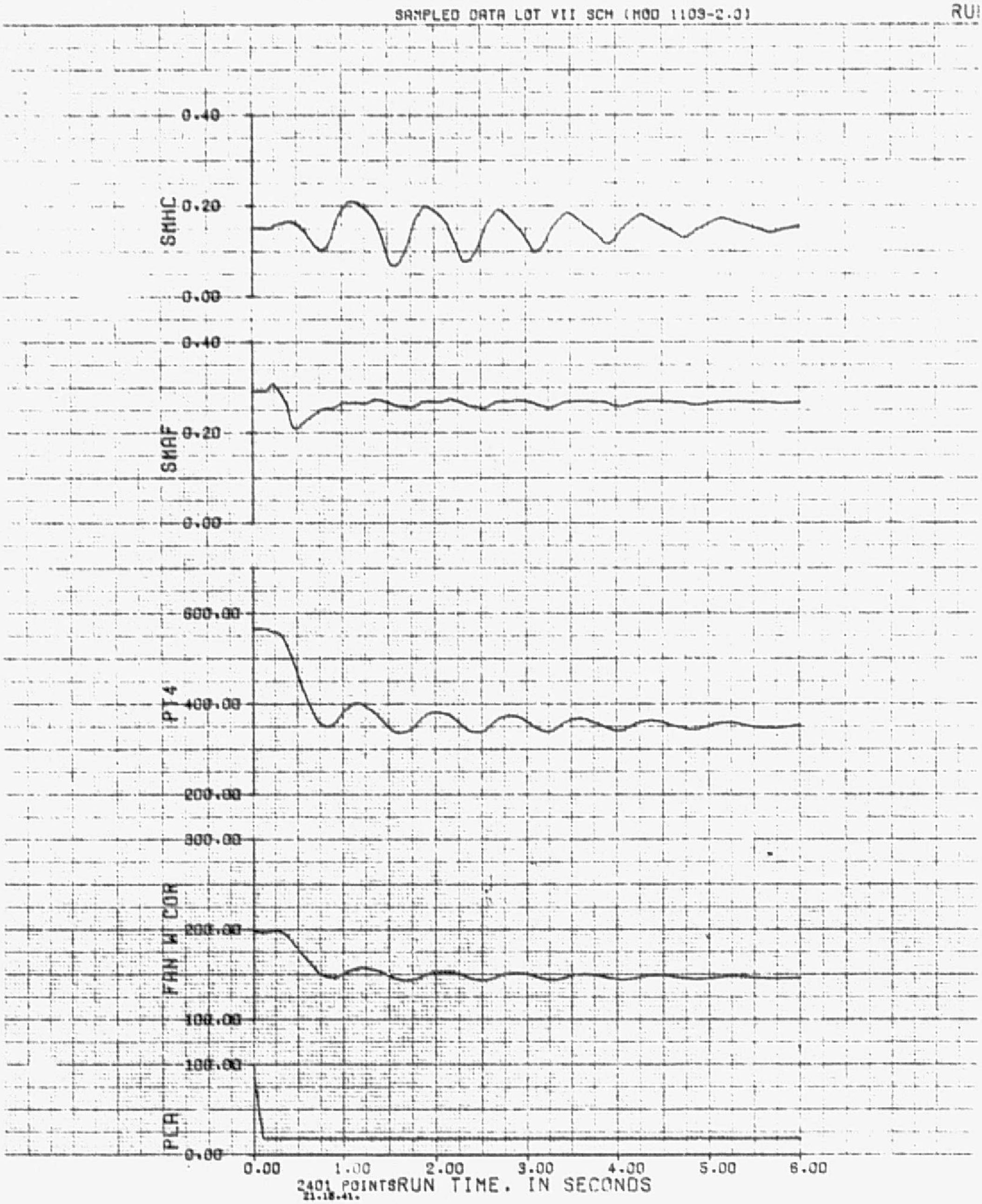

MACH 1.2, SEA LEVEL, INTERMEDIATE - IDLE, 80M JT
SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)
RU
RCVV
CIVV
AJ
FUEL FLOW
PLA
0.00
-20.00
-40.00
-10.00
-30.00
6.50
4.50
2.50
16000.
12000.
8000.
4000.
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



MACH 1.2. SEA LEVEL.   INTERMEDIATE - IDLE DT = .06

SAMPLED DATA LOT VII SCM (MOD 1109-2.0)



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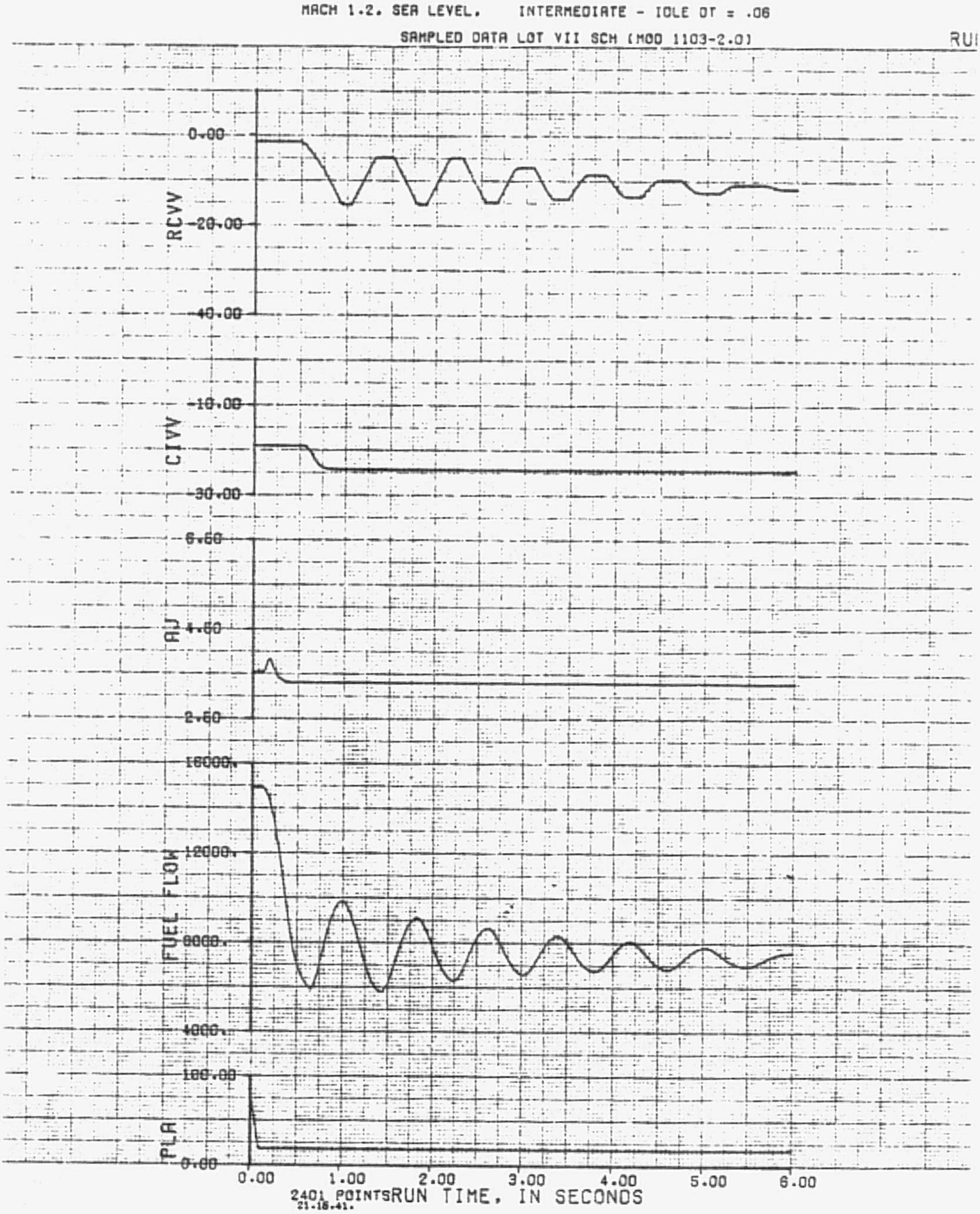
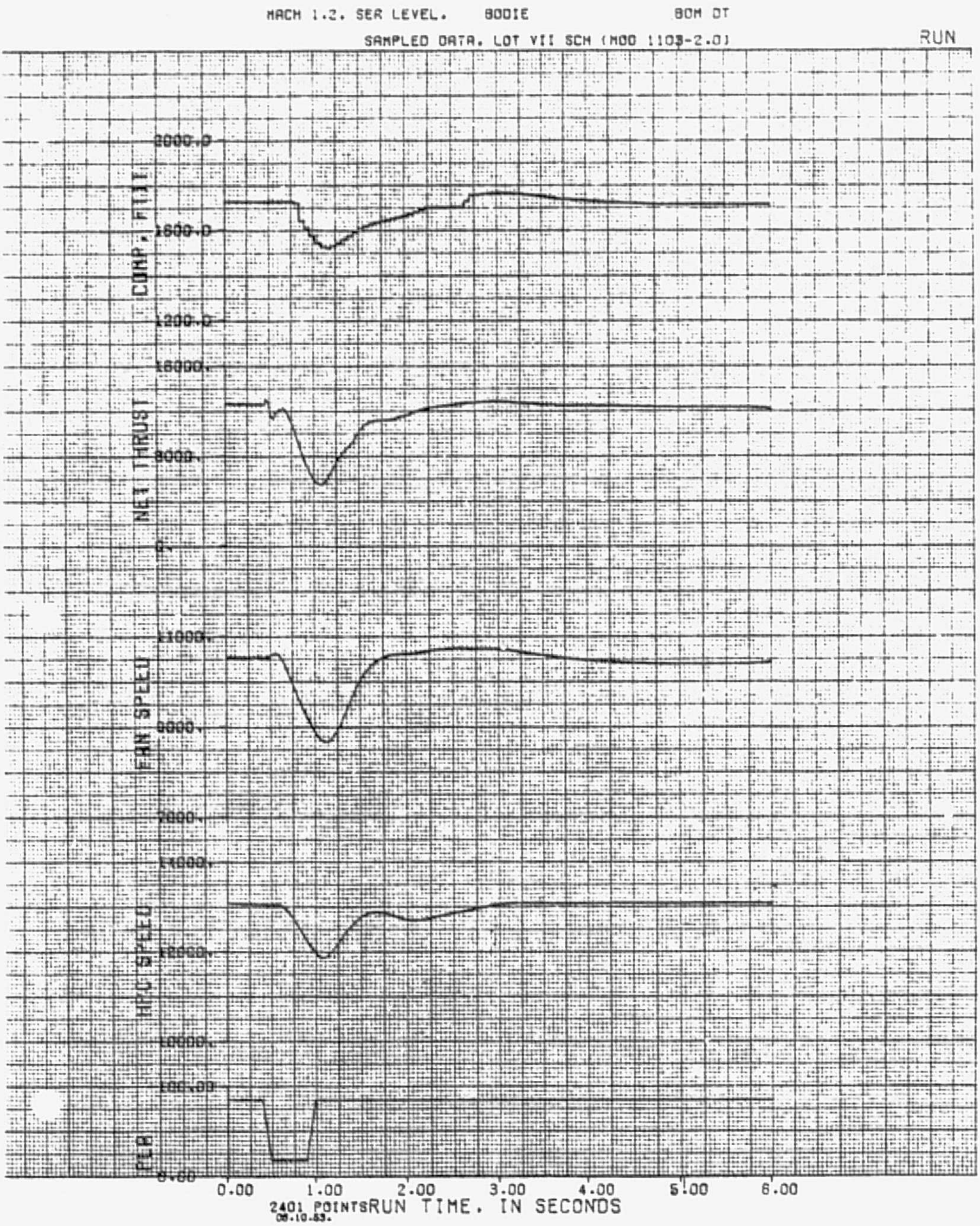
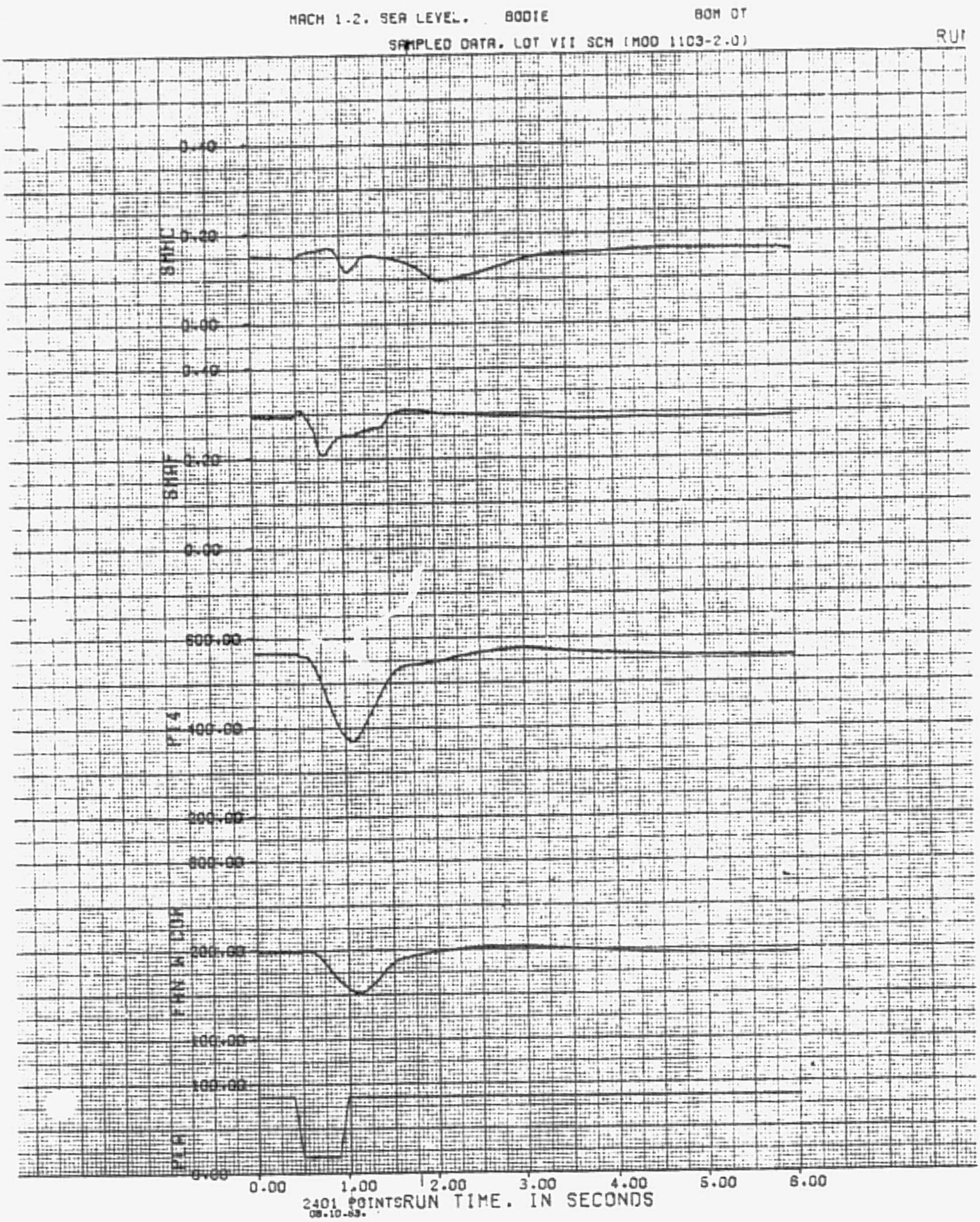
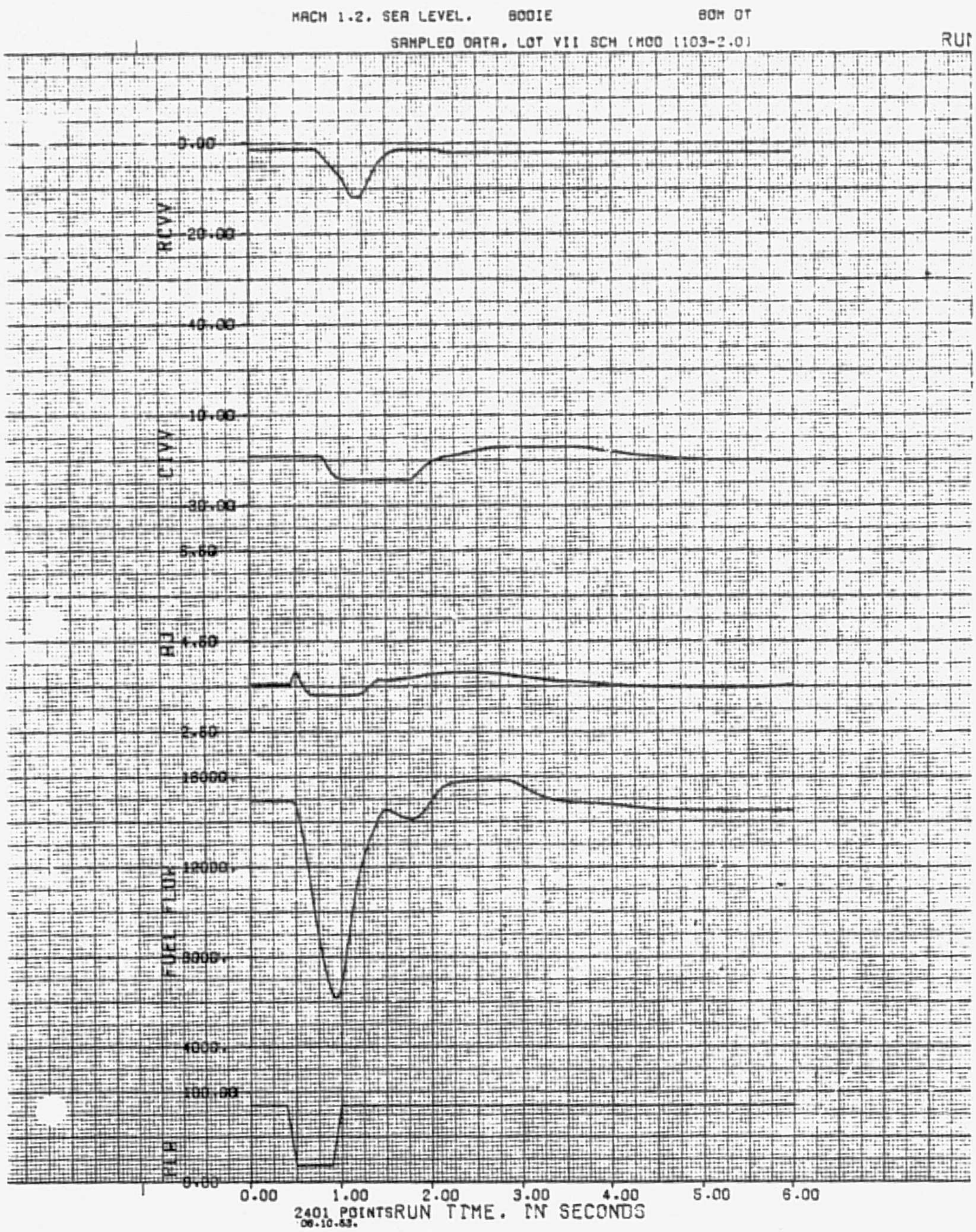



MACH 1.2. SEA LEVEL. BODIE BOM DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
COMP. FTIT
2000.0
1600.0
1200.0
NET THRUST
16000.
8000.
0.
FAN SPEED
11000.
9000.
7000.
HPC SPEED
14000.
12000.
10000.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

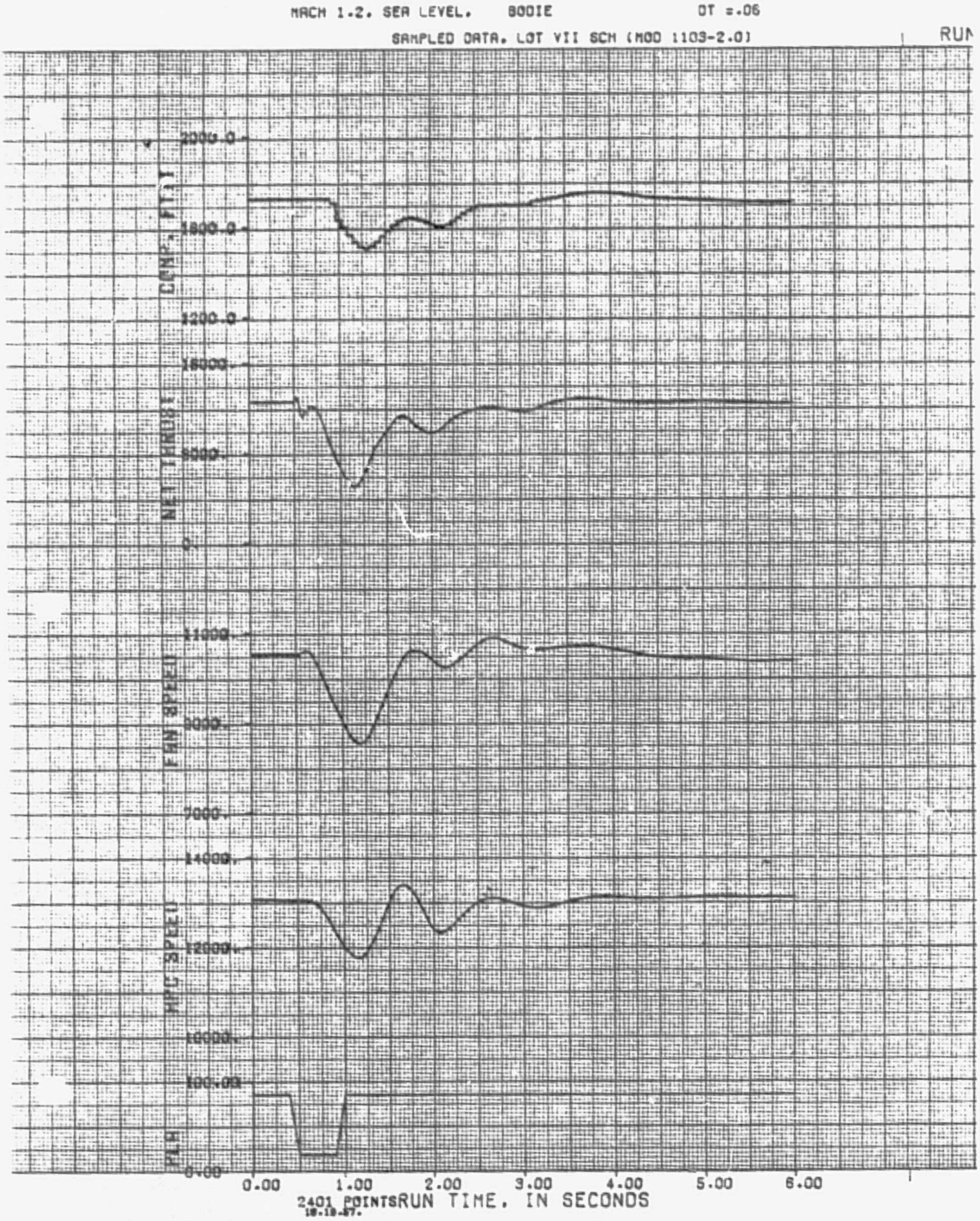
ORIGINAL PAGE IS
OF POOR QUALITY





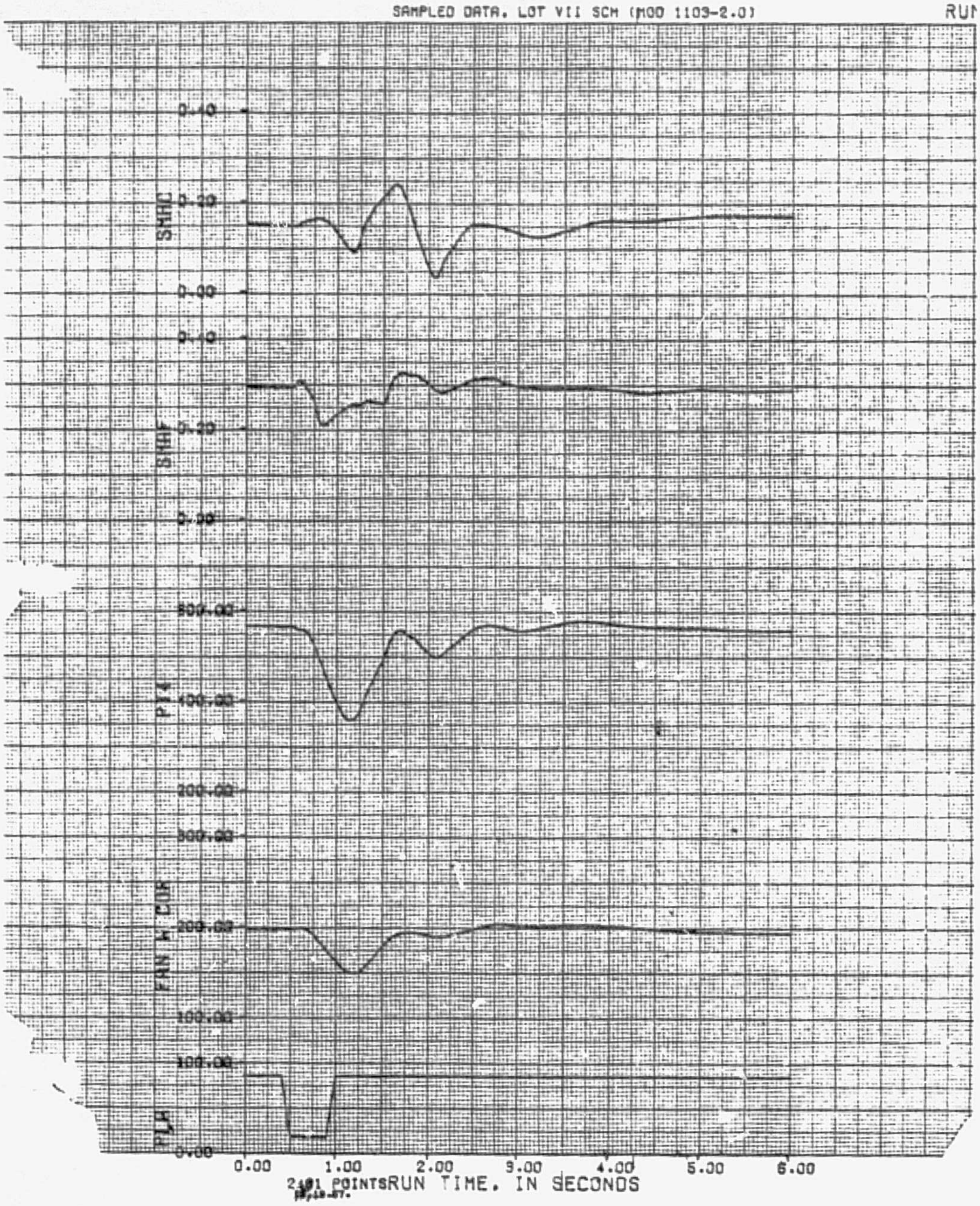
MACH 1.2. SEA LEVEL. BODIE
BOM OT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
RCVV
0.00
20.00
40.00
CIVV
10.00
30.00
AJ
5.60
4.60
2.60
FUEL FLOW
16000.
12000.
8000.
4000.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY

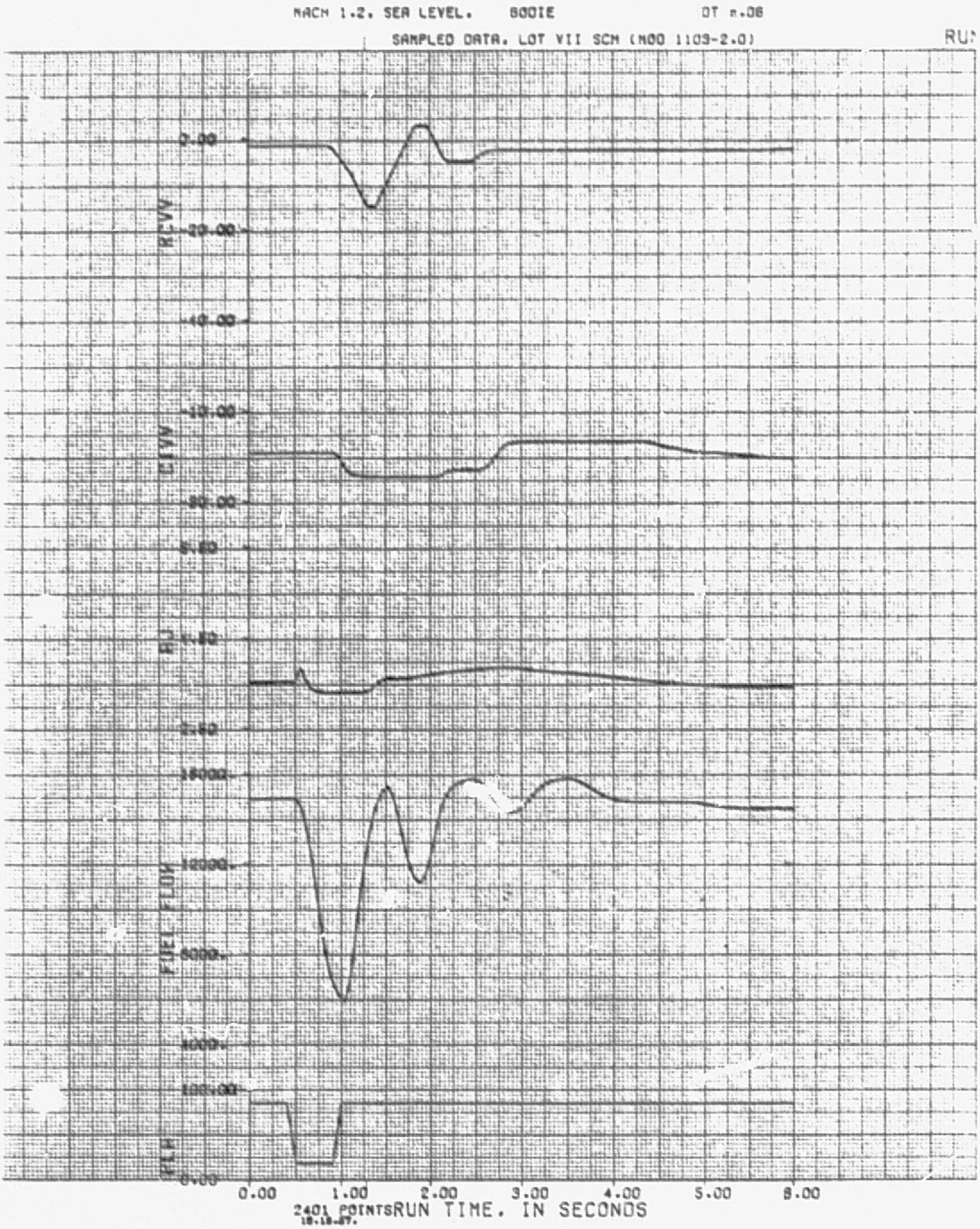


MACH 1.2, SEA LEVEL.   BODIE   DT =.06

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)   RUN



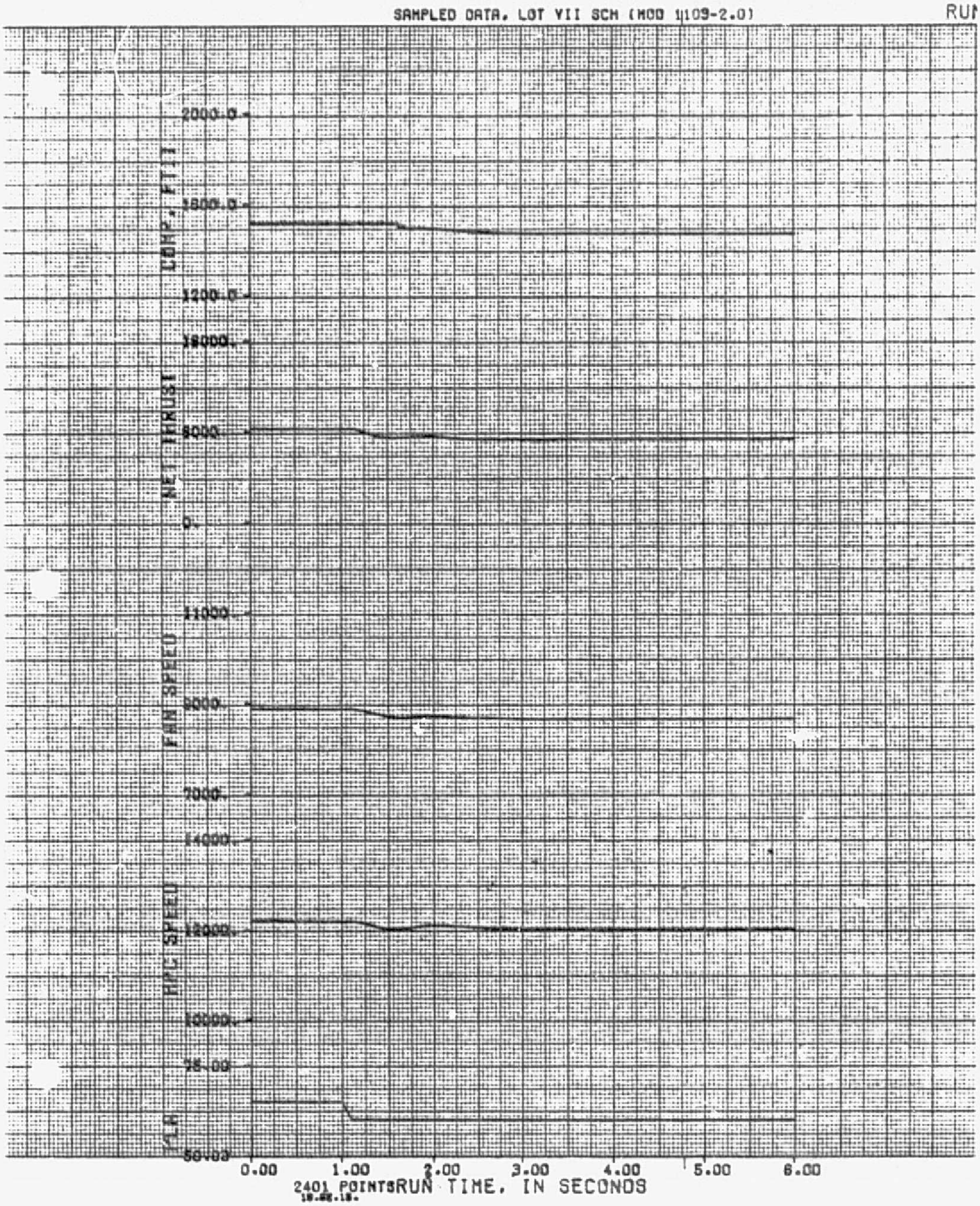
ORIGINAL PAGE IS
OF POOR QUALITY



MACH 1.2, SEA LEVEL. 65 - 60 DEG PLA. 80M DT

SAMPLED DATA, LOT VII SCH (MOD 1109-2.0)

RUN



ORIGINAL PAGE IS
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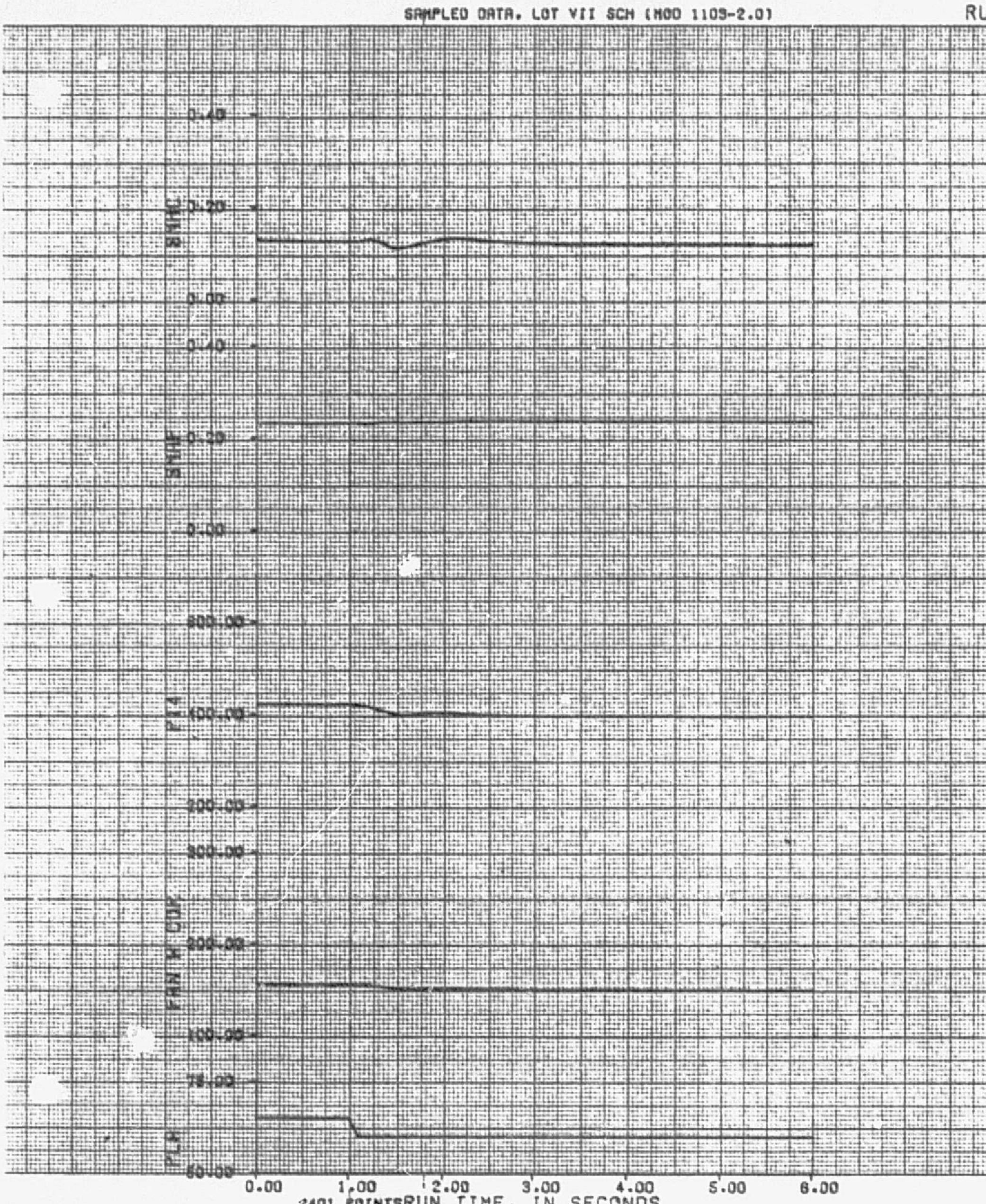
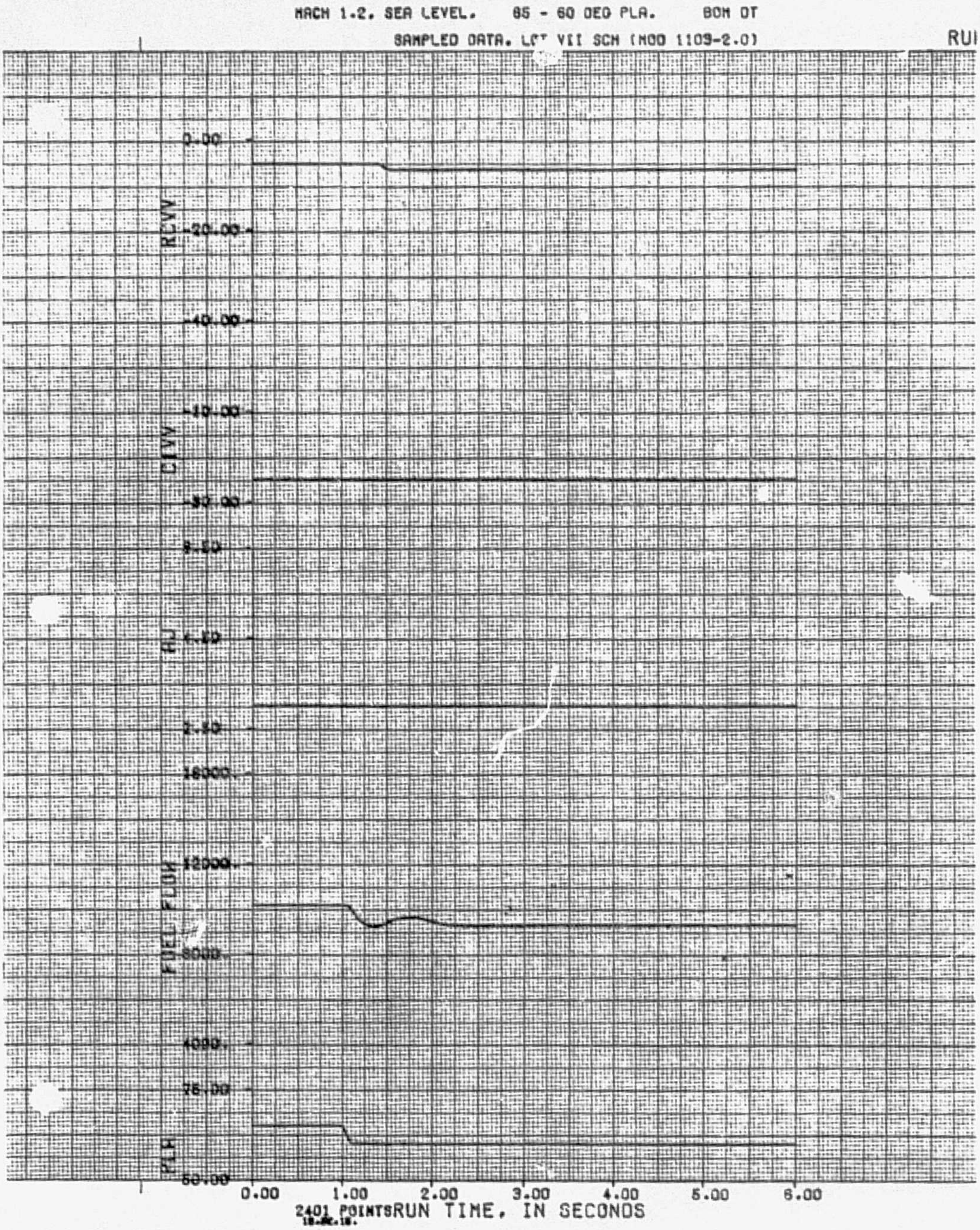
MACH 1.2, SEA LEVEL. 65 - 60 DEG PLA. 80M DT

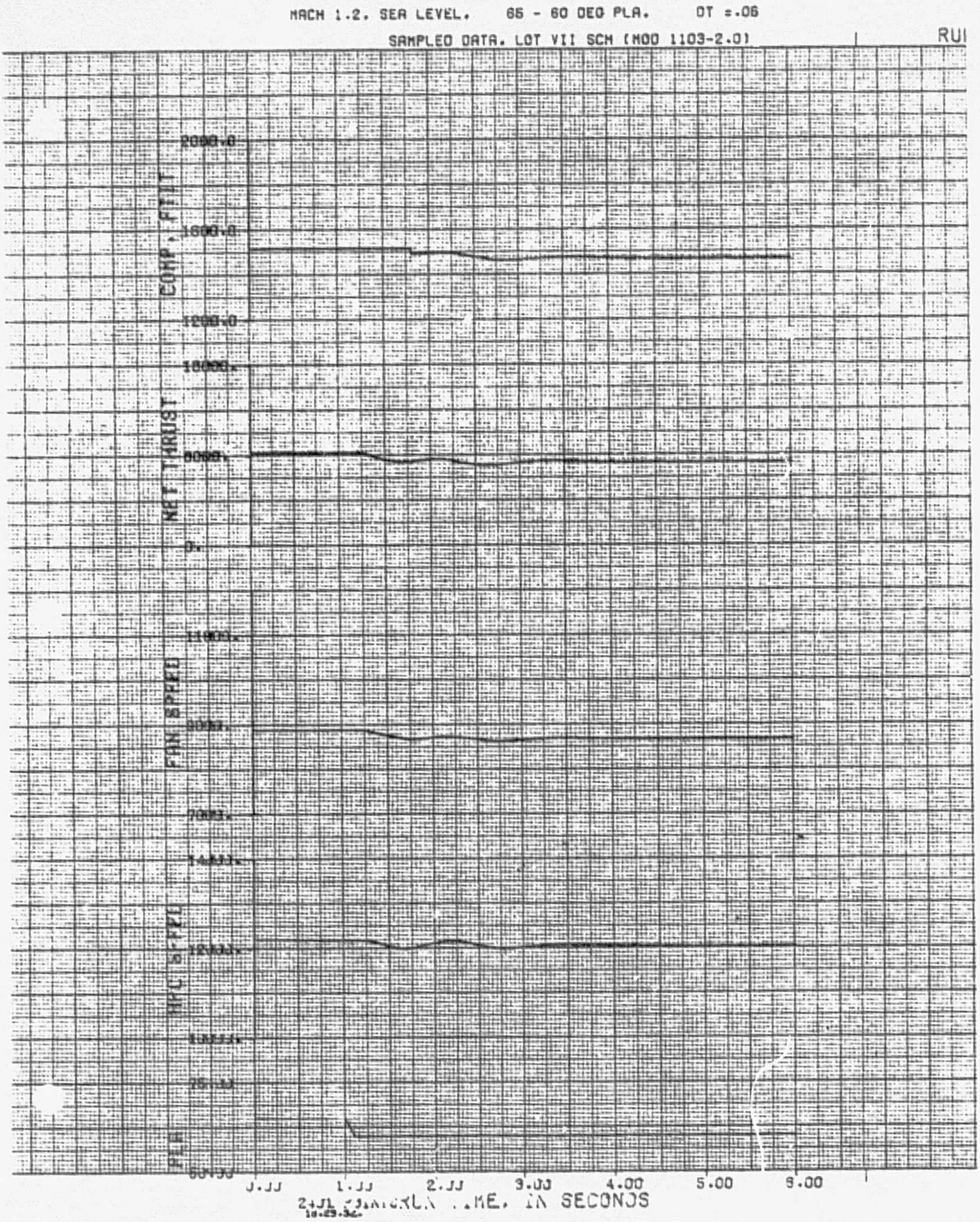
SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)

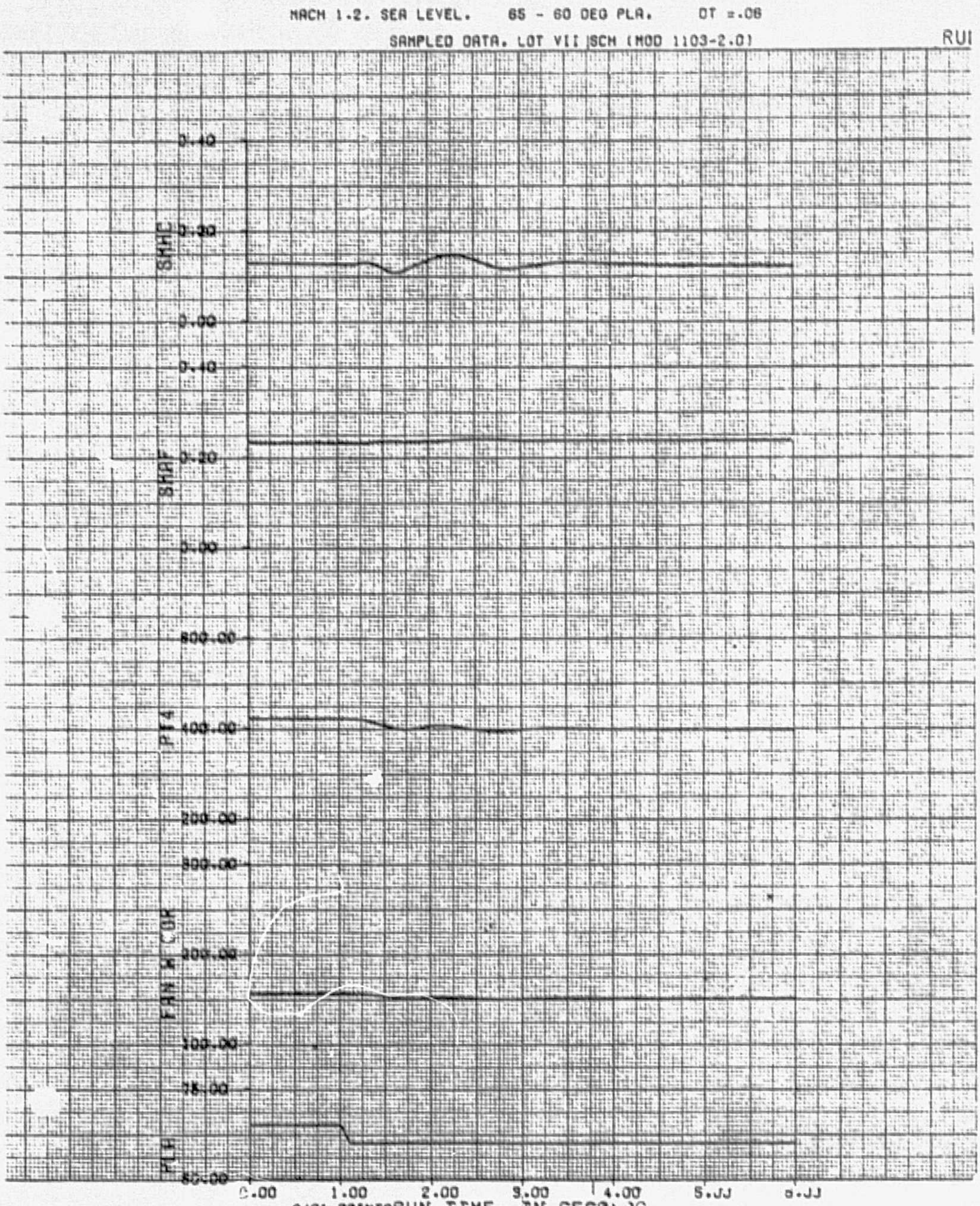
RUN



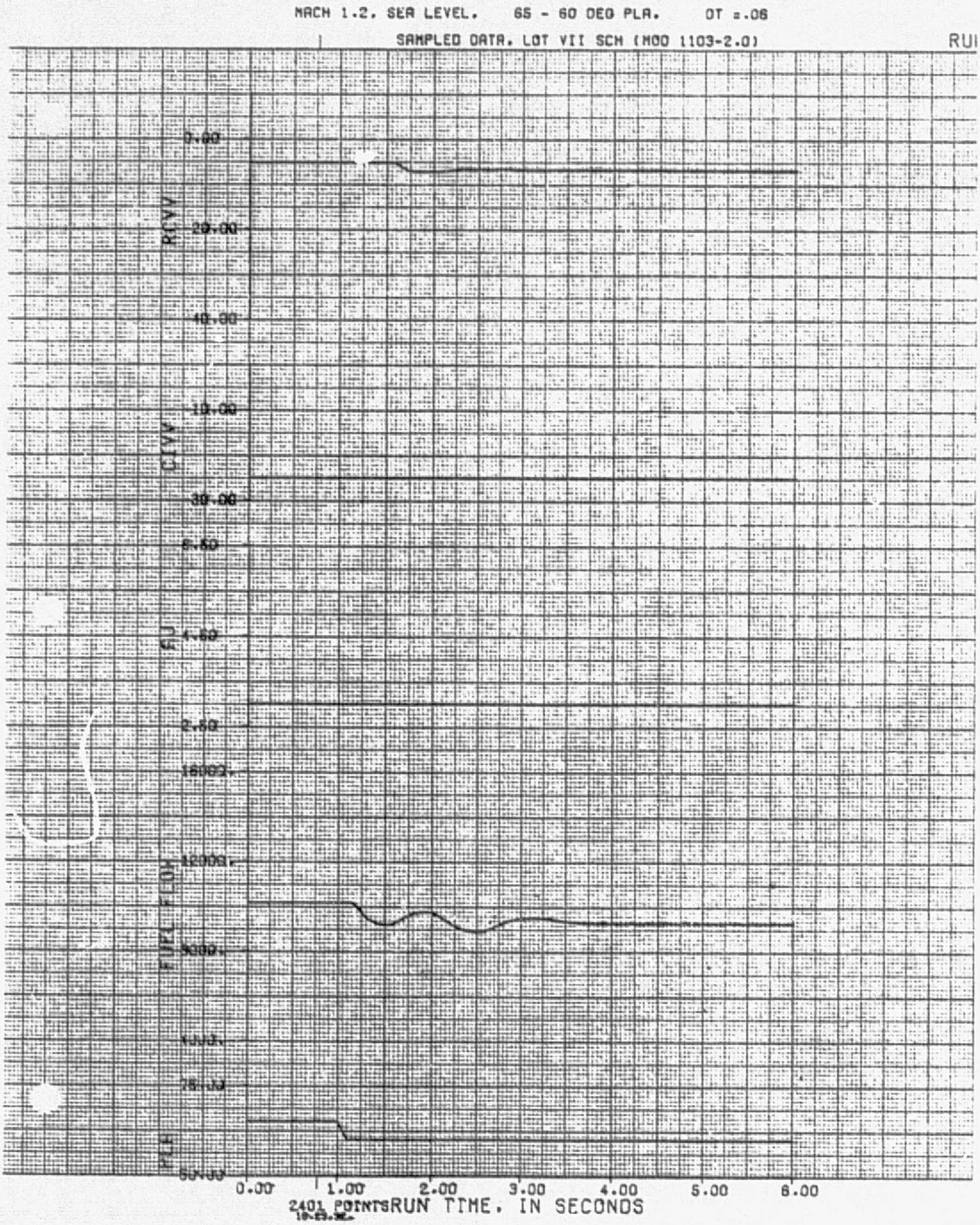

MACH 1.2, SEA LEVEL. 65 - 60 DEG PLA. 80M DT
SAMPLED DATA, LOT VII SCM (MOD 1109-2.0)
RU
0.00
-20.00
-40.00
-10.00
-30.00
8.50
4.50
2.50
16000.
12000.
8000.
4000.
76.00
56.00
RCVV
CIVV
AJ
FUEL FLOW
PLA
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



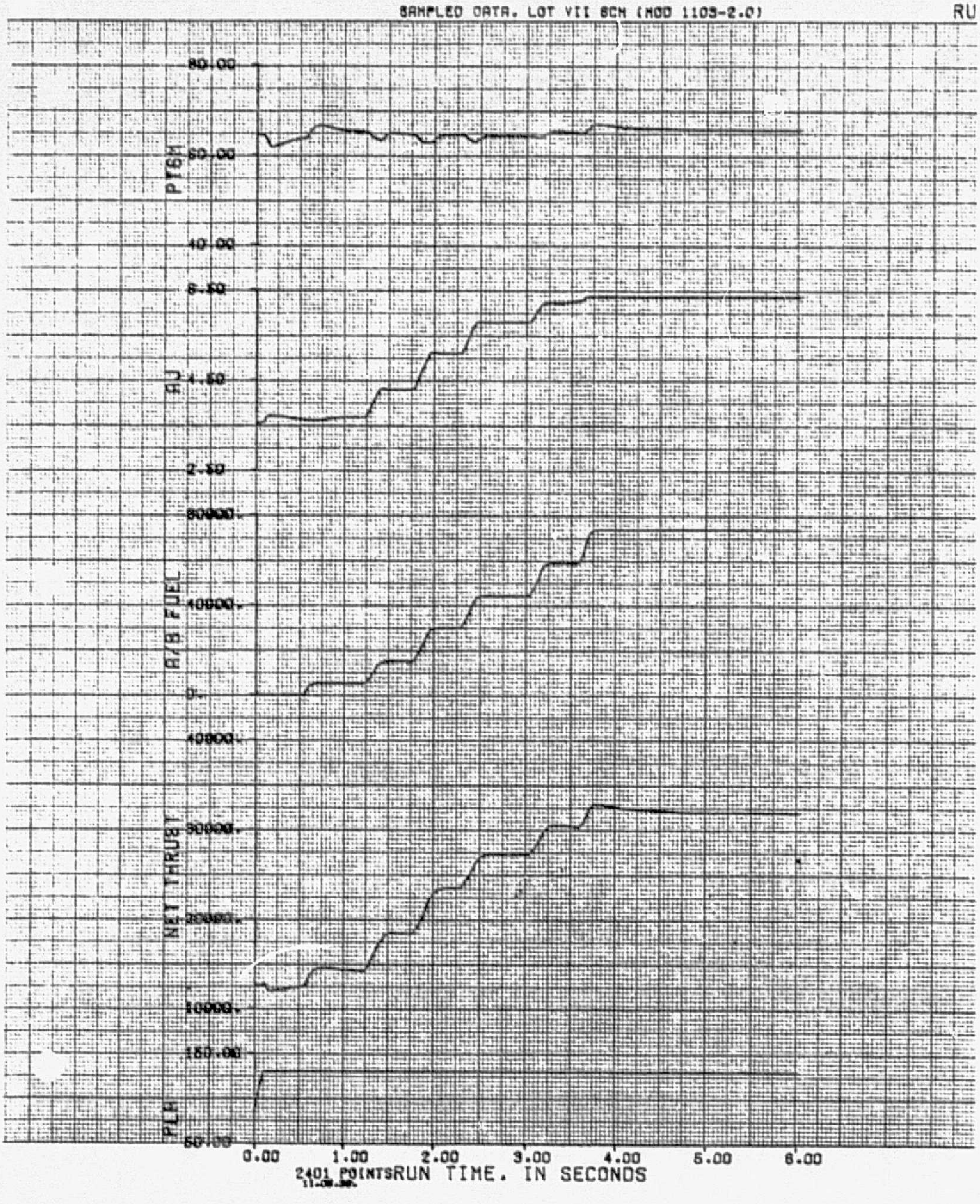

MACH 1.2. SEA LEVEL. 65 - 60 DEG PLA. DT =.06
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
SMAC
SMAF
PT4
FAN R COR
PLA
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



MACH 1.2, SEA LEVEL, INTERMEDIATE - MAX. 80M DT

SAMPLED DATA, LOT VII 8CM (MOD 1103-2.0)



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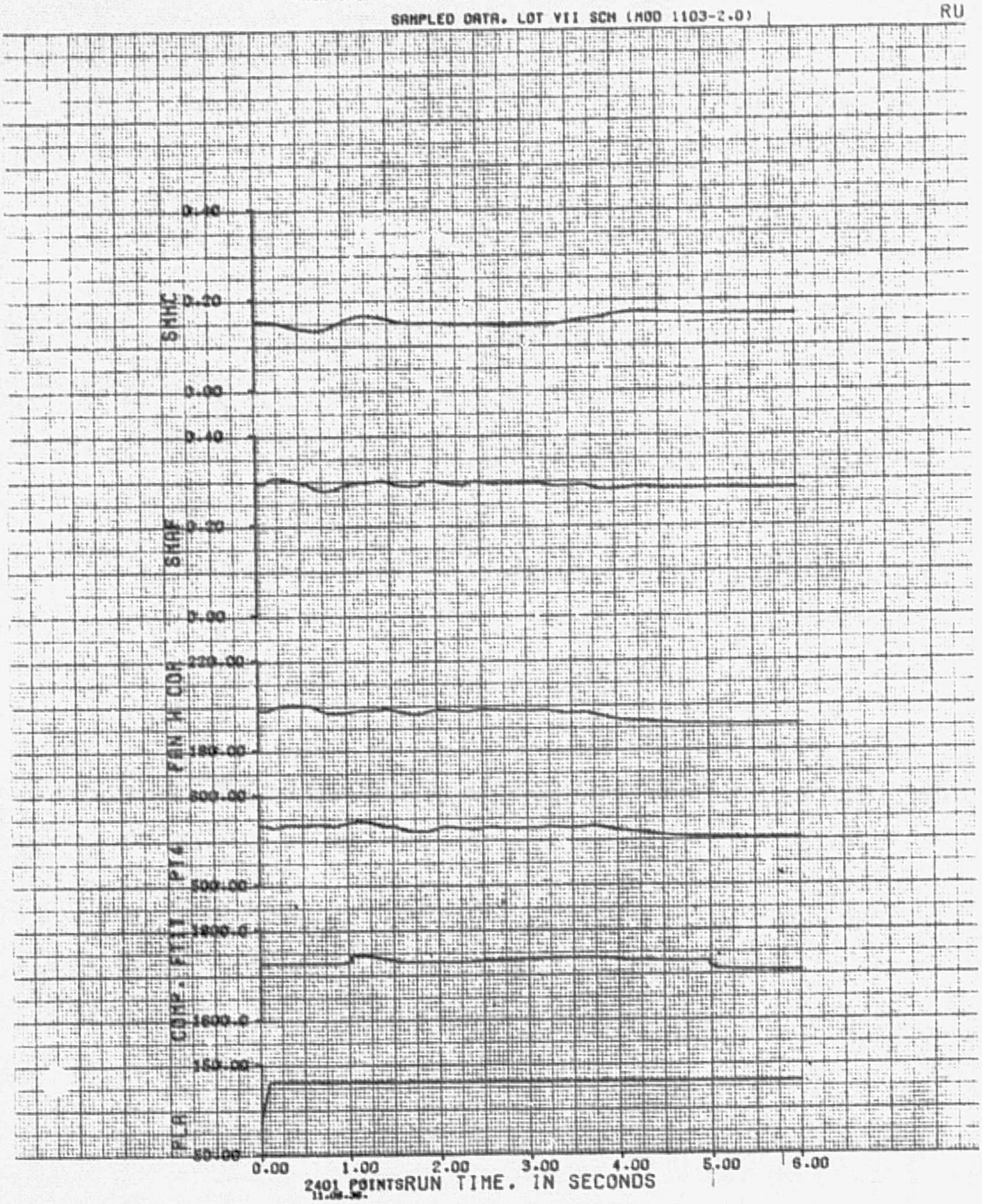
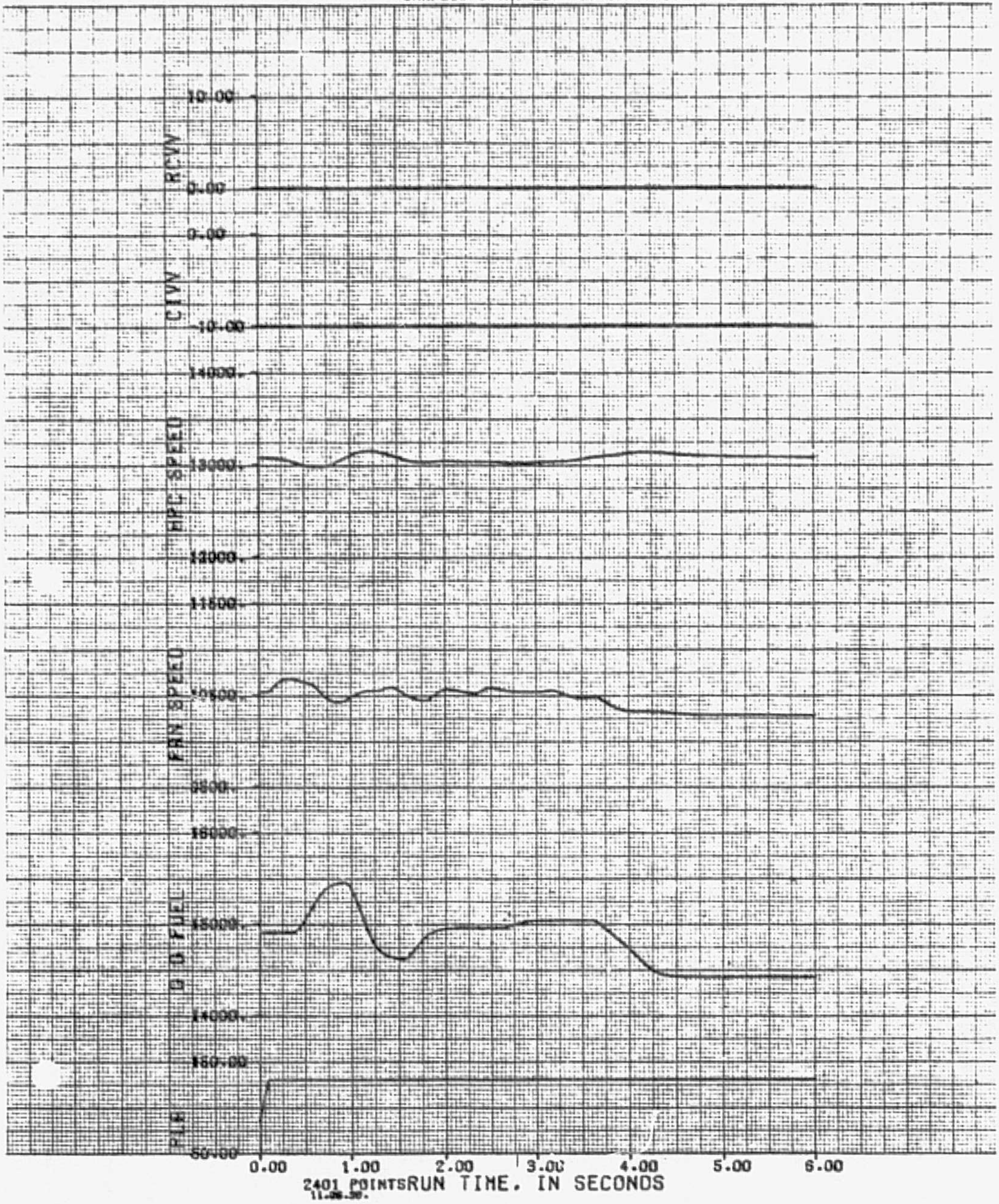
MACH 1.2, SEA LEVEL. INTERMEDIATE - MAX. 80N DT
SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)



MACH 1.2. SEA LEVEL. INTERMEDIATE - MAX. 80M DT

SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)

RU



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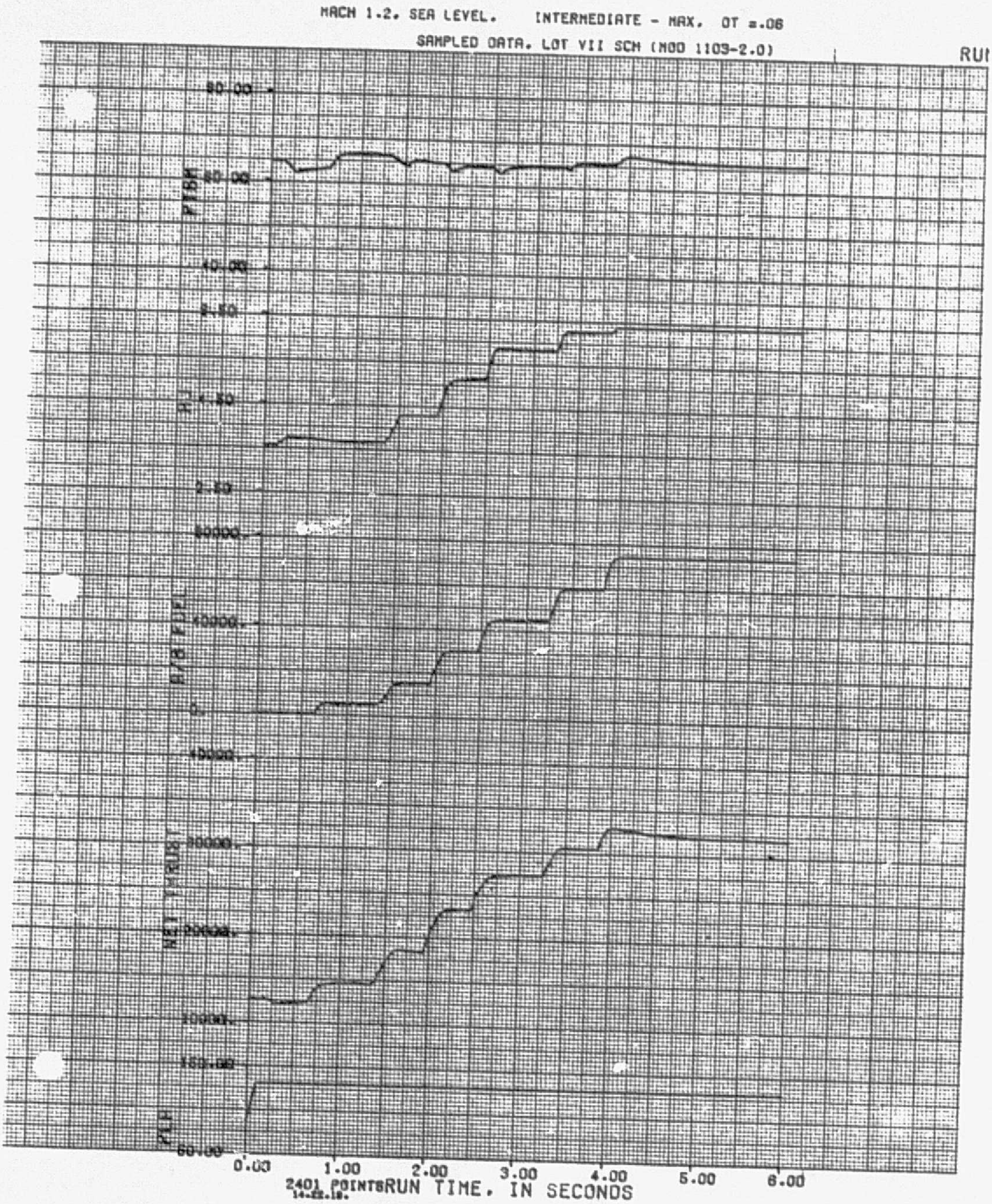
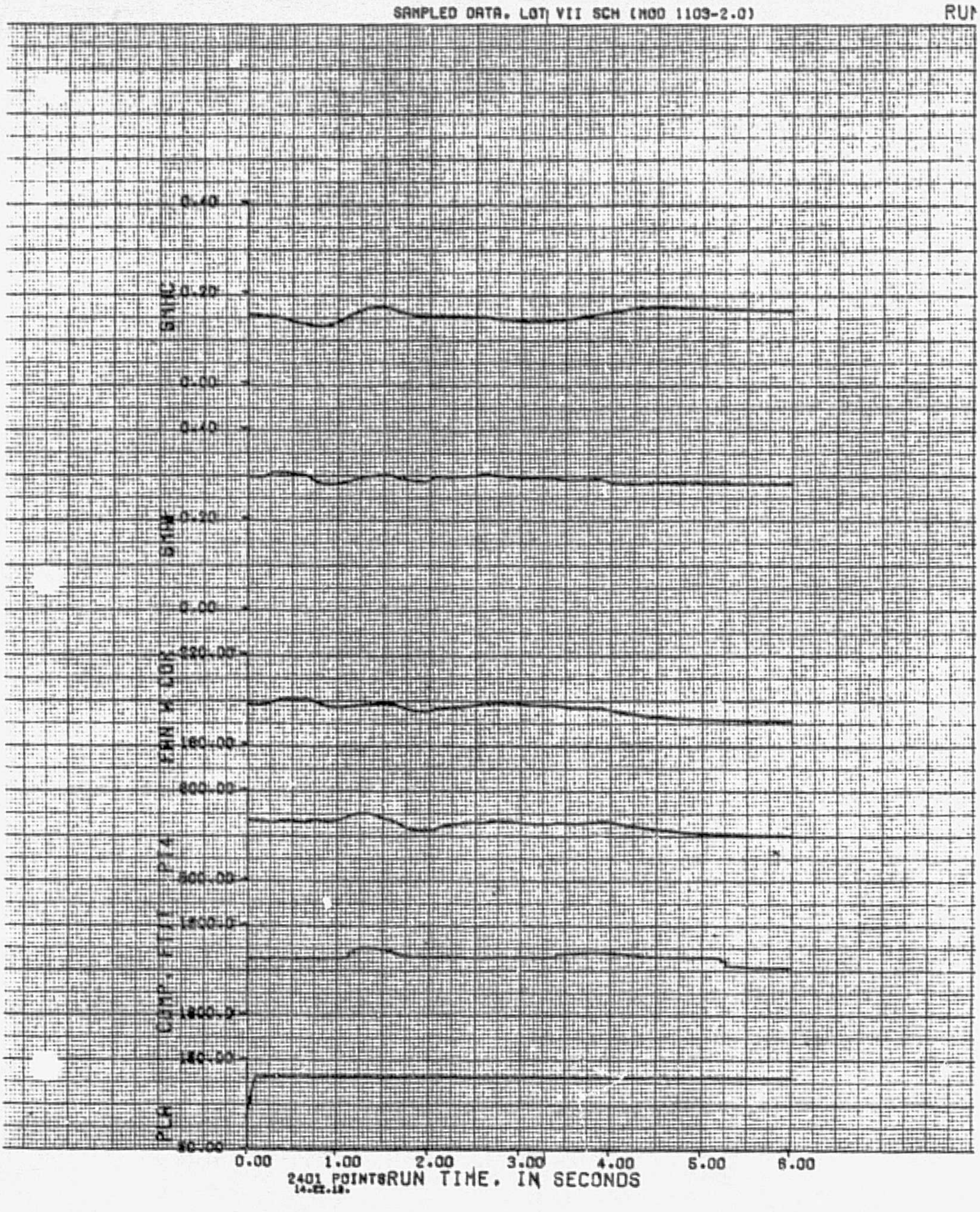


MACH 1.2, SEA LEVEL. INTERMEDIATE - MAX, DT =.06
SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)



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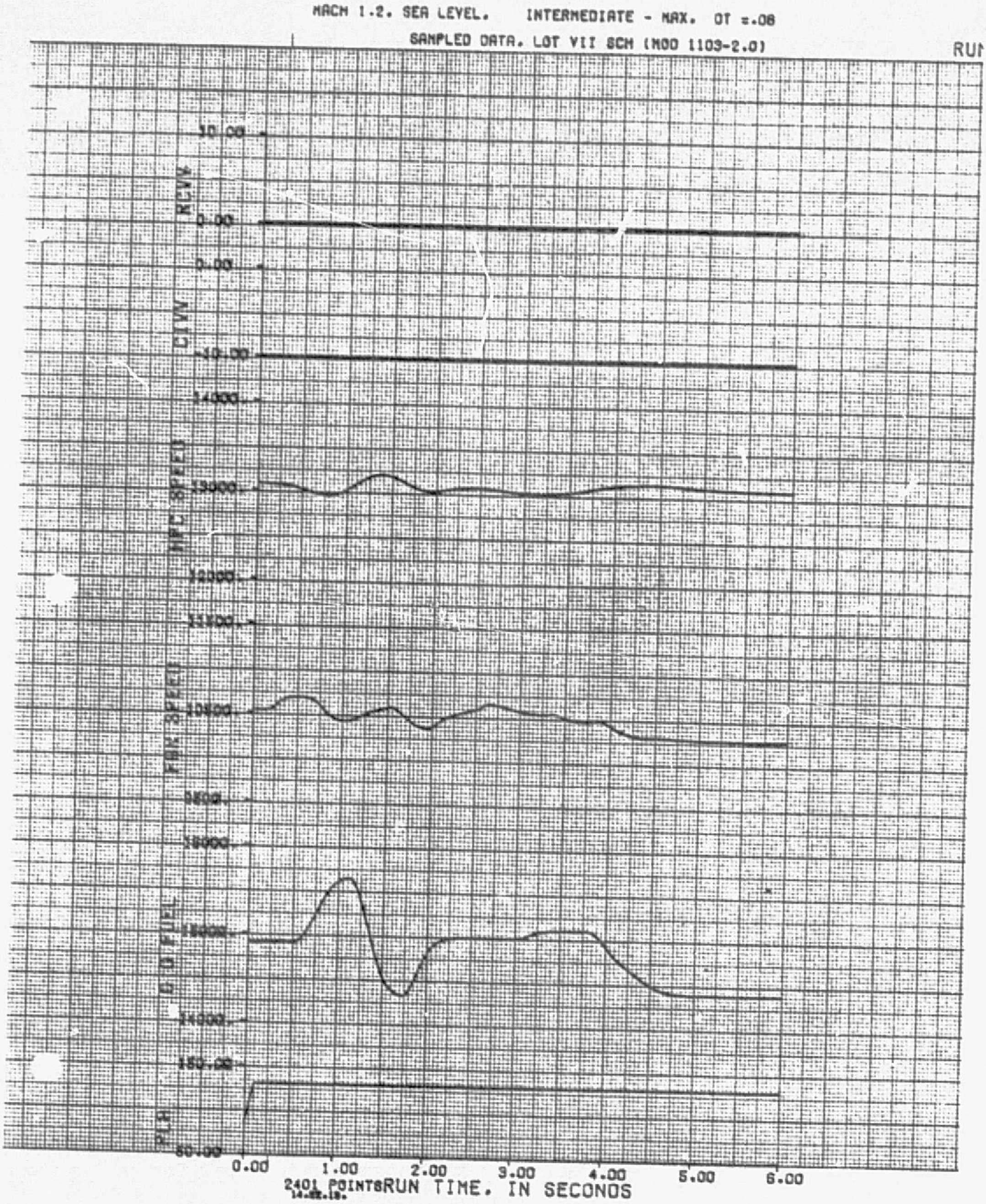
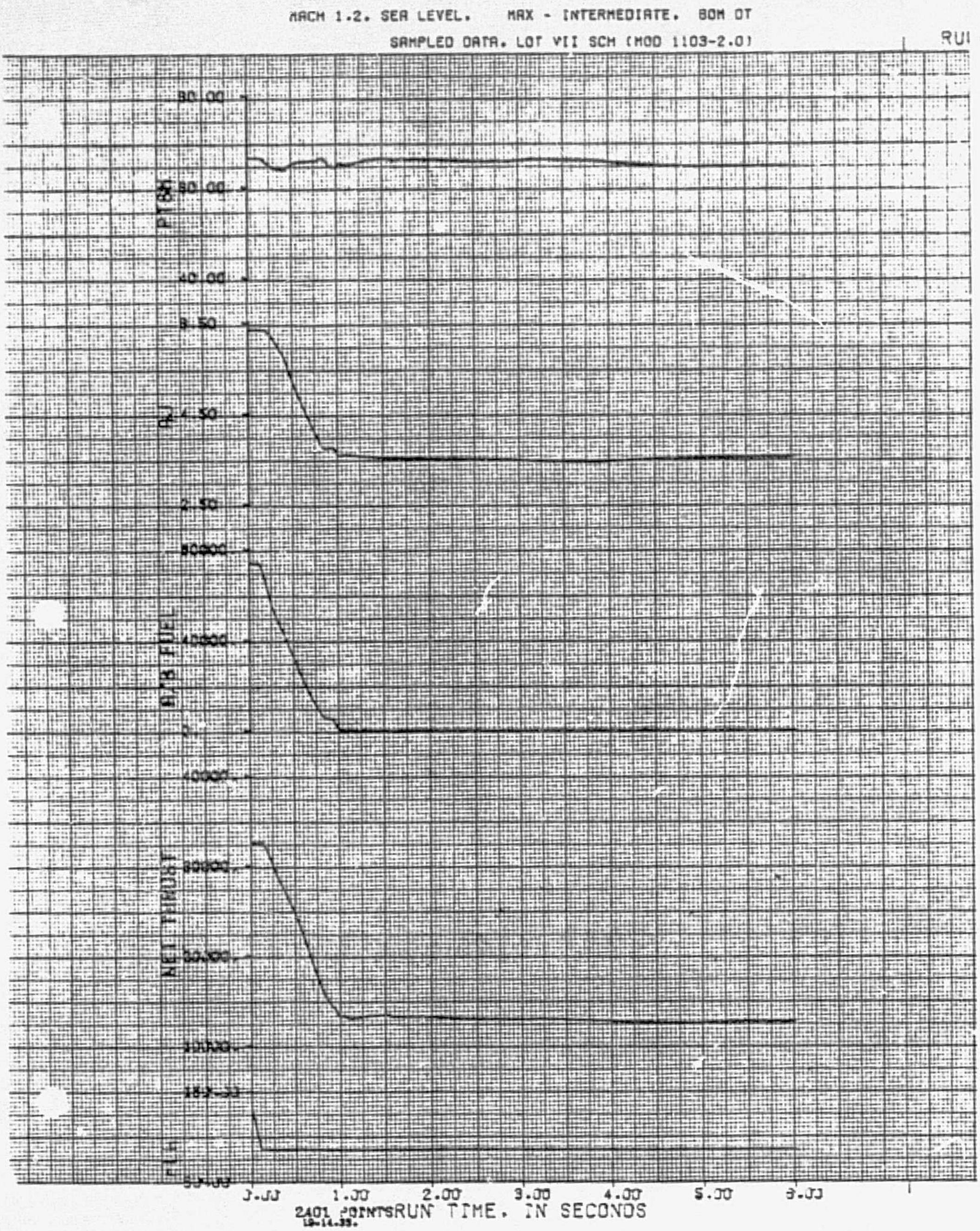
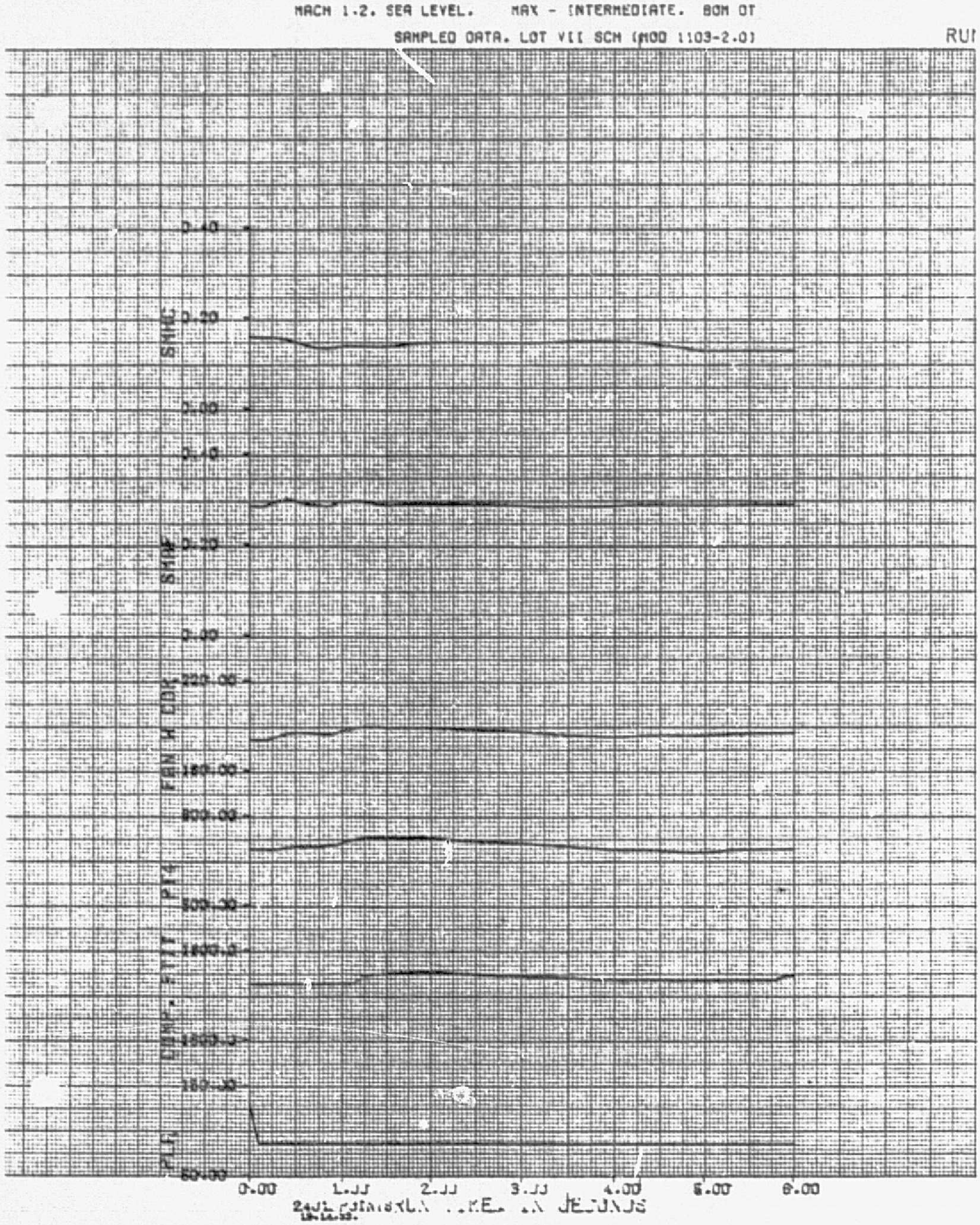
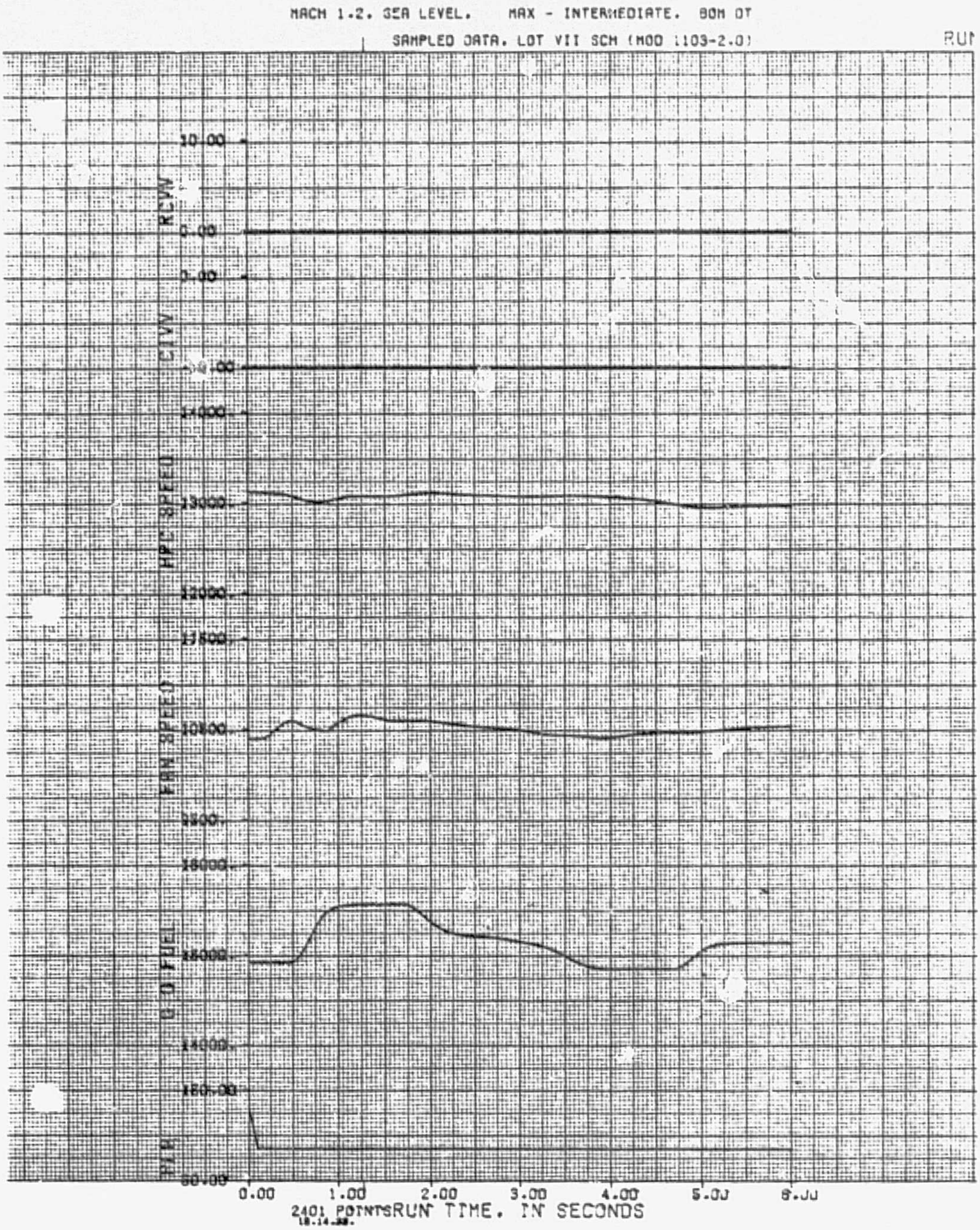


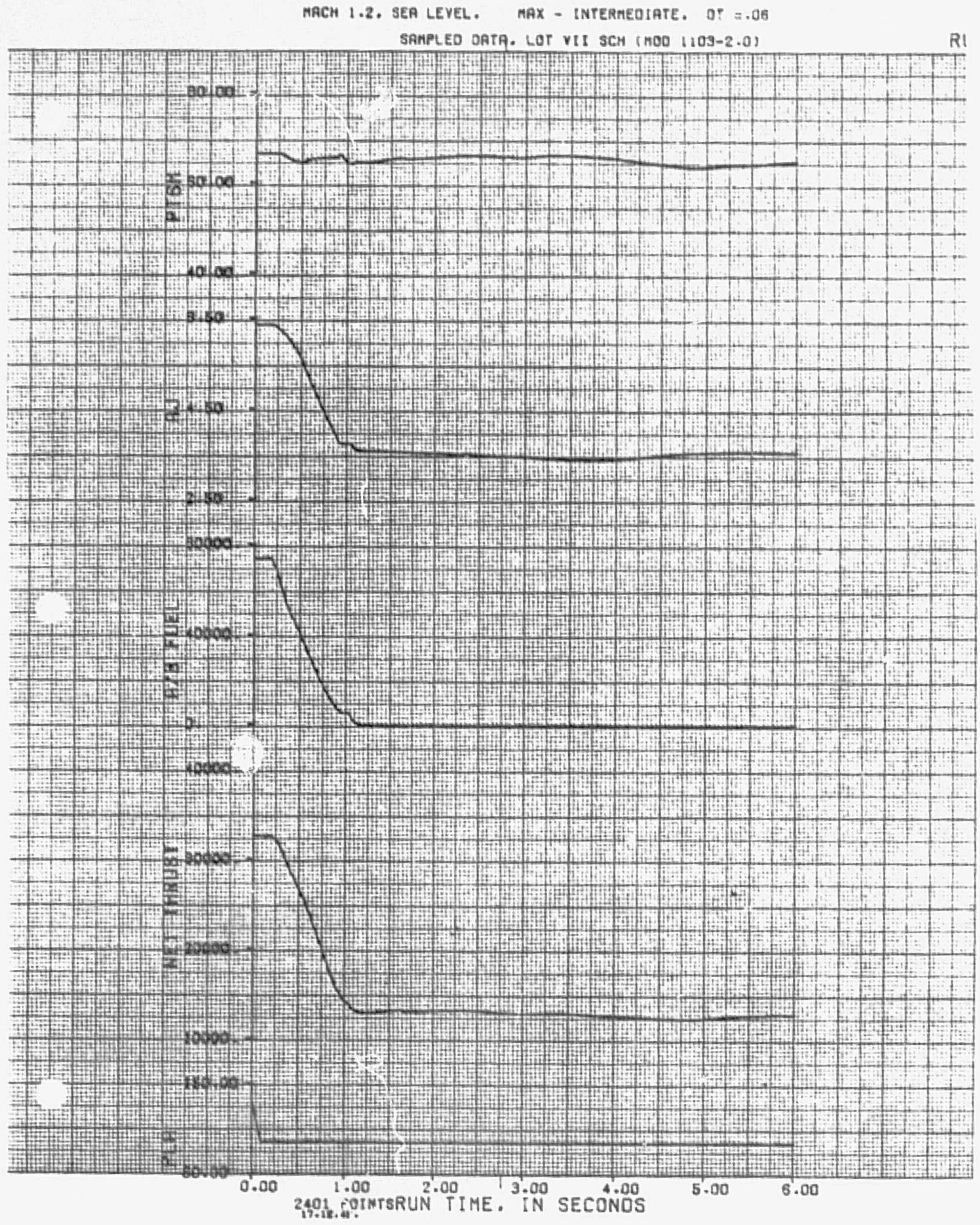

MACH 1.2, SEA LEVEL. MAX - INTERMEDIATE. 80M OT
SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)
RUN TIME, IN SECONDS
2401 POINTS

ORIGINAL PAGE IS OF POOR QUALITY

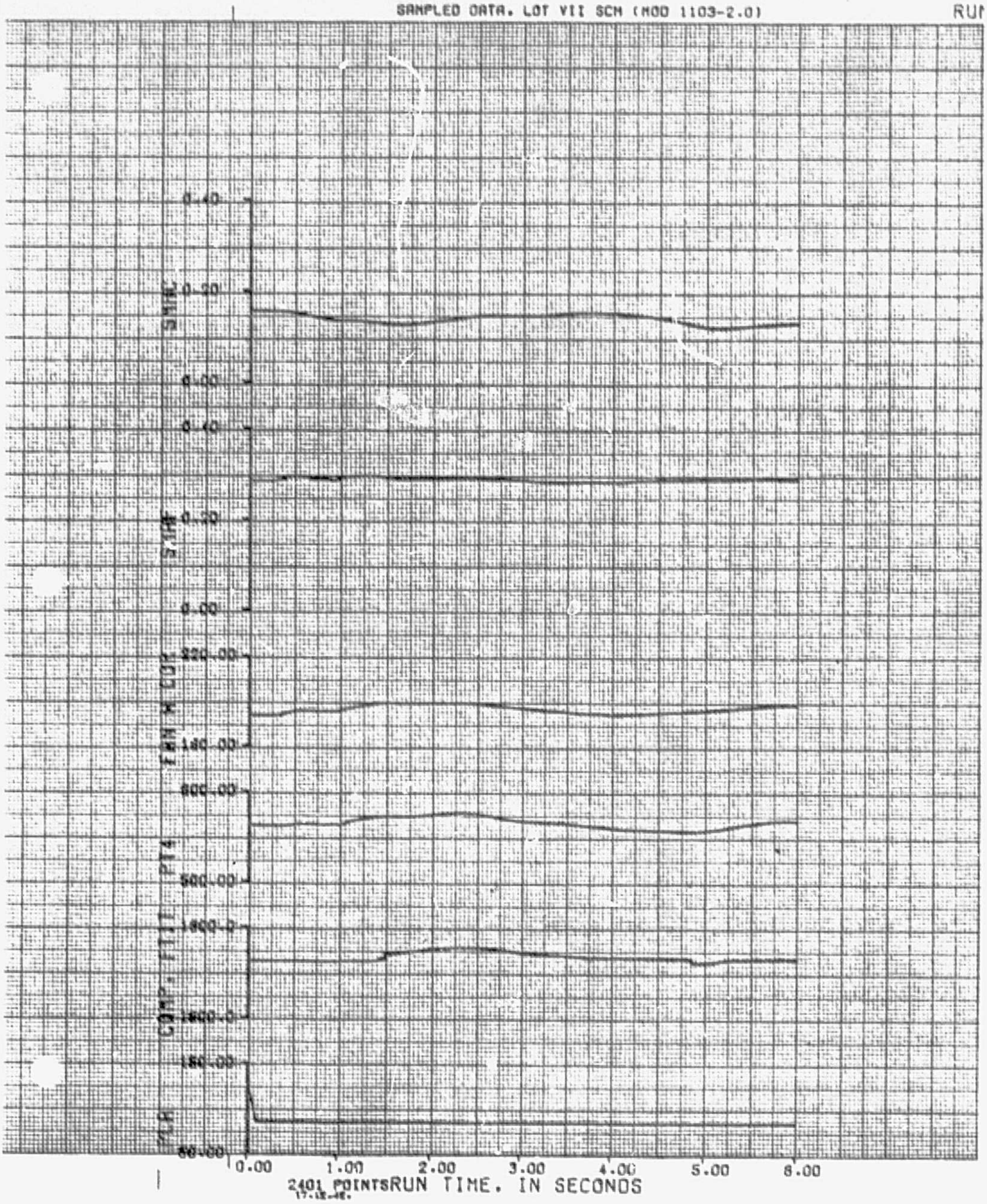



MACH 1.2. SEA LEVEL.   MAX - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
10.00
RCVV
CIVV
HPC SPEED
13000.
12000.
FAN SPEED
10800.
FUEL
0.00
1.00
2.00
3.00
4.00
2401 POINTS
RUN TIME. IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



MACH 1.2. SEA LEVEL.   MAX - INTERMEDIATE. DT =.06



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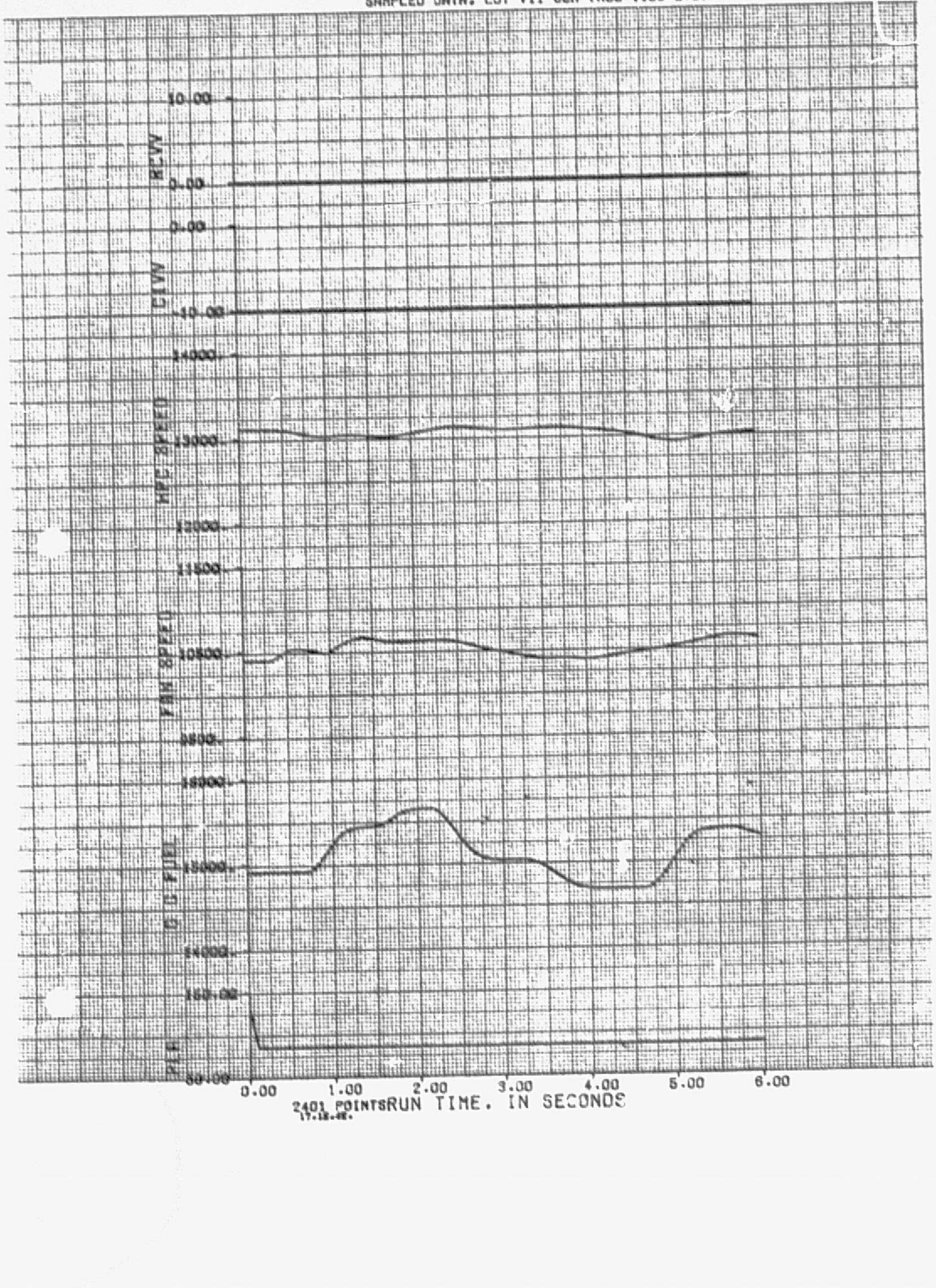
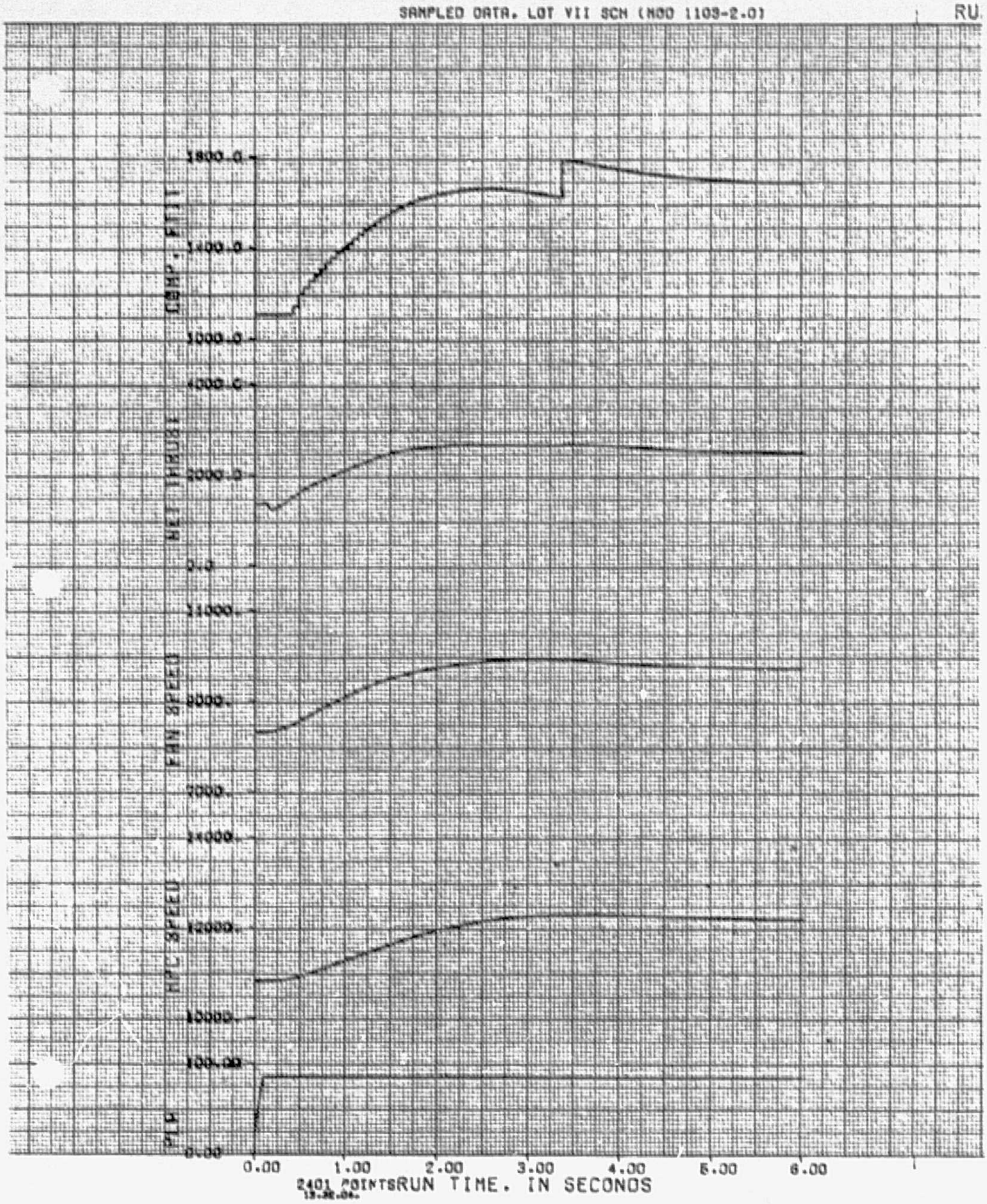
MACH 1.2. SEA LEVEL. MAX - INTERMEDIATE. DT =.08

SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)

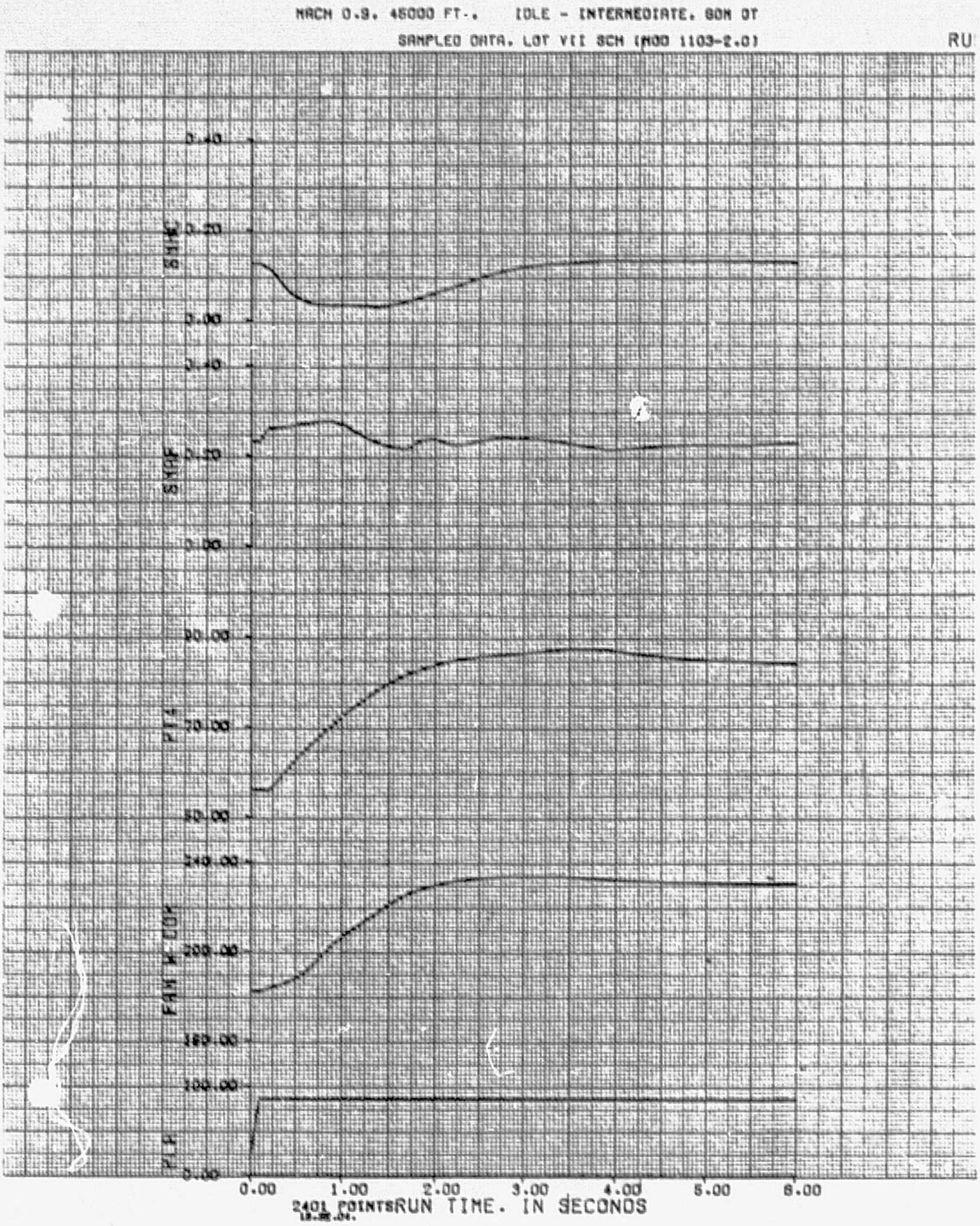


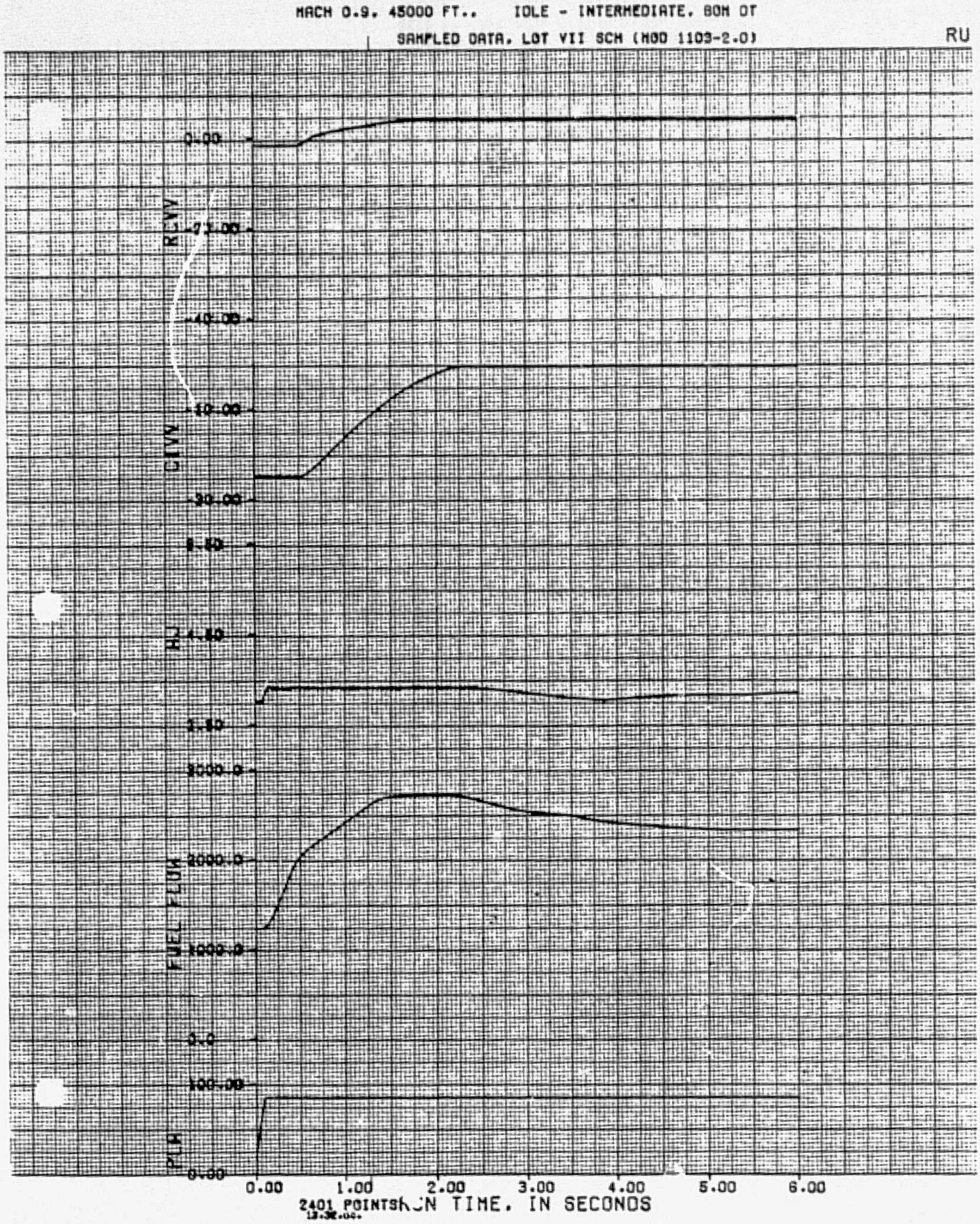
MACH 0.9, 45000 FT., IDLE - INTERMEDIATE, 80M DT

SAMPLED DATA, LOT VII SCM (MOD 1103-2.0) RU



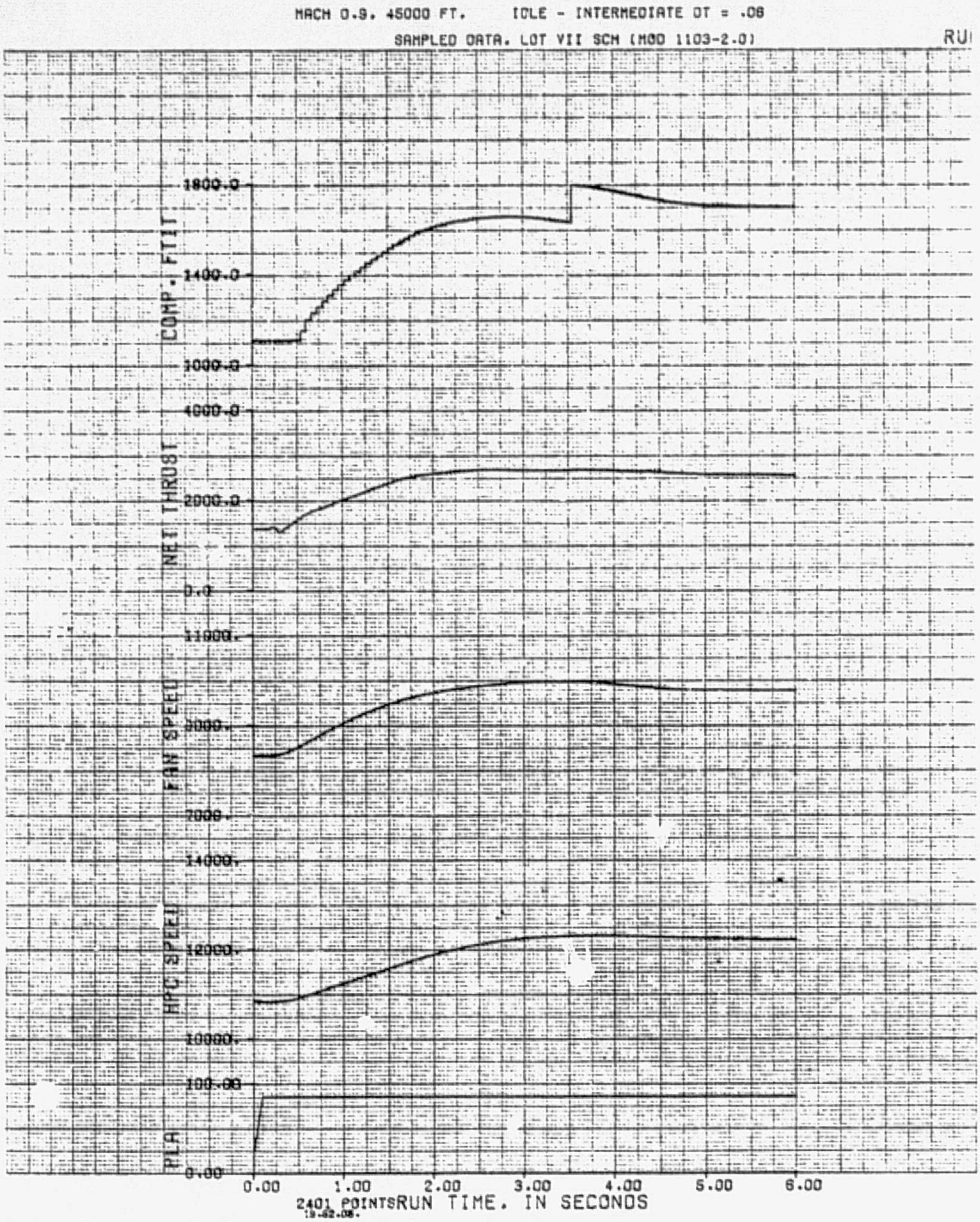
ORIGINAL PAGE IS
OF POOR QUALITY

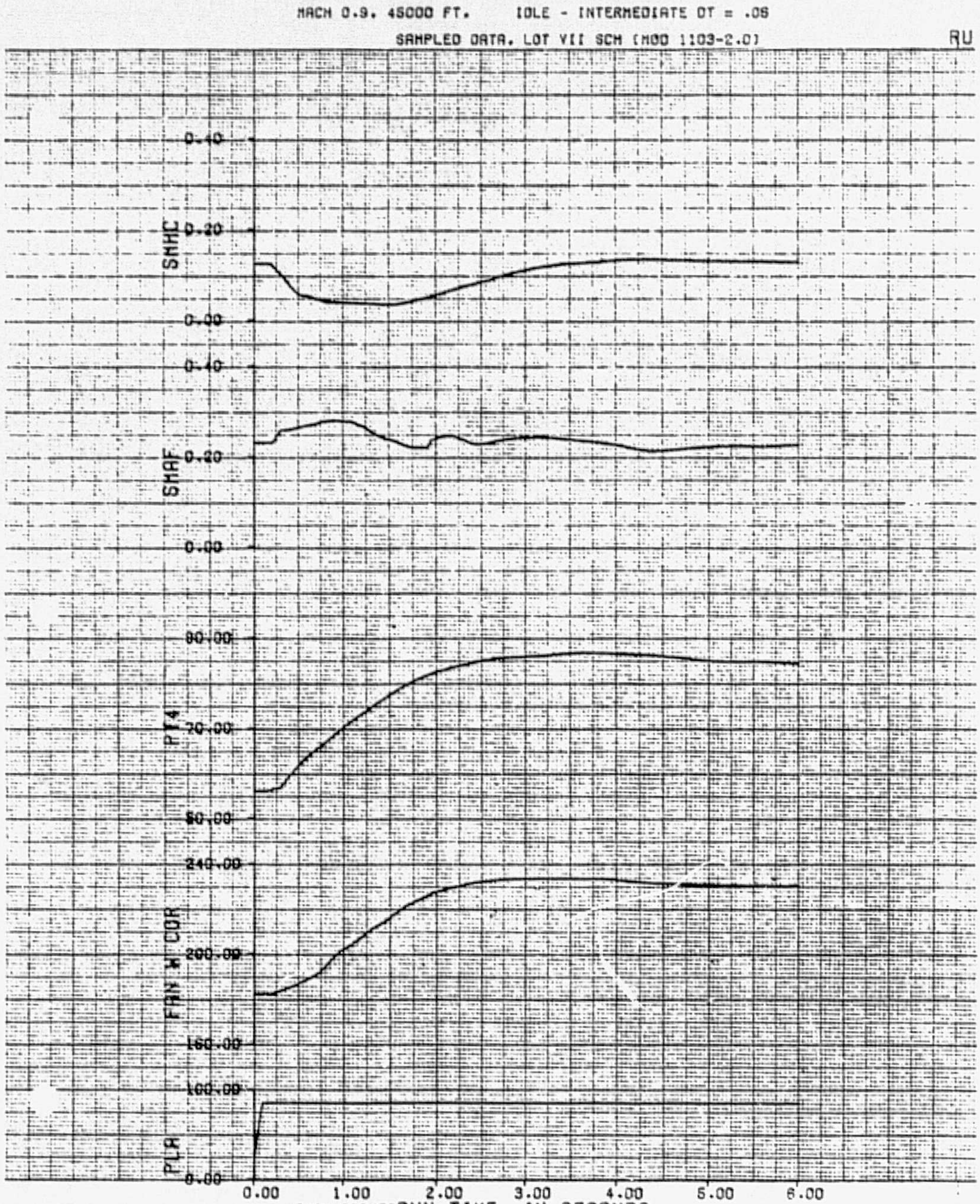




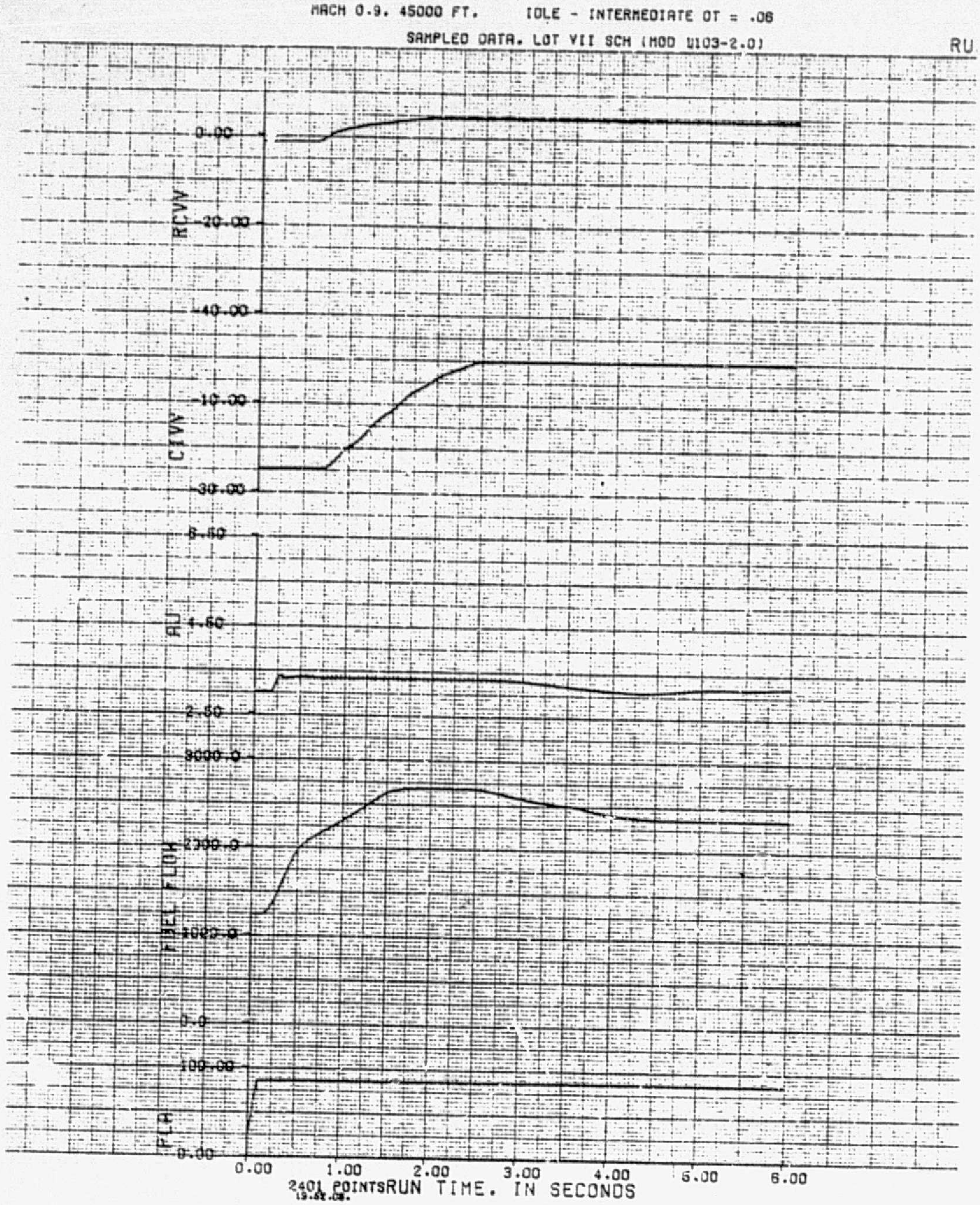
MACH 0.9. 45000 FT.. IDLE - INTERMEDIATE. 80M DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RU
REVV
CIVV
RU
FUEL FLOW
PLA
0.00
-20.00
-40.00
-10.00
-30.00
8.40
4.40
1.60
3000.0
2000.0
1000.0
0.0
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
TIME. IN SECONDS

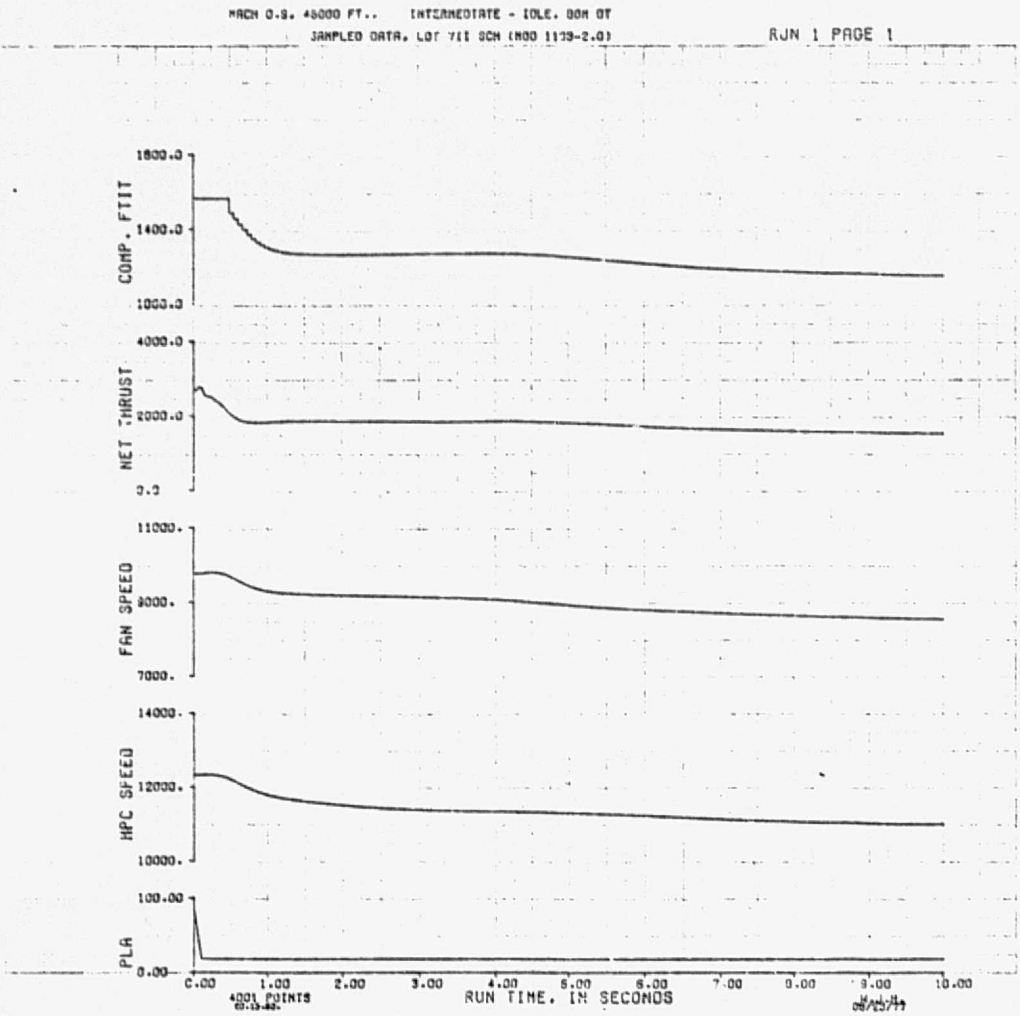
ORIGINAL PAGE
OF POOR QUAL




MACH 0.9, 45000 FT. IDLE - INTERMEDIATE DT = .05
SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)
RU
SMHC
SMAF
PT4
FAN W COR
PLA
0.40
0.20
0.00
0.40
0.20
0.00
80.00
70.00
60.00
240.00
200.00
160.00
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



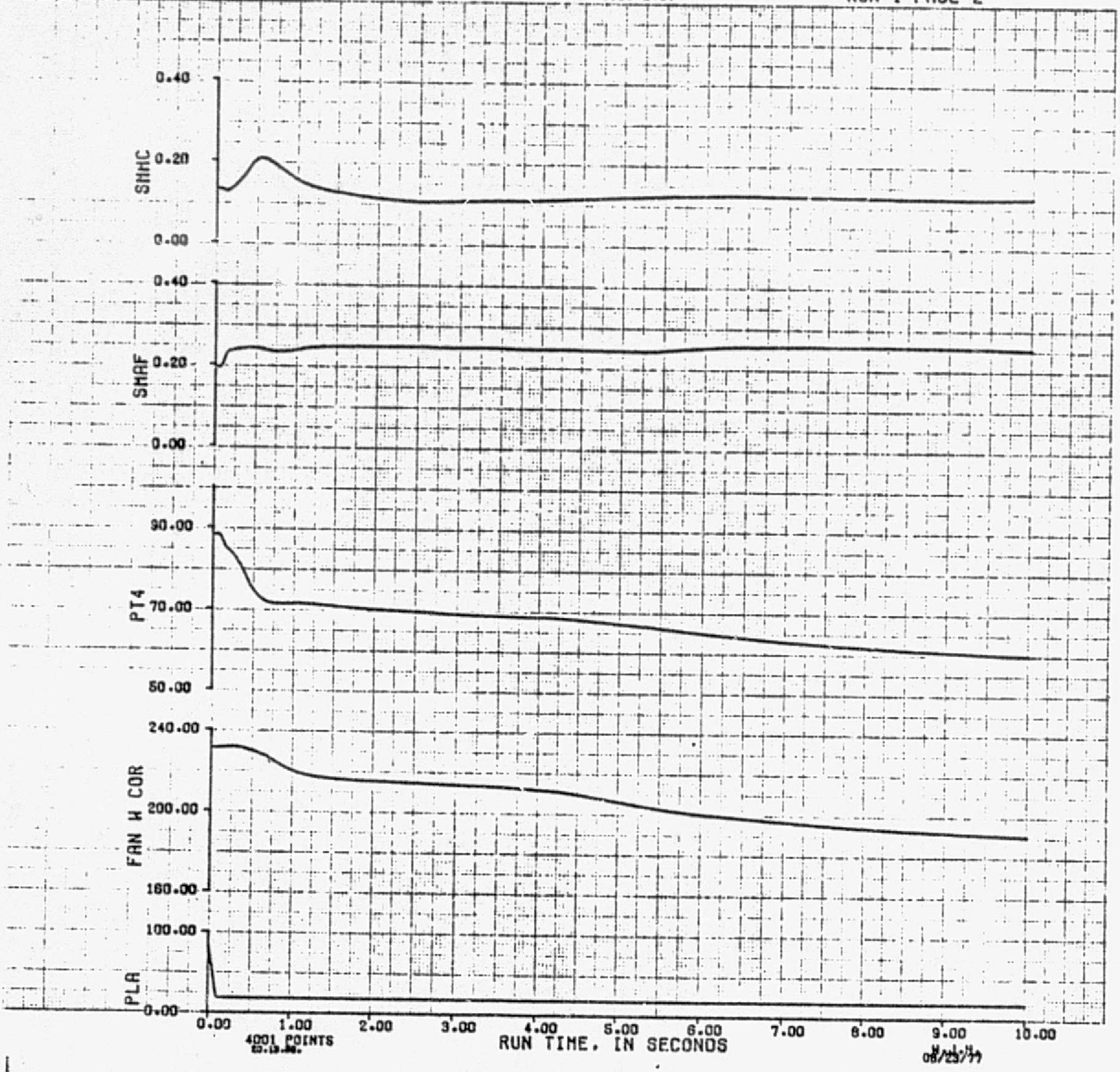

MACH 0.9, 45000 FT.. INTERMEDIATE - IDLE. 80M OT
SAMPLED DATA, LOT VII SCH (MOD 1133-2.0)
RUN 1 PAGE 1
COMP. FTIT
1800.0
1400.0
1000.0
NET THRUST
4000.0
2000.0
0.0
FAN SPEED
11000.
9000.
7000.
HPC SPEED
14000.
12000.
10000.
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
4001 POINTS
RUN TIME, IN SECONDS

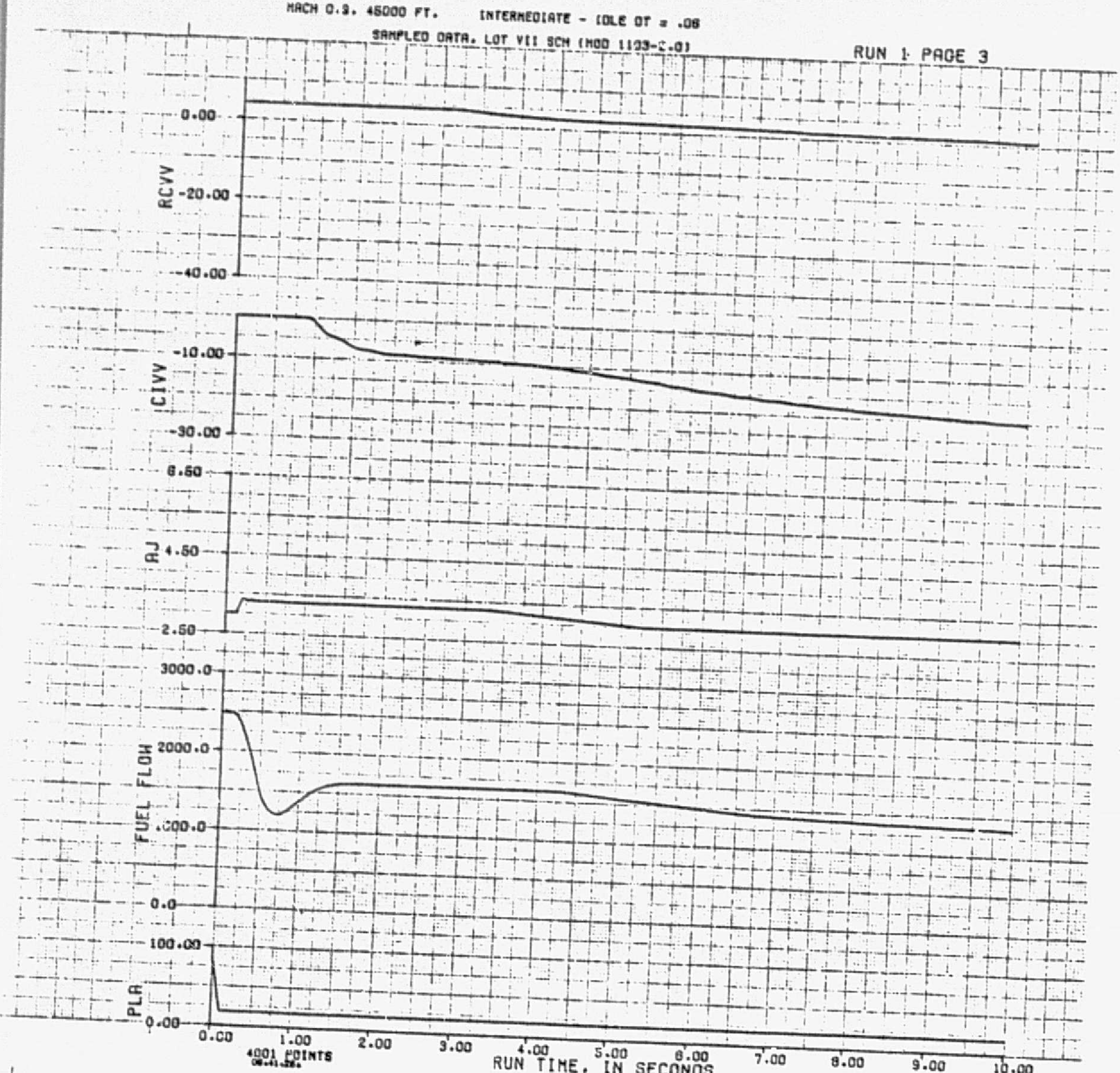
ORIGINAL PAGE IS
OF POOR QUALITY

MACH 0.9, 45000 FT., INTERMEDIATE - IDLE, 80% OT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)

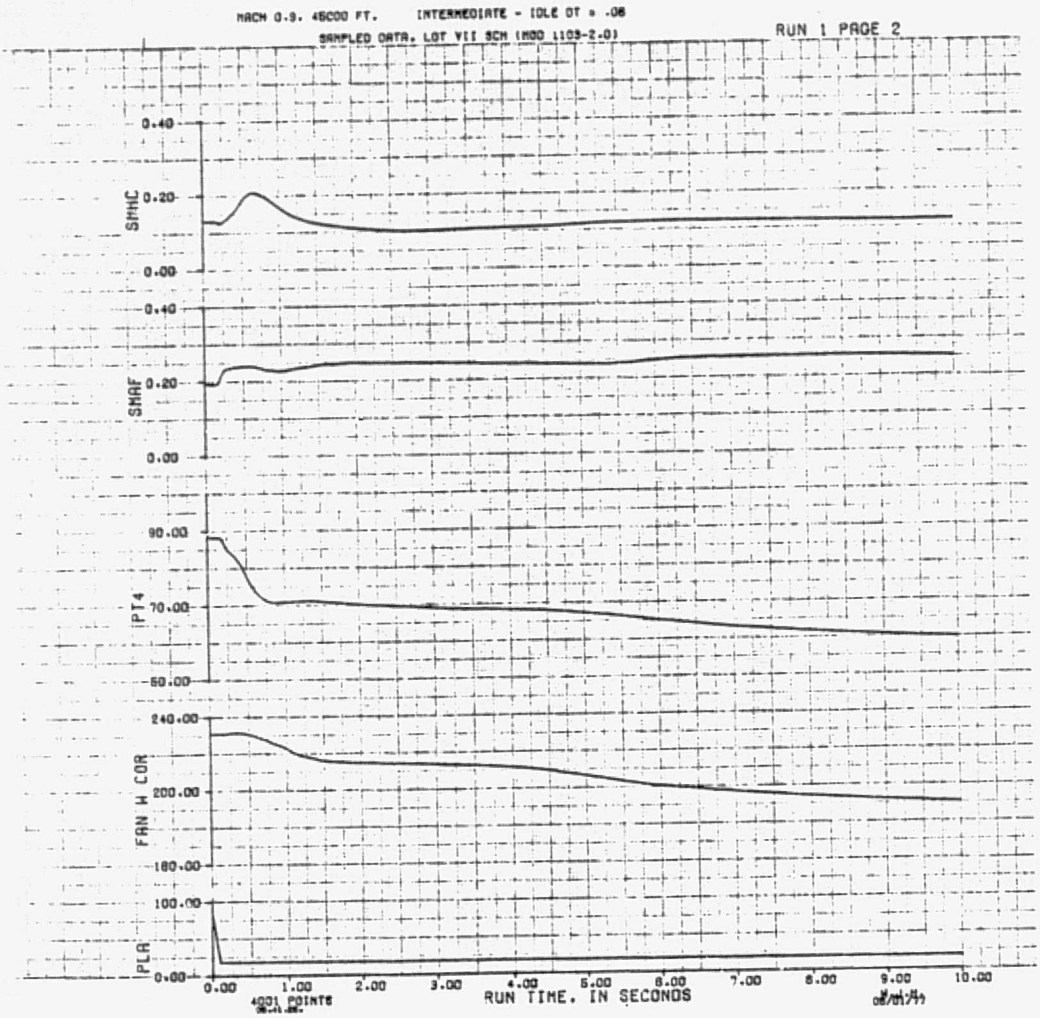
RUN 1 PAGE 2

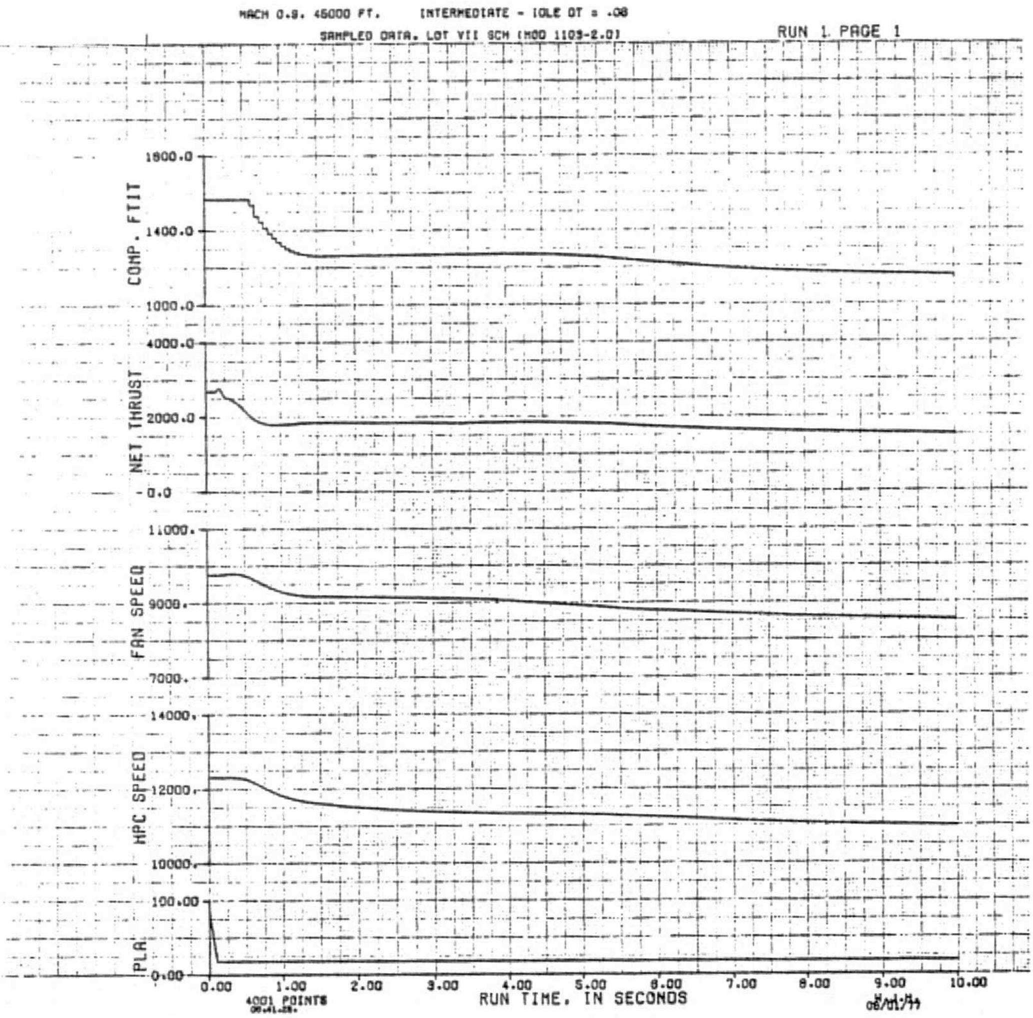




MACH 0.9, 45000 FT. INTERMEDIATE - IDLE DT = .08
SAMPLED DATA, LOT VII SCM (MOD 1193-2.0)
RUN 1 PAGE 3
RCVV
0.00
-20.00
-40.00
ICIVV
-10.00
-30.00
AJ
6.50
4.50
2.50
FUEL FLOW
3000.0
2000.0
1000.0
0.0
PLA
100.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
4001 POINTS
RUN TIME, IN SECONDS

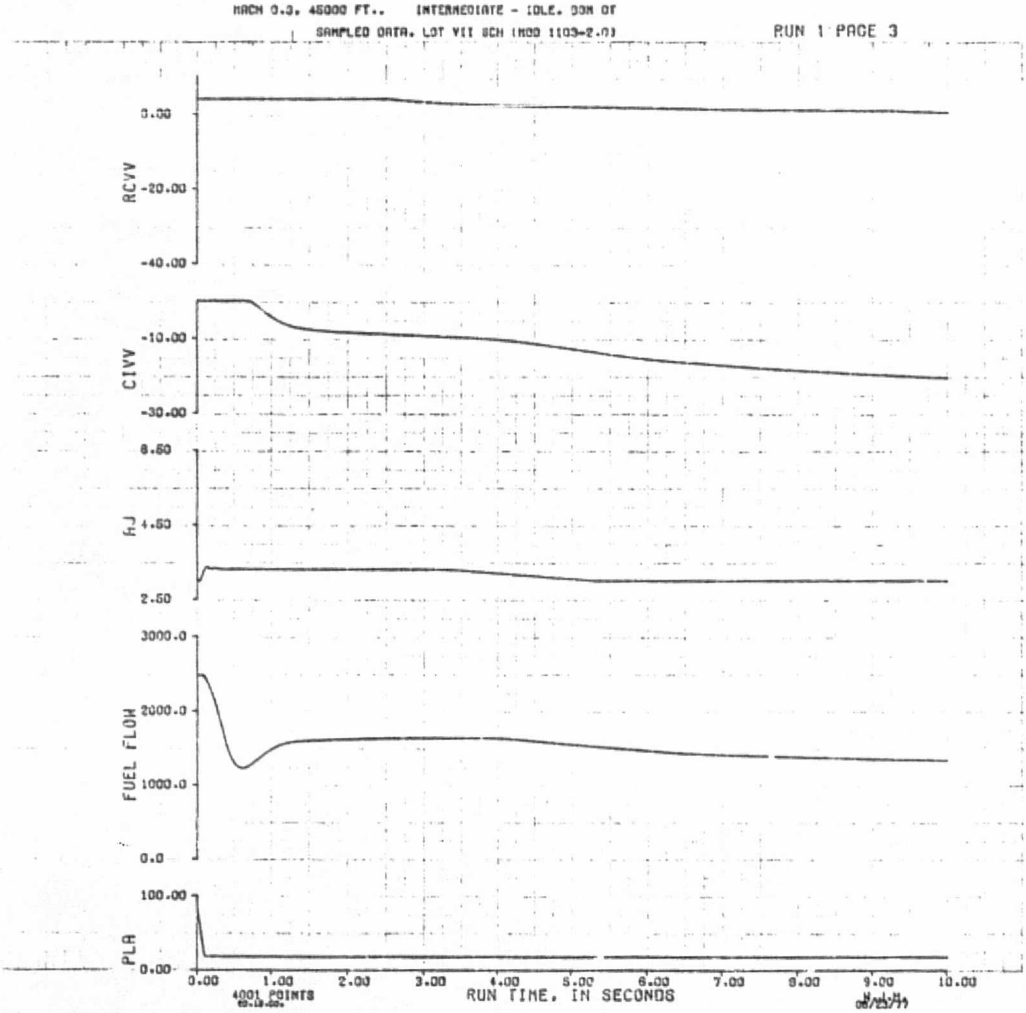
ORIGINAL PAGE IS
OF POOR QUALITY





ORIGINAL PAGE IS
OF POOR QUALITY

C-6

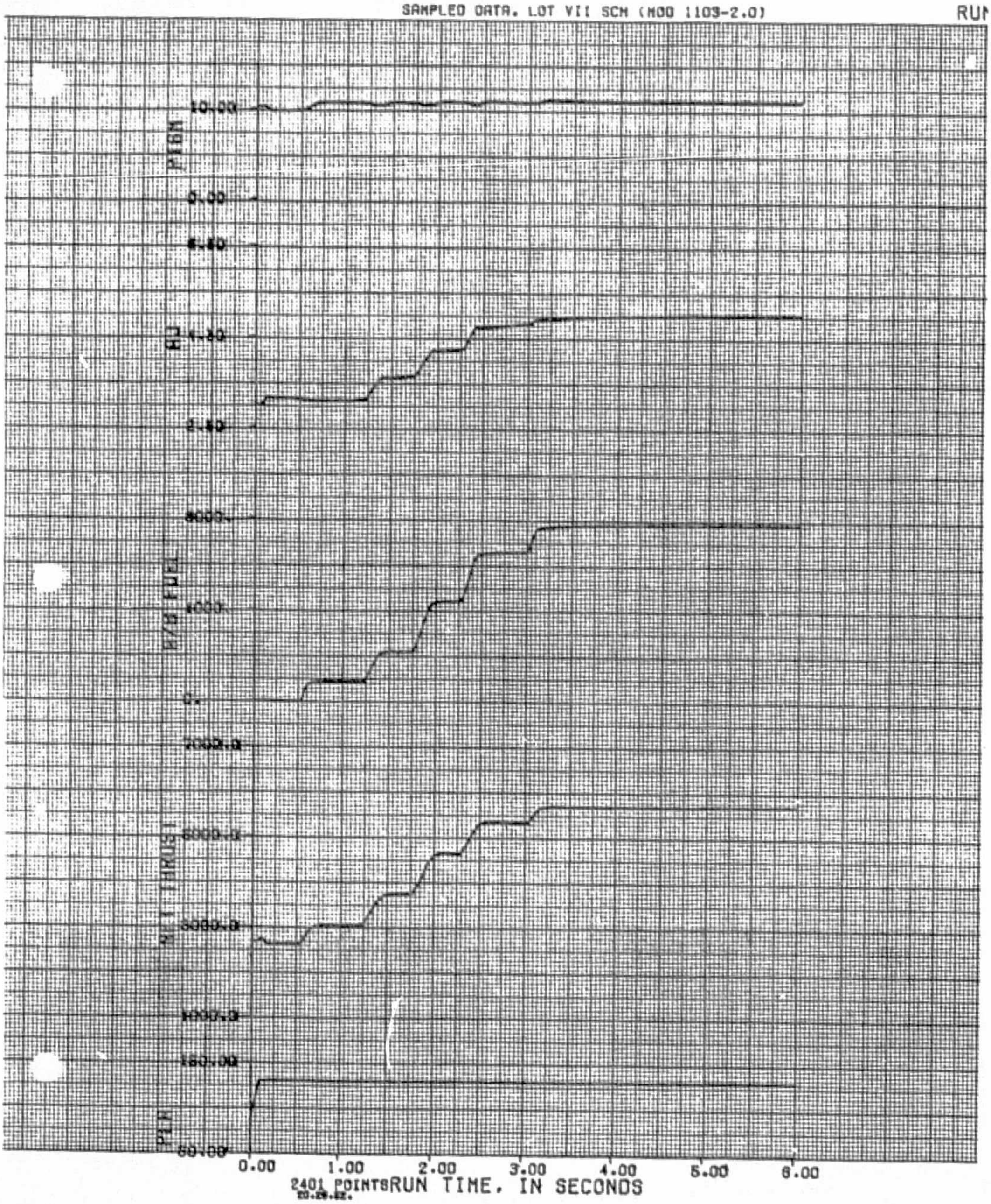


MACH 0.3, 45000 FT.. INTERMEDIATE - IDLE. 30% OT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN 1 PAGE 3
RCVV
CIVV
AJ
FUEL FLOW
PLA
4001 POINTS
RUN TIME, IN SECONDS

MACH 0.9, 45000 FT..   INTERMEDIATE - MAX. 60M DT

SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)

RUN



ORIGINAL PAGE IS
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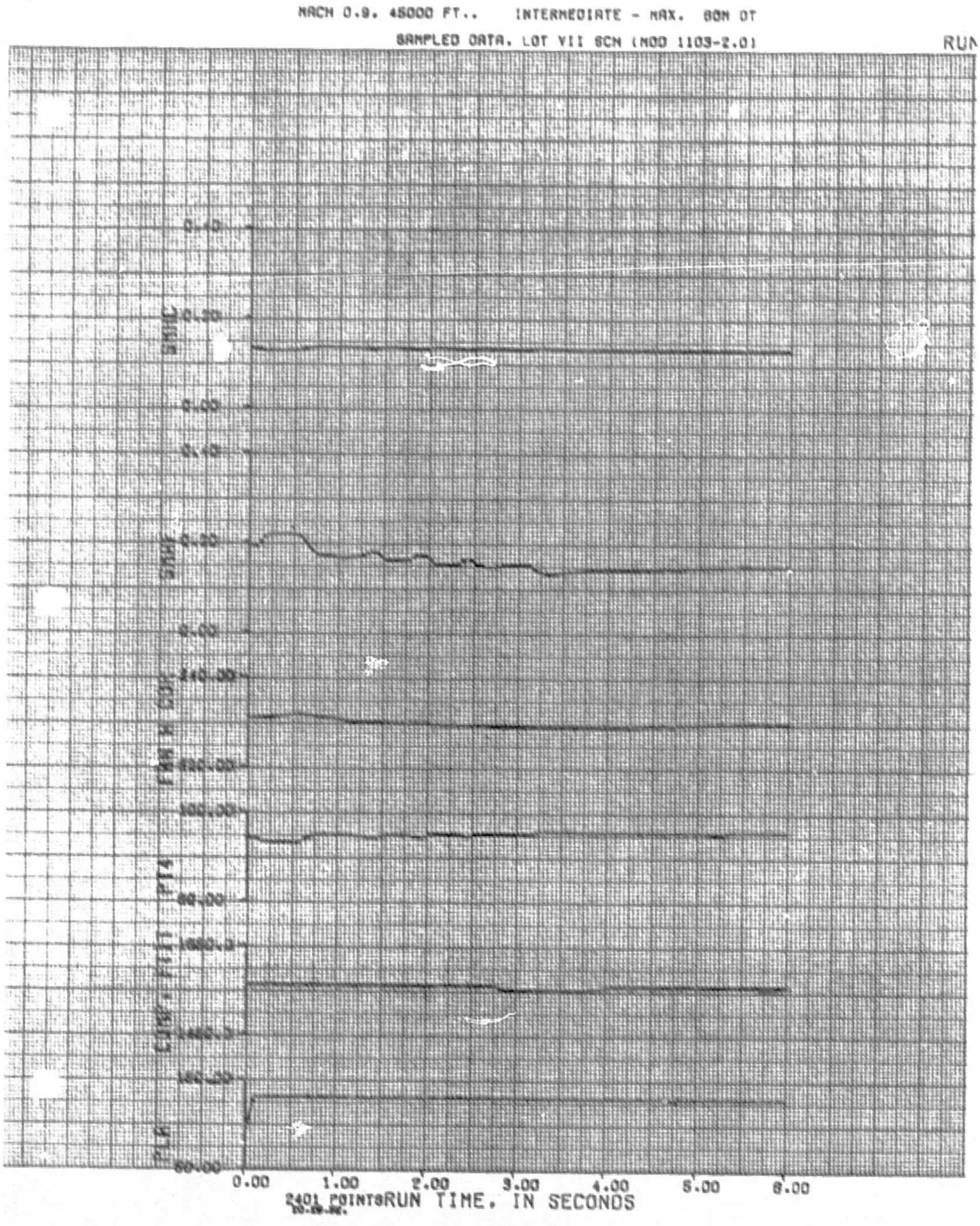
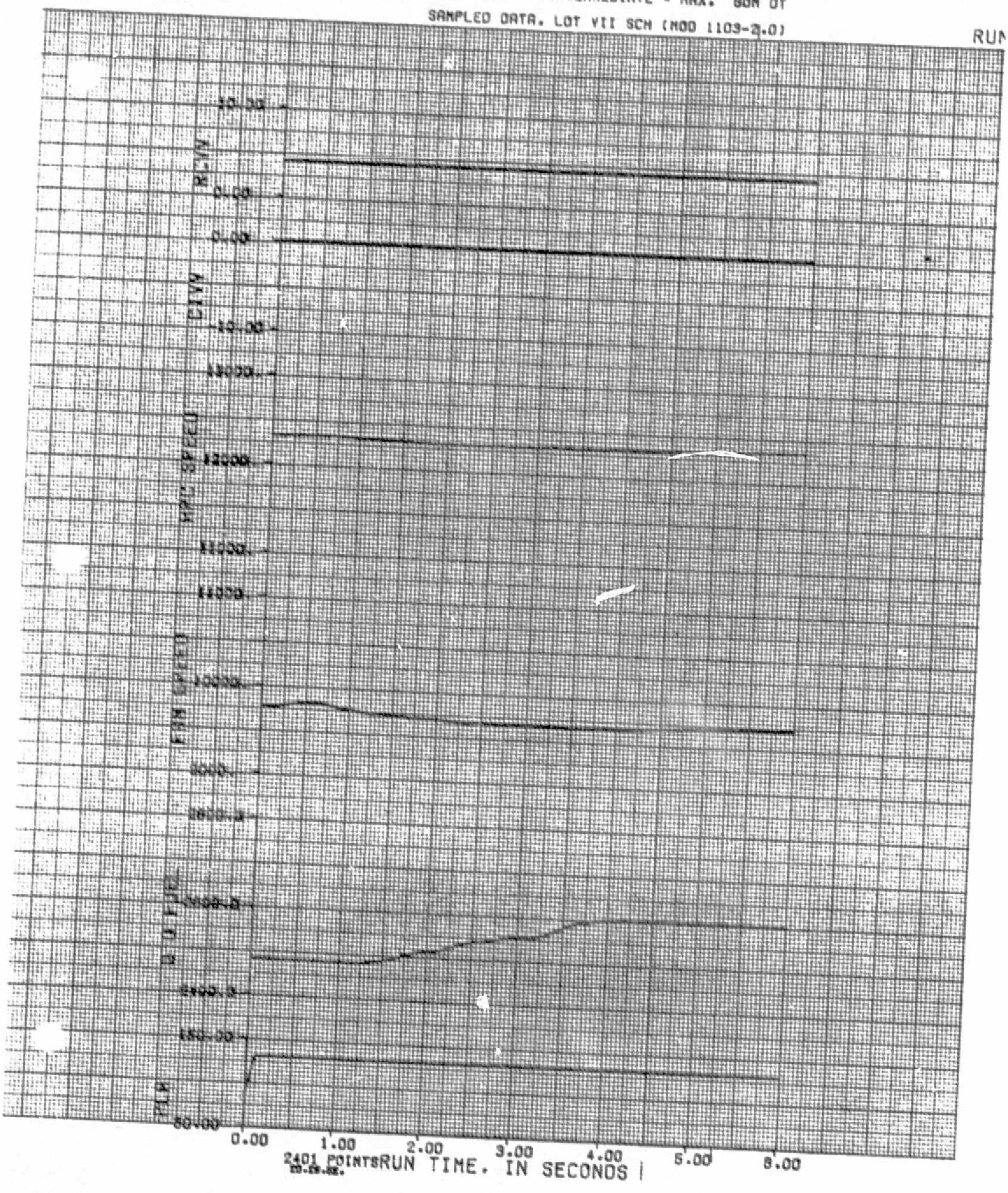
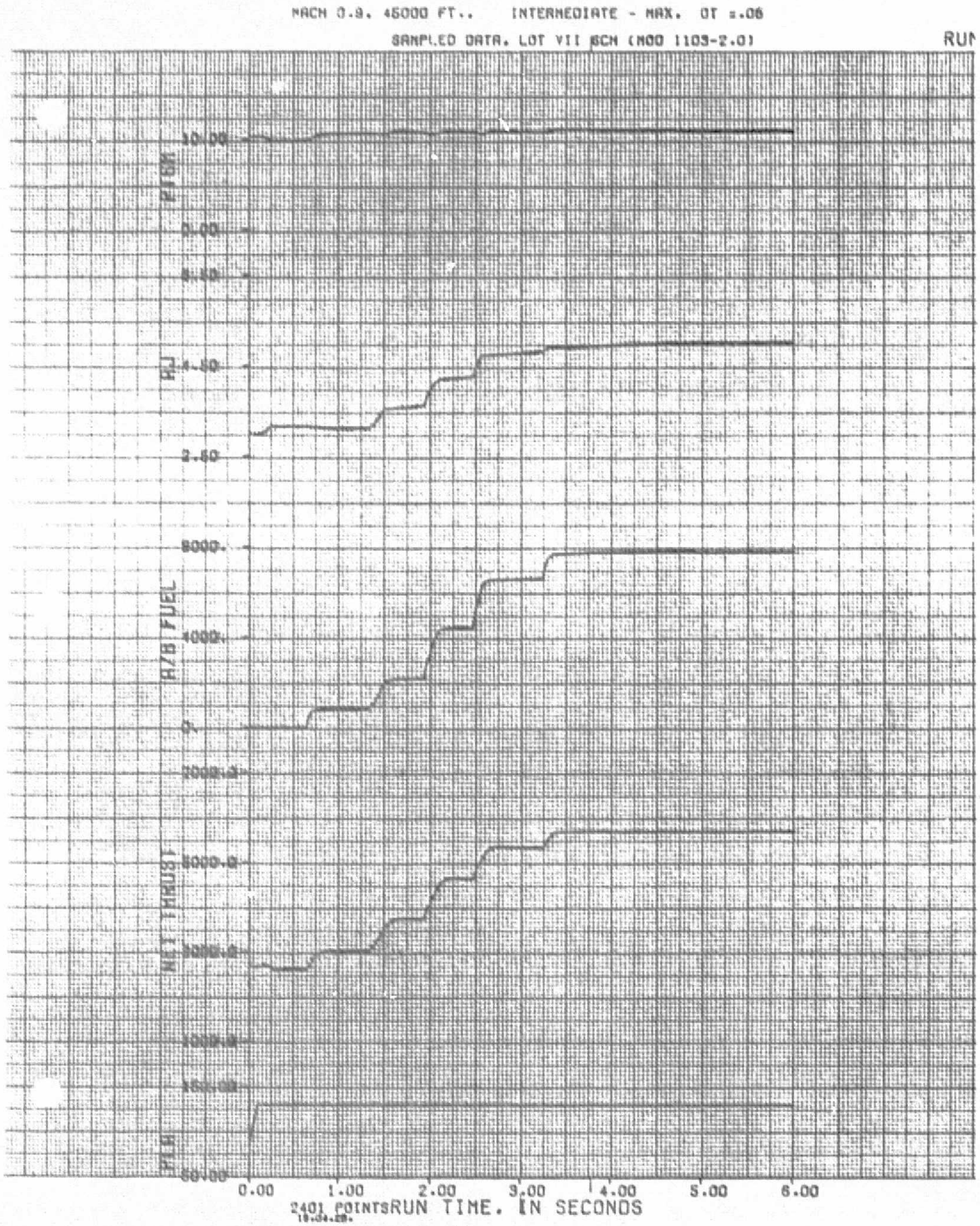


MACH 0.9, 45000 FT.. INTERMEDIATE - MAX. 80M DT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)



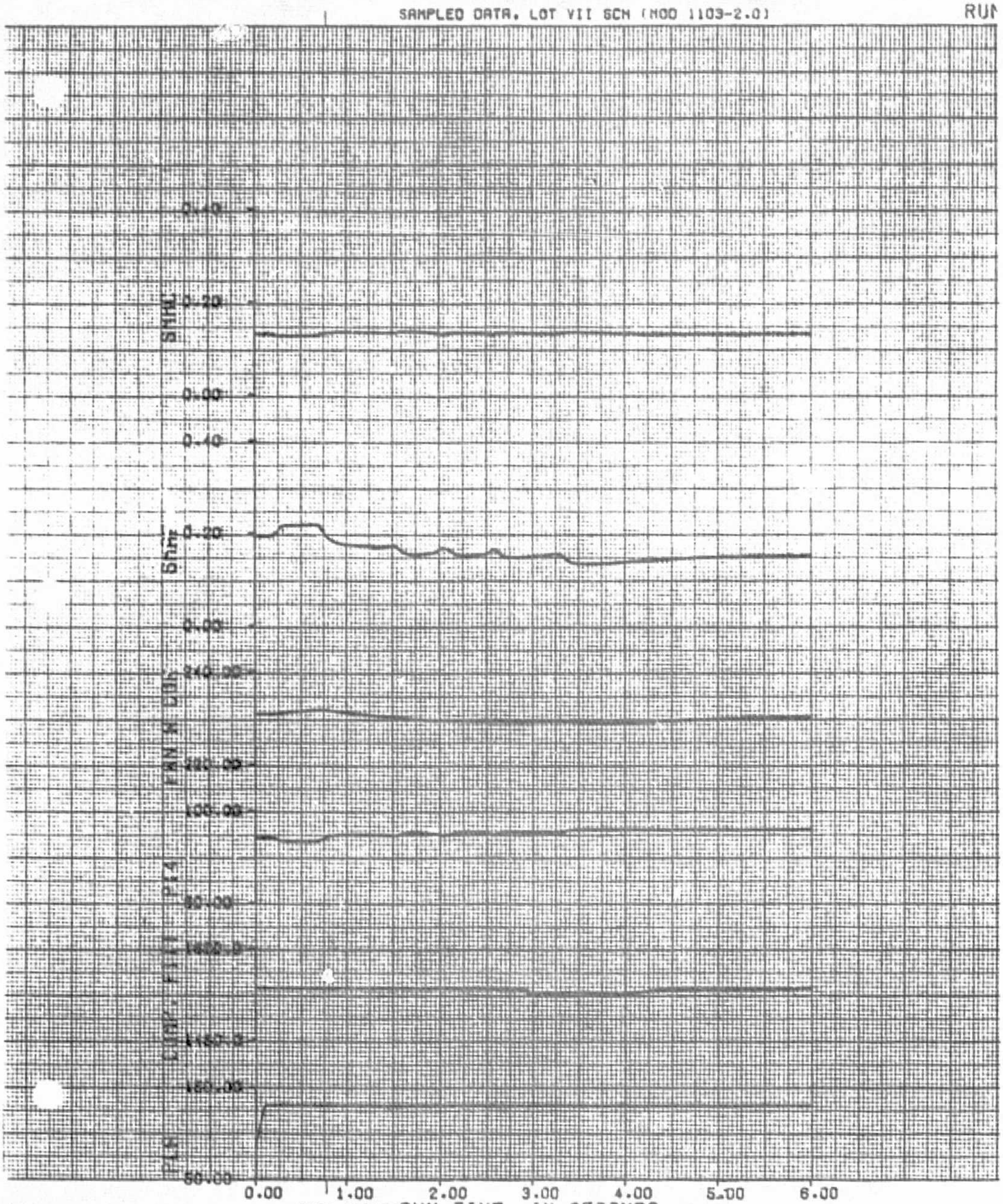
ORIGINAL PAGE IS
OF POOR QUALITY



MACH 0.9. 45000 FT.. INTERMEDIATE - MAX. DT =.06

SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)

RUN



ORIGINAL PAGE IS
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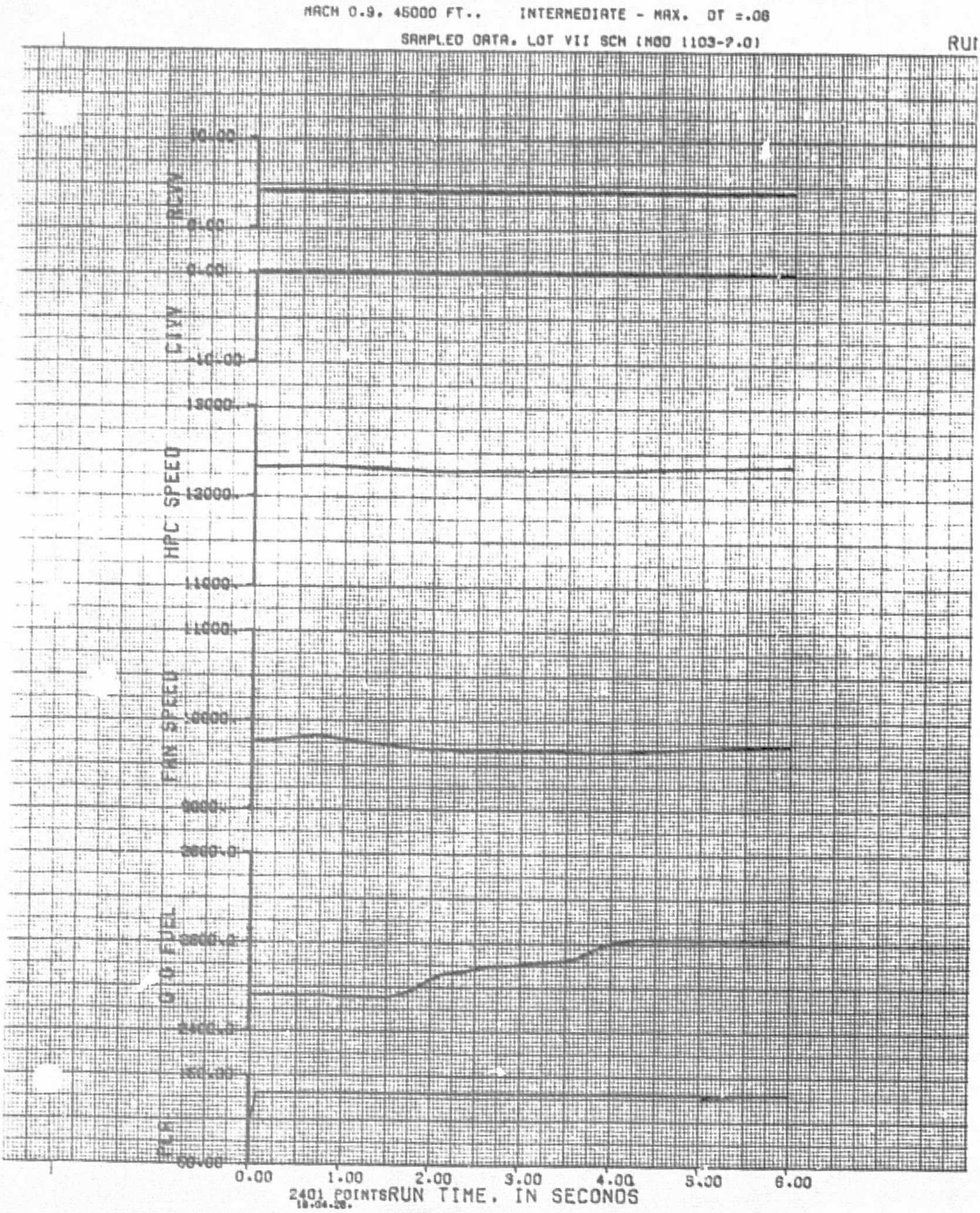
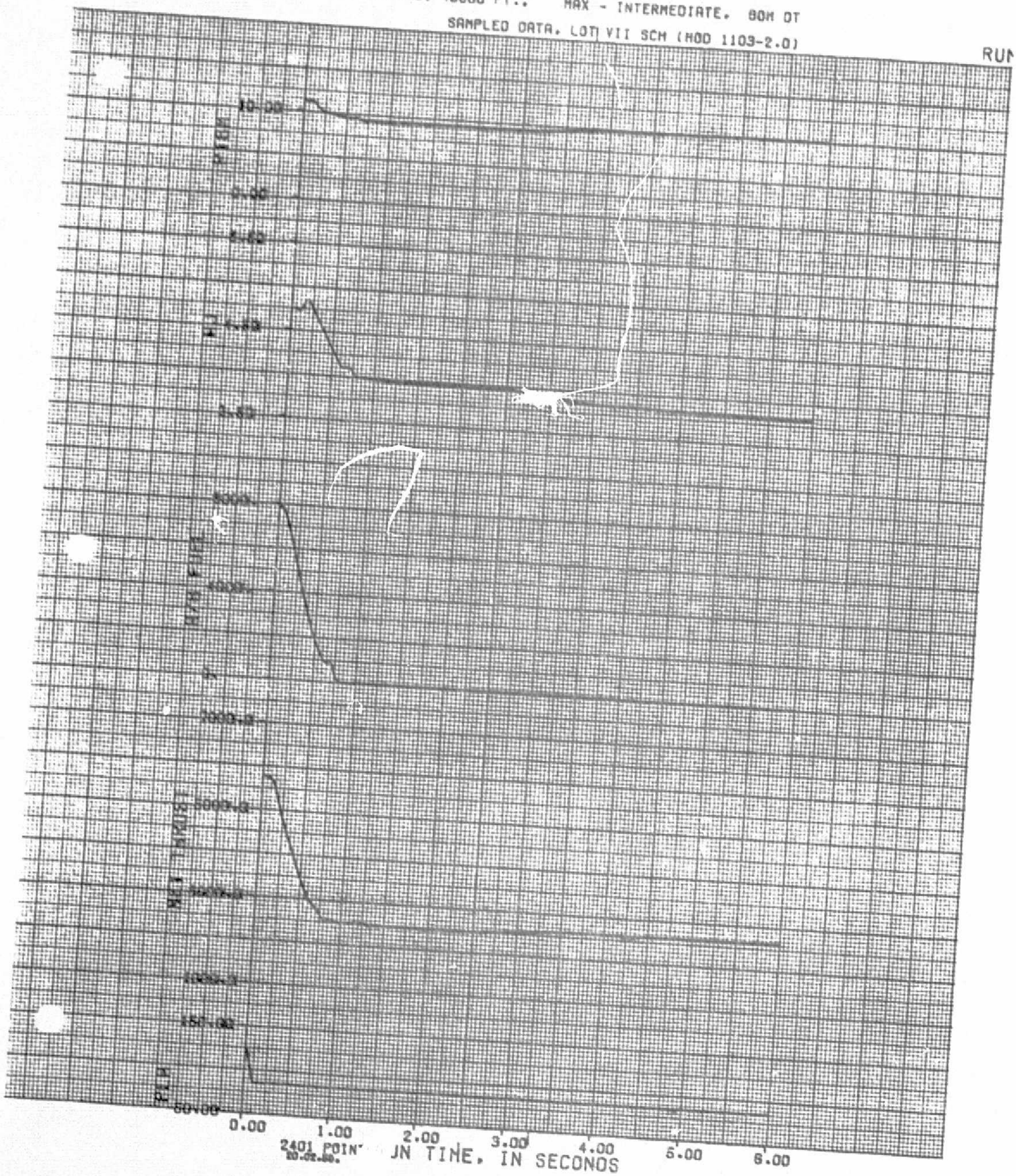
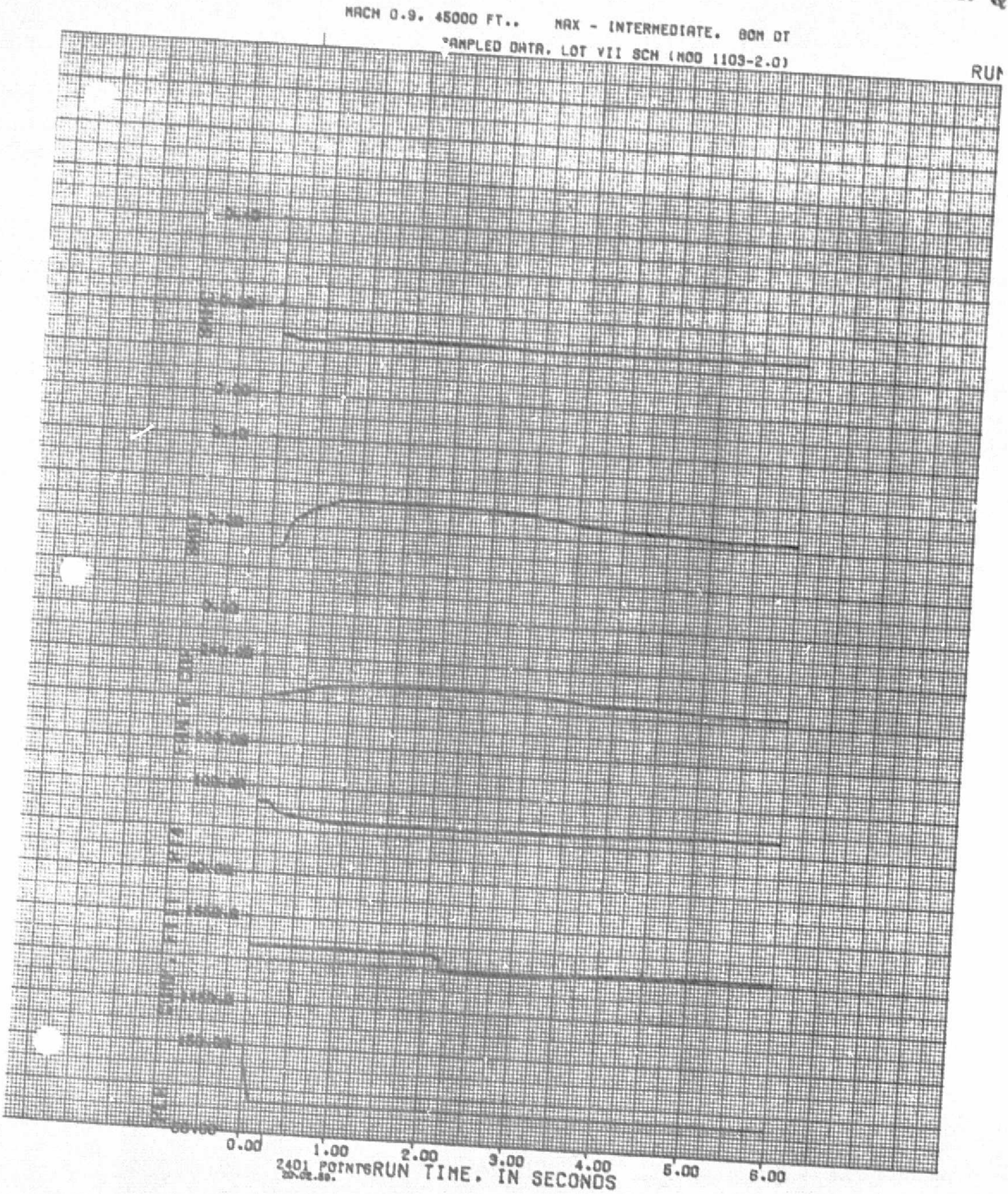


MACH 0.8. 45000 FT..   MAX - INTERMEDIATE. 80M DT

SAMPLED DATA. LOT VII SCM (MOD 1103-2.0)

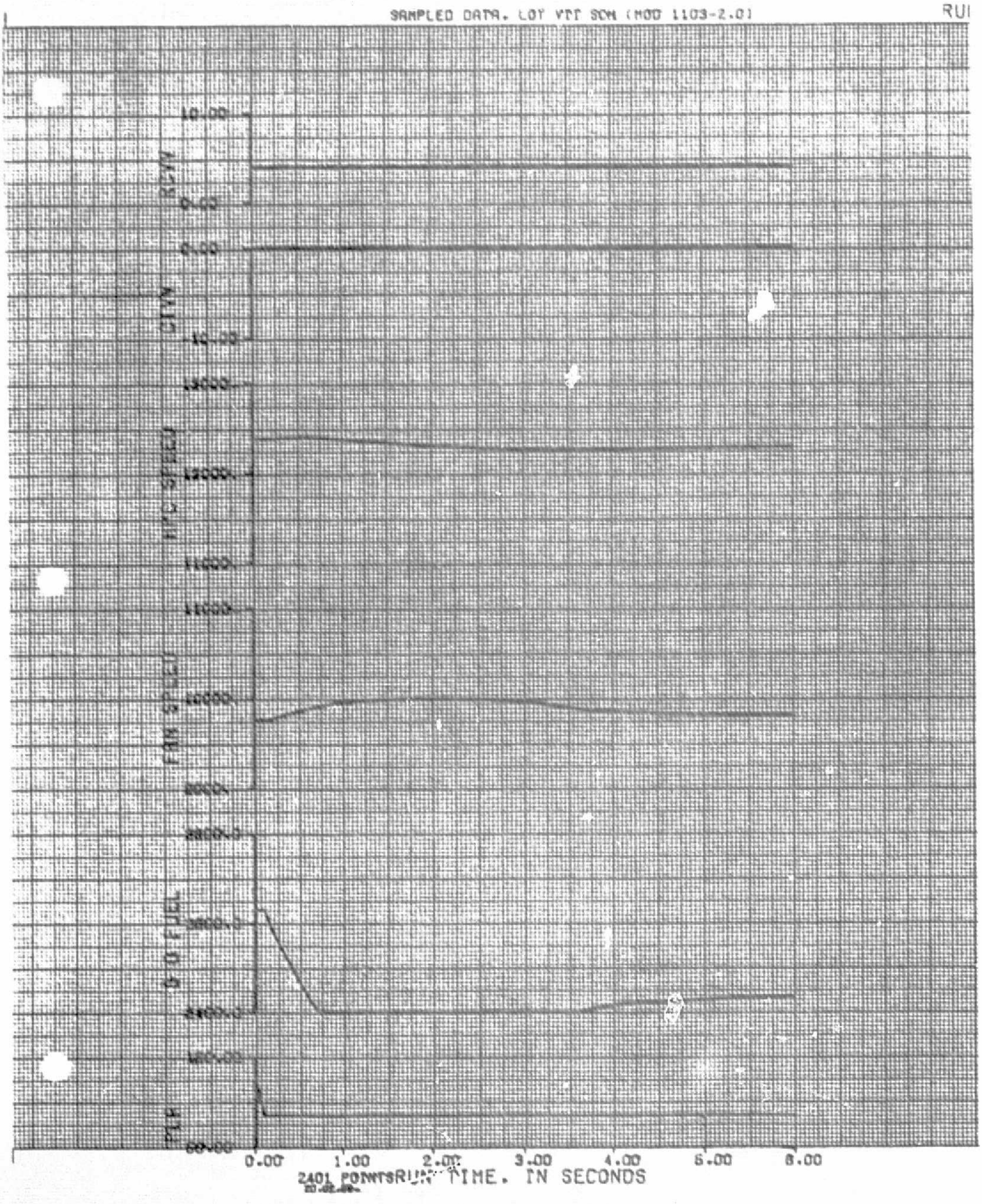


ORIGINAL PAGE IS
OF POOR QUALITY



MACH 0.9. 45000 FT.. MAX - INTERMEDIATE. 80M OT

SAMPLED DATA. LOT VTT SCH (MOD 1103-2.0)



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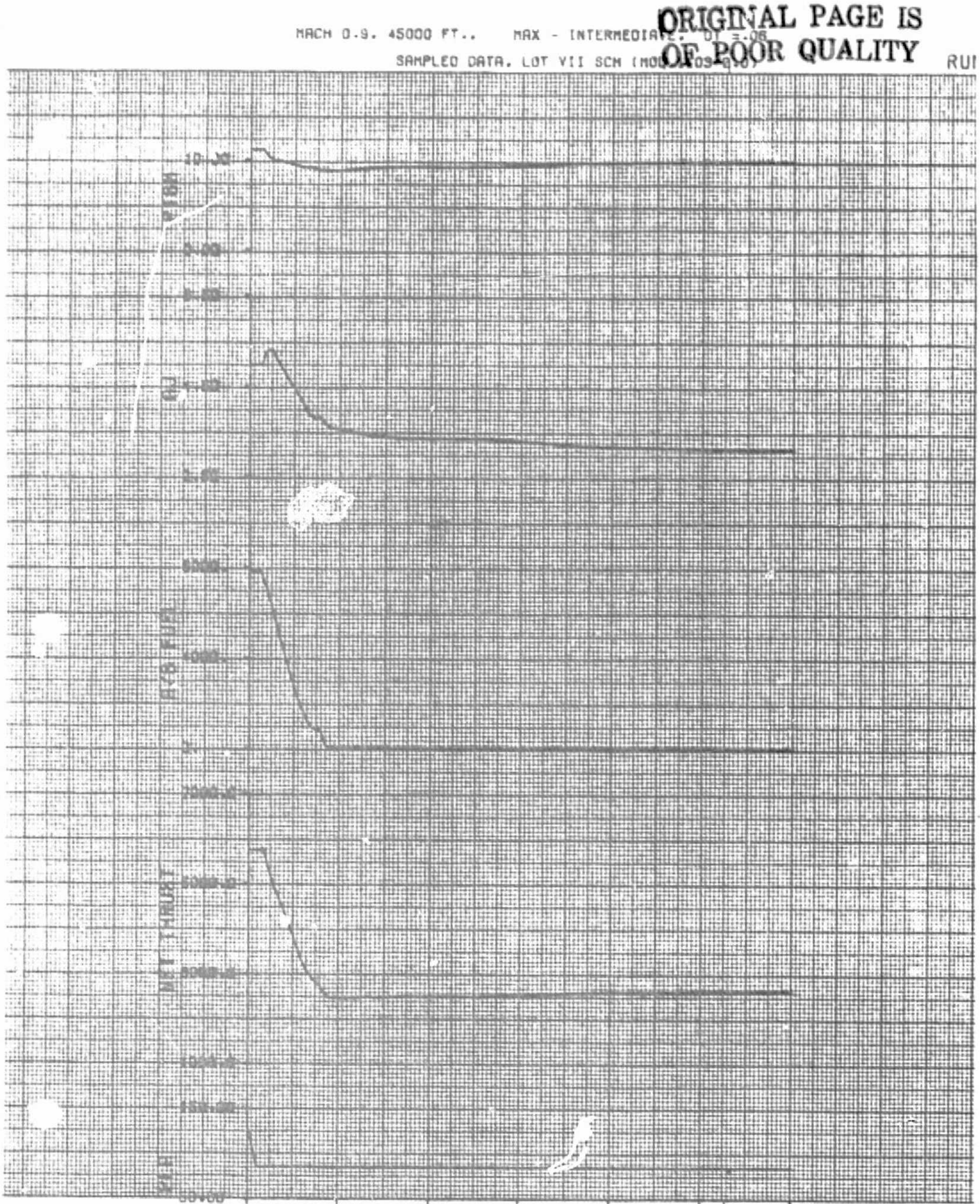
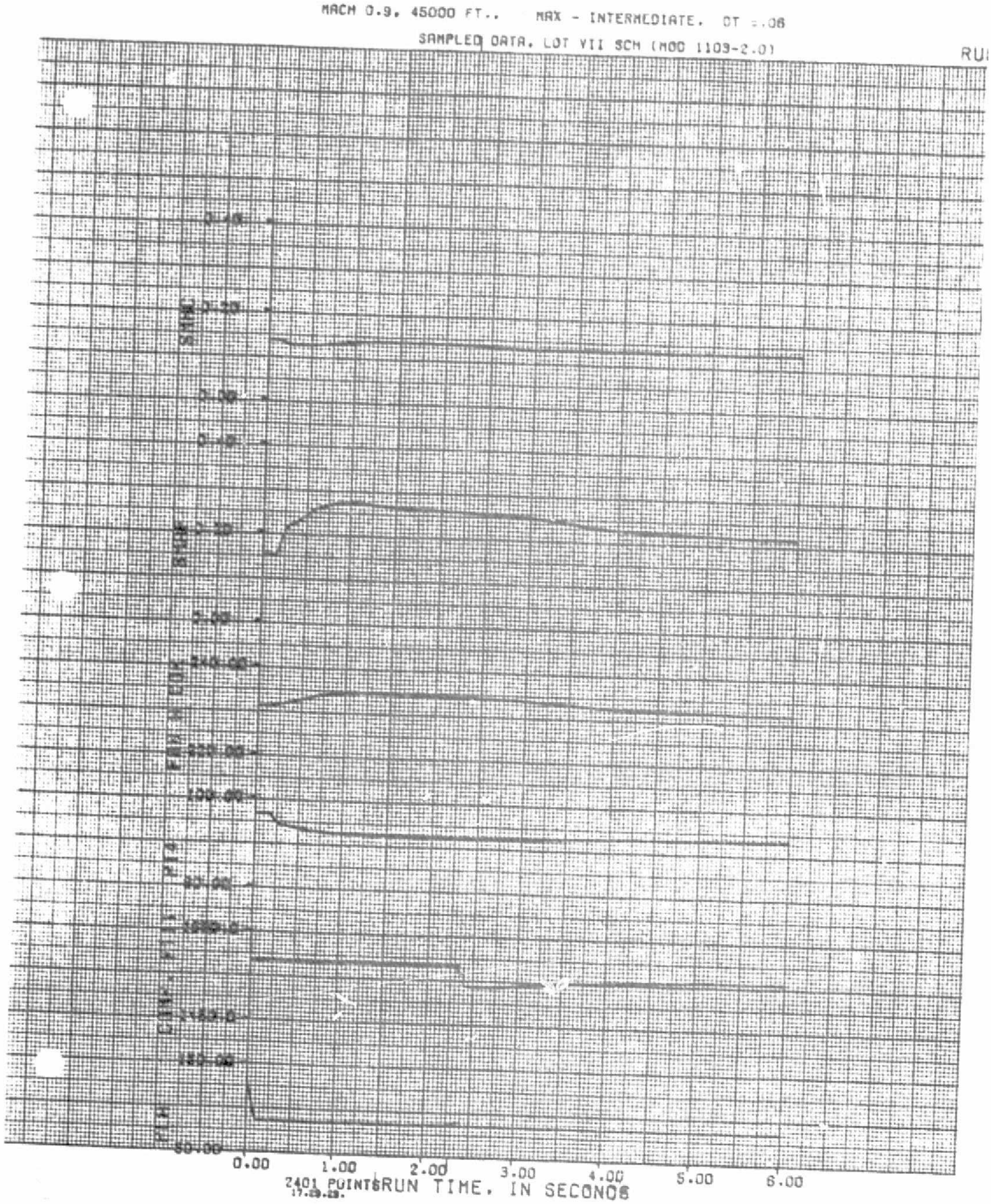
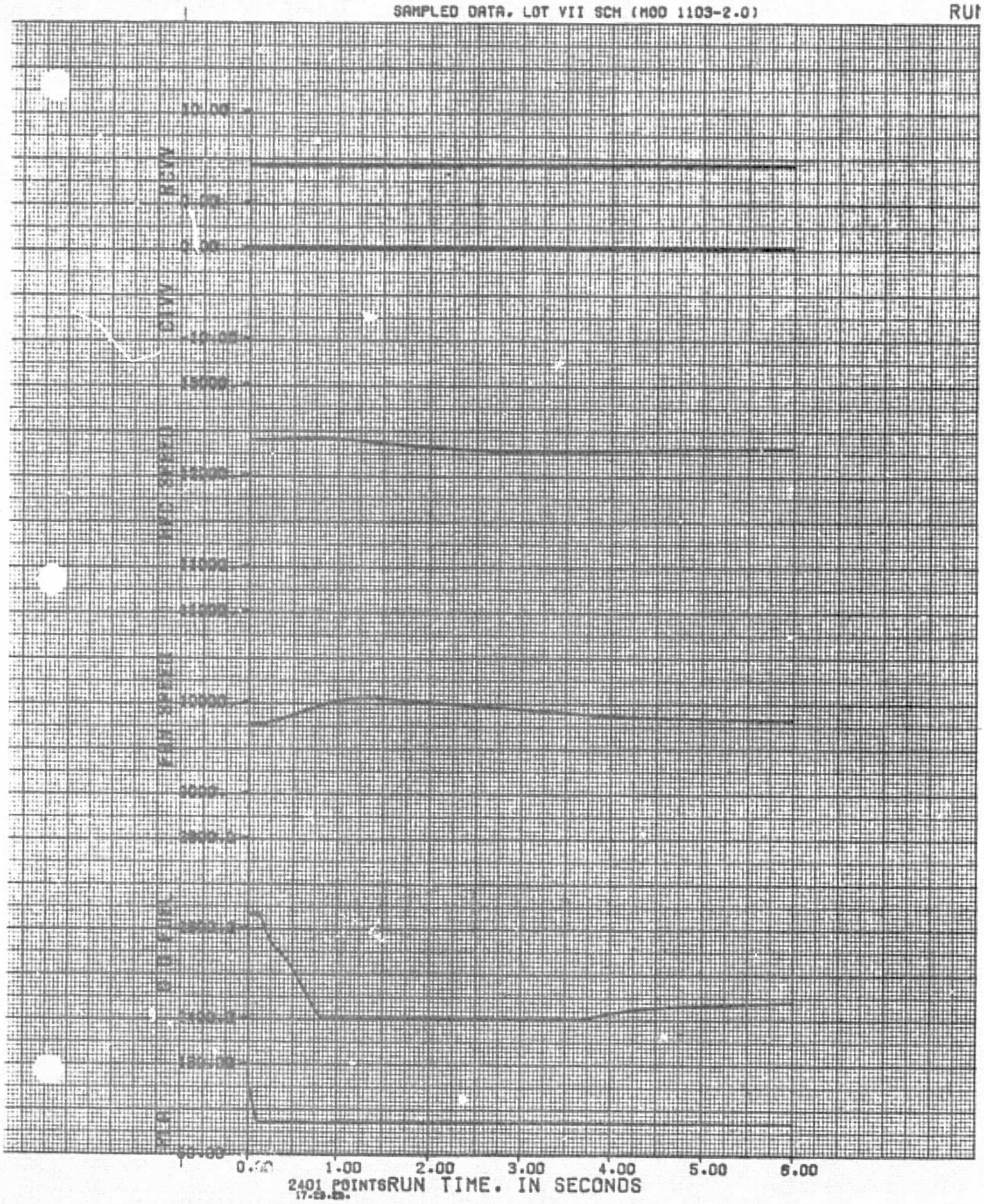


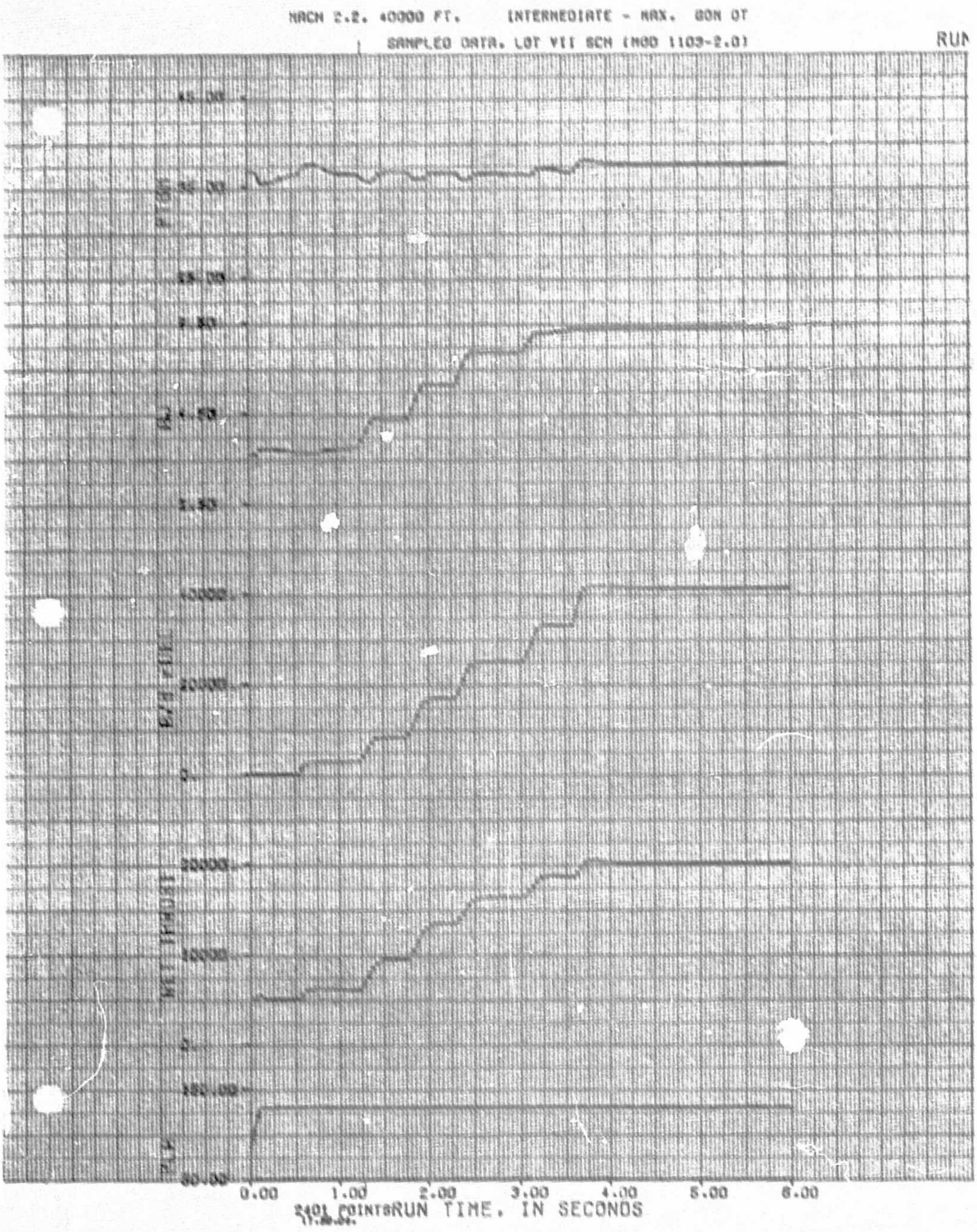

MACH 0.9, 45000 FT.. MAX - INTERMEDIATE, DT =.06
SAMPLED DATA, LOT VII SCH (MOD 1109-2.0)
RU
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS
RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY

MACH 0.9, 45000 FT.,   MAX - INTERMEDIATE, DT =.08

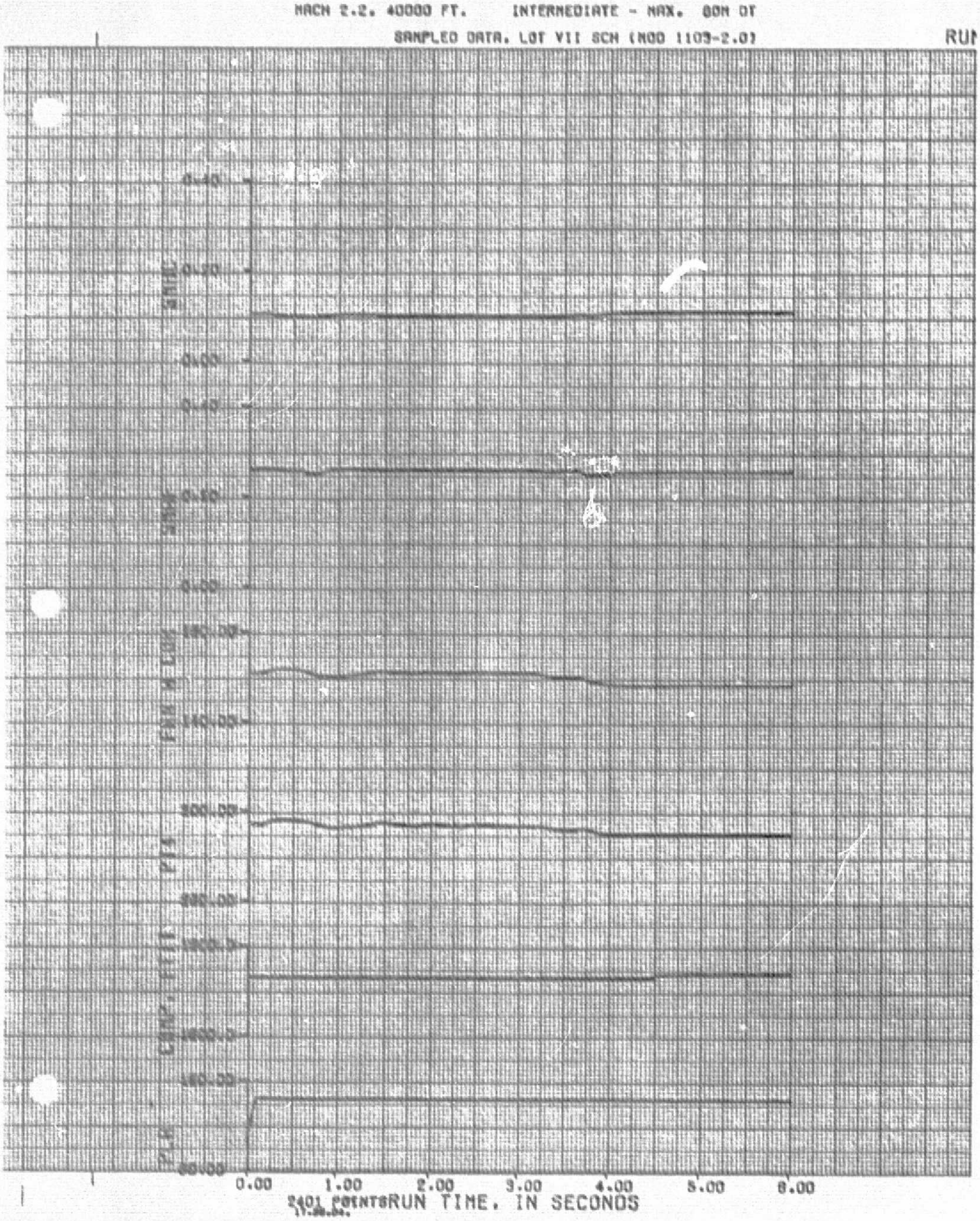
SAMPLED DATA, LOT VII SCM (MOD 1103-2.0)   RUN

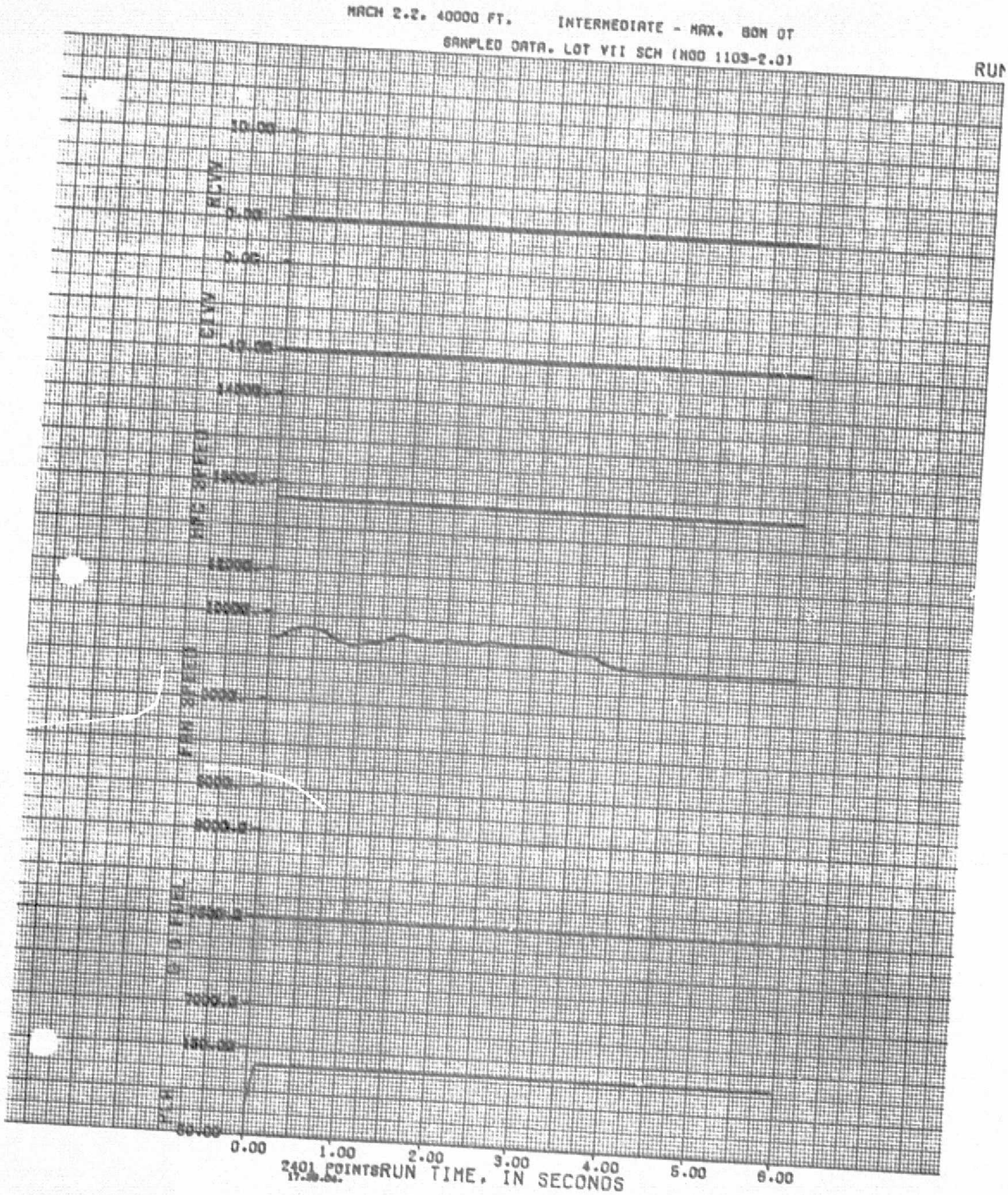




MACH 2.2, 40000 FT. INTERMEDIATE - MAX. GOV OT
SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)
RUN
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY



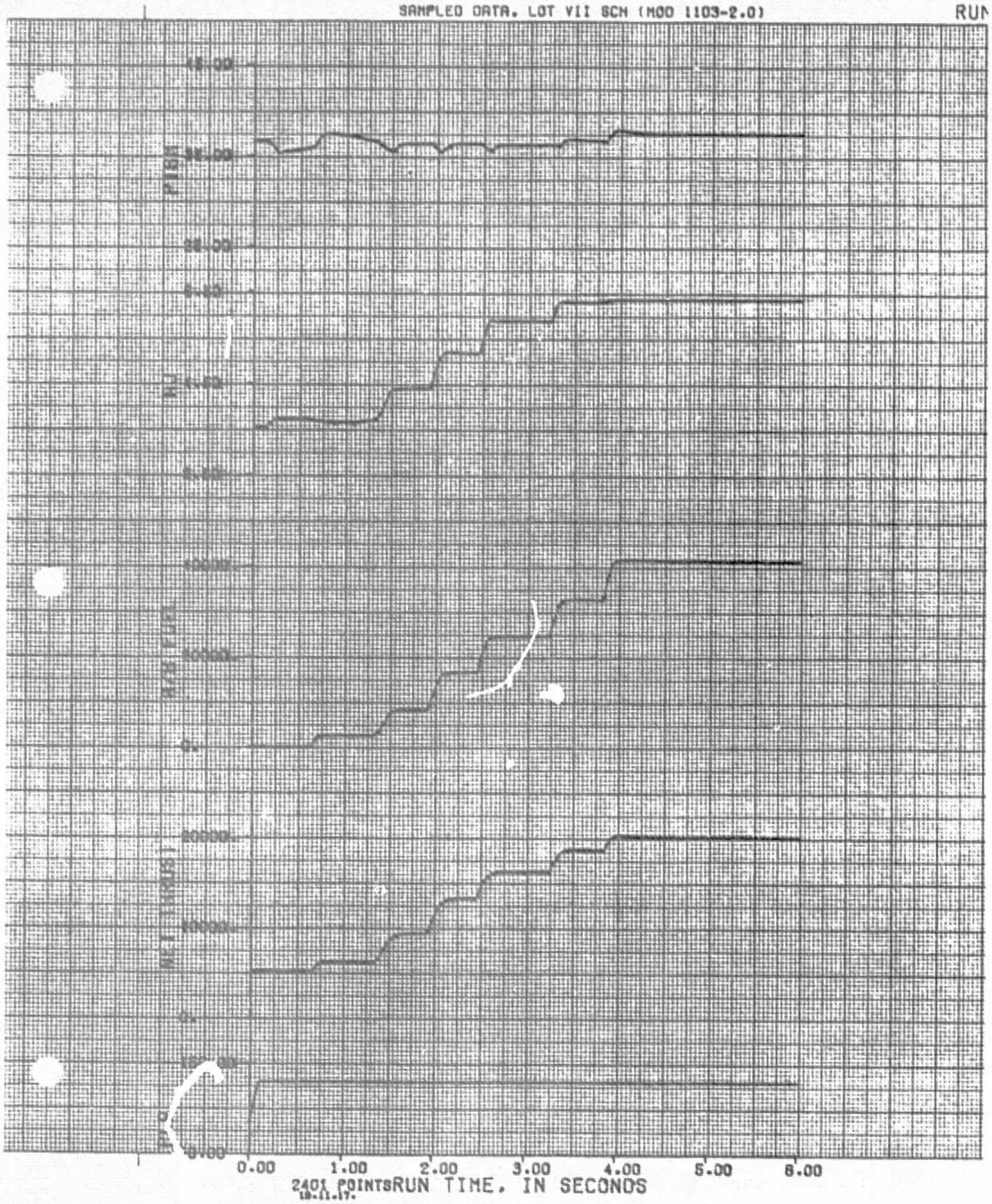

MACH 2.2, 40000 FT.   INTERMEDIATE - MAX. BOM OT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUN
2401 POINTS
RUN TIME, IN SECONDS
0.00
1.00
2.00
3.00
4.00
5.00
6.00

ORIGINAL PAGE IS OF POOR QUALITY

MACH 2.2, 40000 FT. INTERMEDIATE - MAX. DT = .06

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)

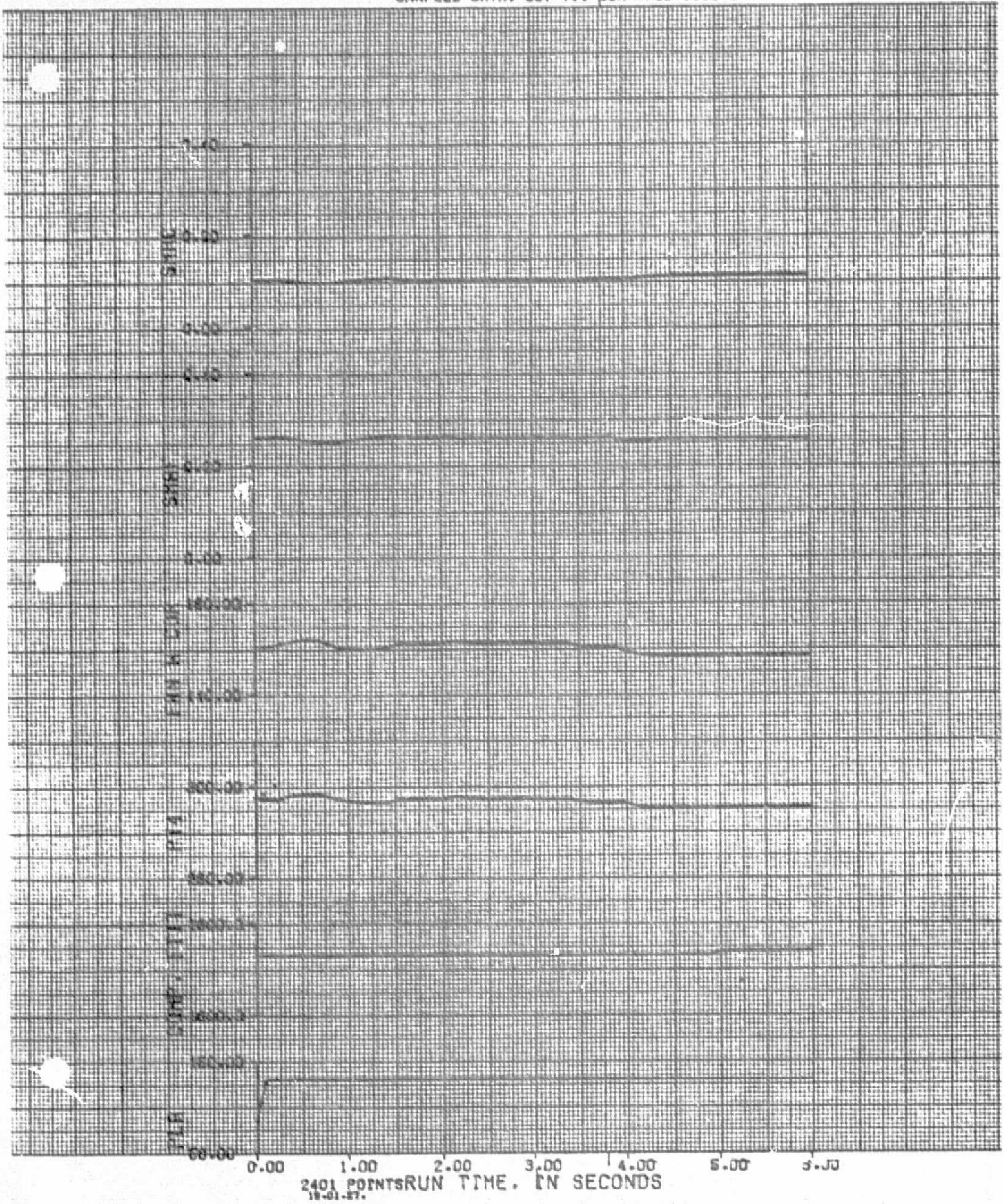
RUN



MACH 2.2, 40000 FT.   INTERMEDIATE - MAX. DT =.06

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)

RUN



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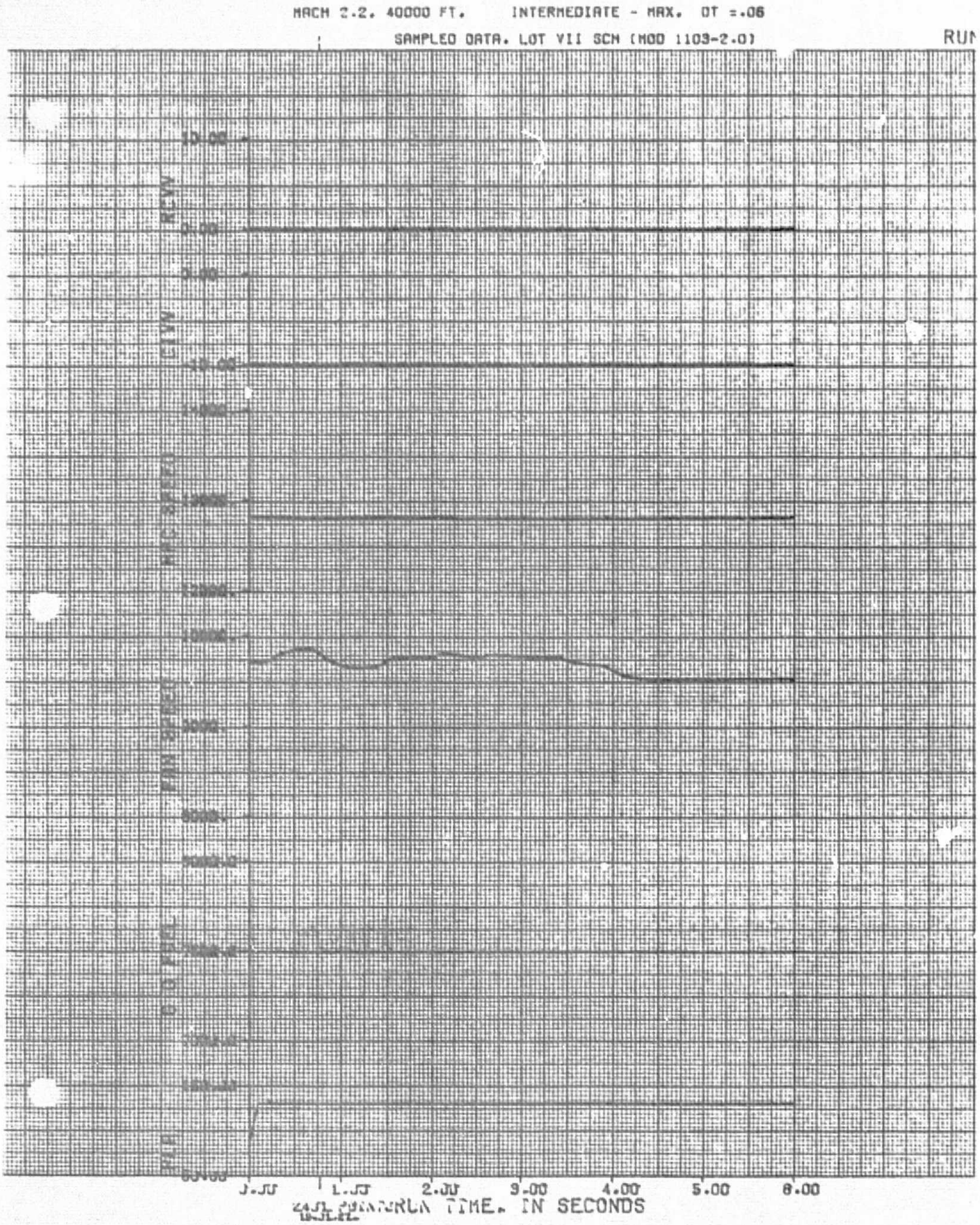
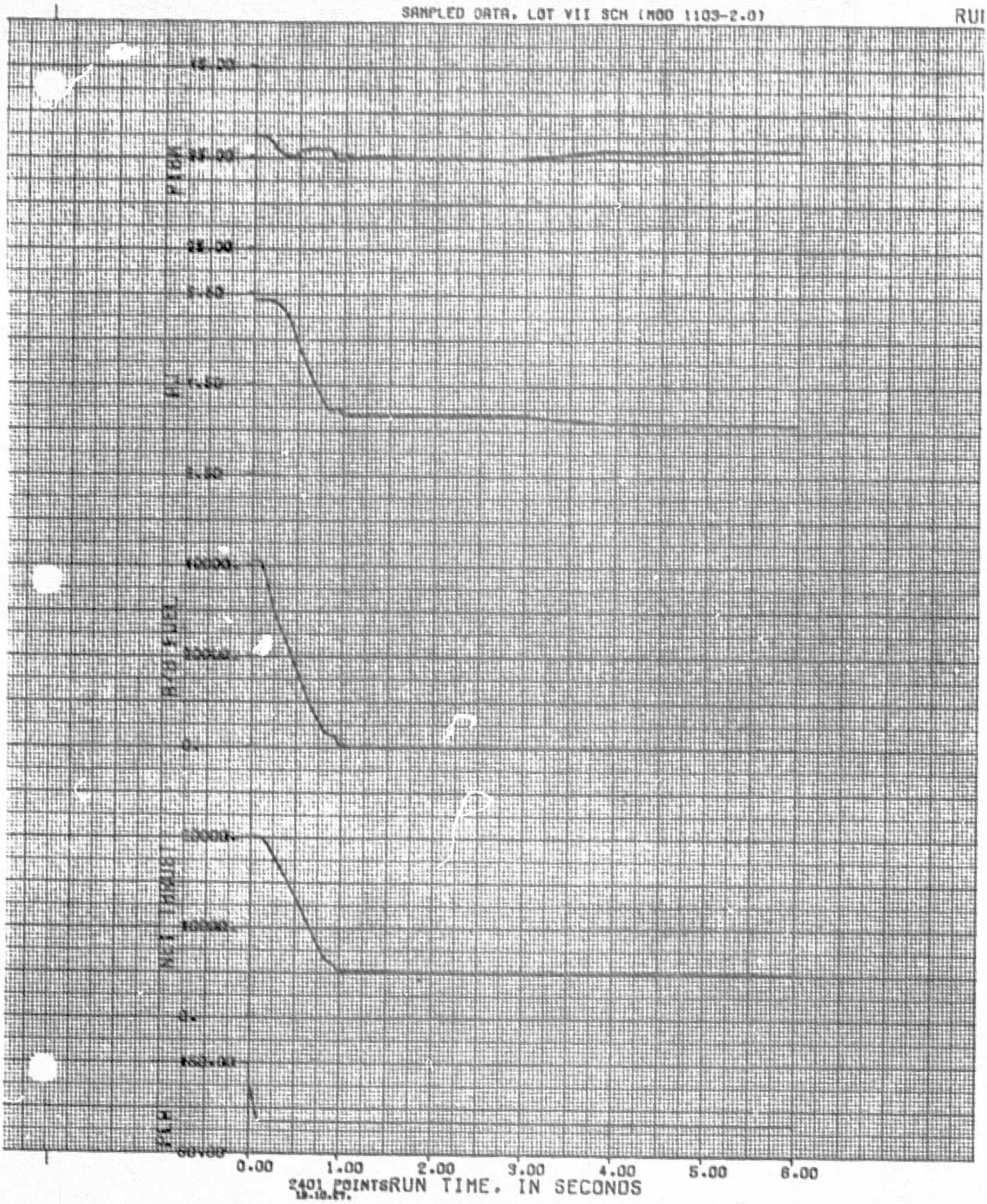


MACH 2.2, 40000 FT.   MAX - INTERMEDIATE. BOM OT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)



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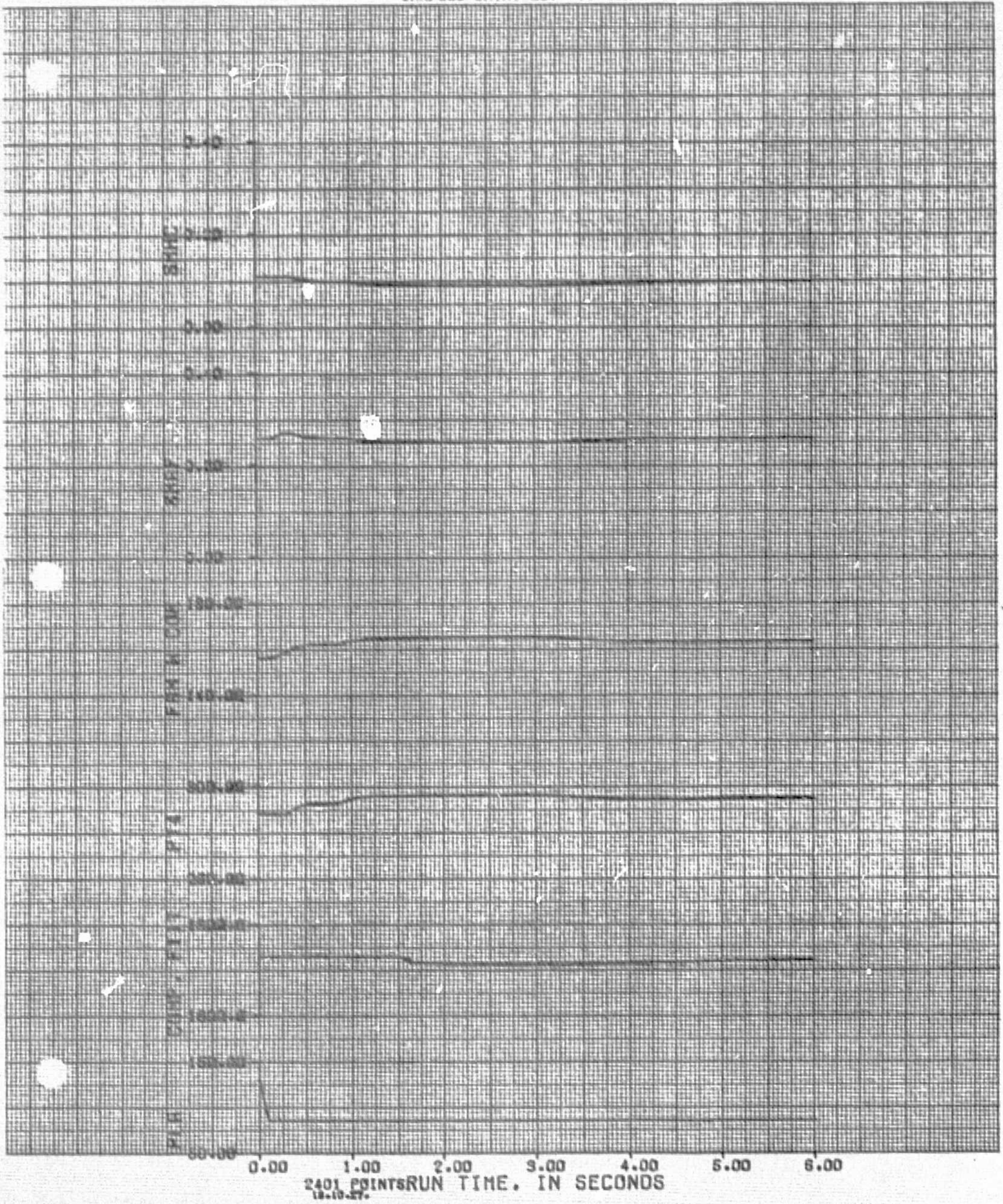
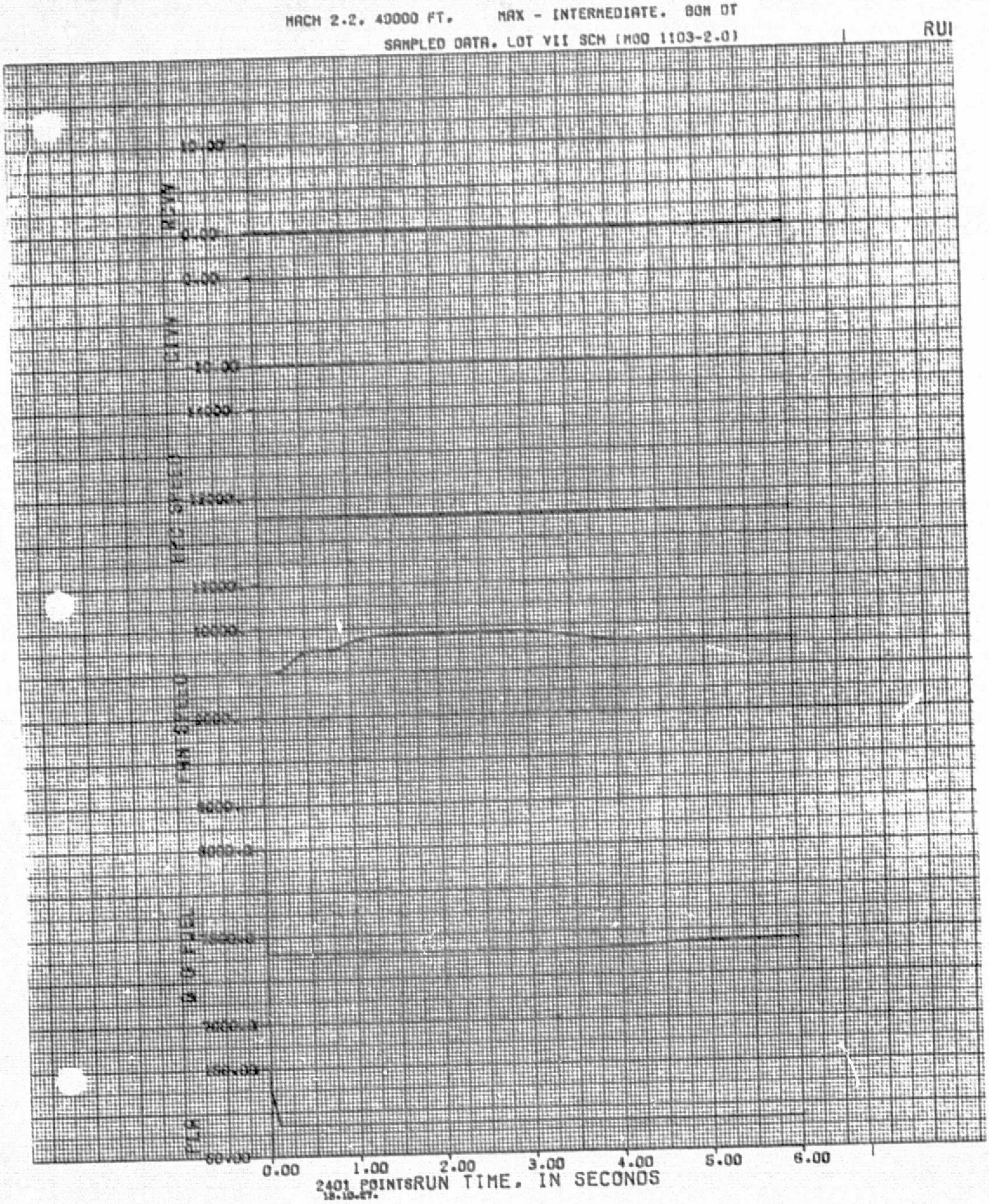
MACH 2.2, 40000 FT. MAX - INTERMEDIATE, 80M DT

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)

RU

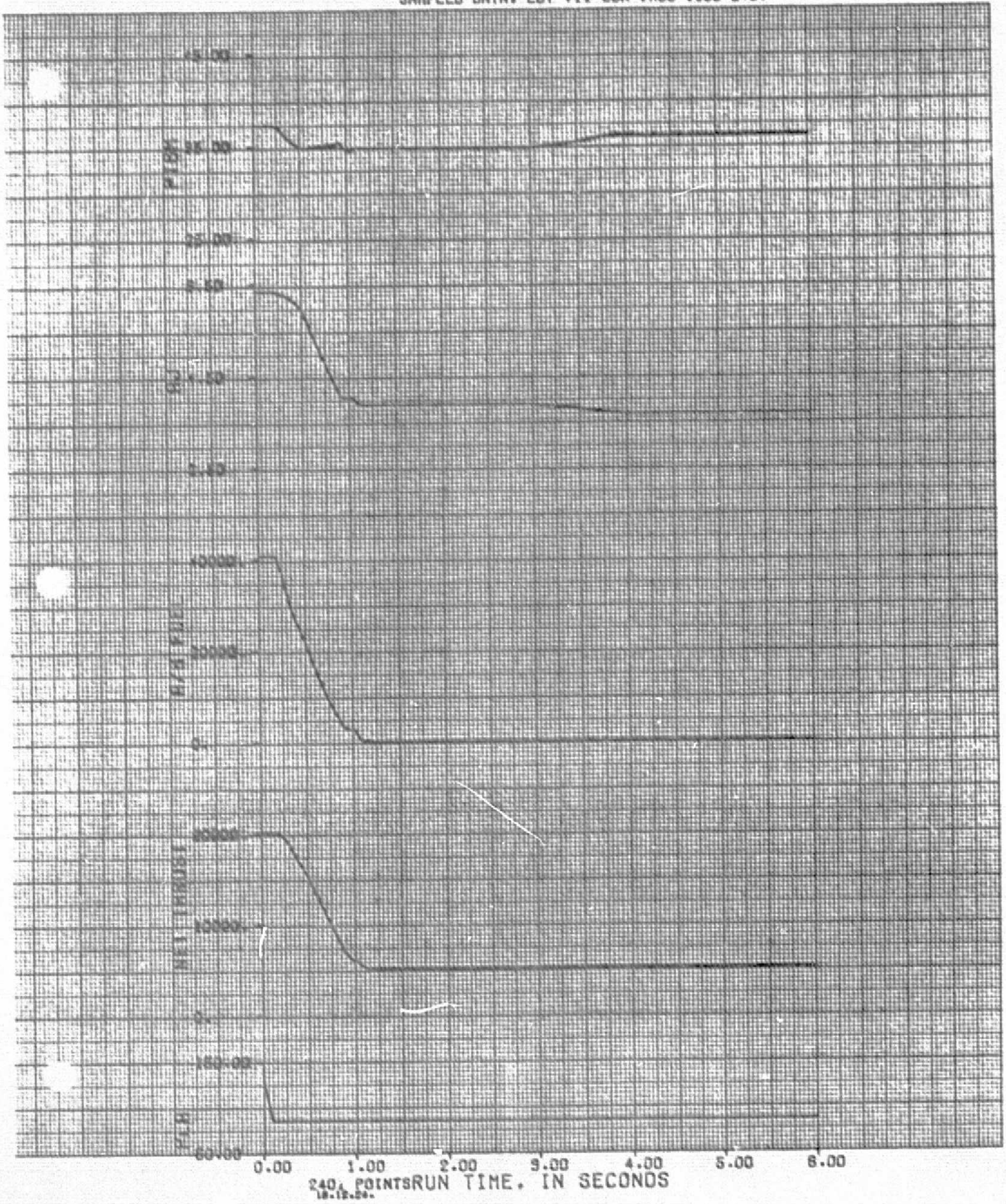



MACH 2.2, 40000 FT.   MAX - INTERMEDIATE. BOM DT
SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)
RUI
0.00
1.00
2.00
3.00
4.00
5.00
6.00
2401 POINTS RUN TIME, IN SECONDS

ORIGINAL PAGE IS
OF POOR QUALITY

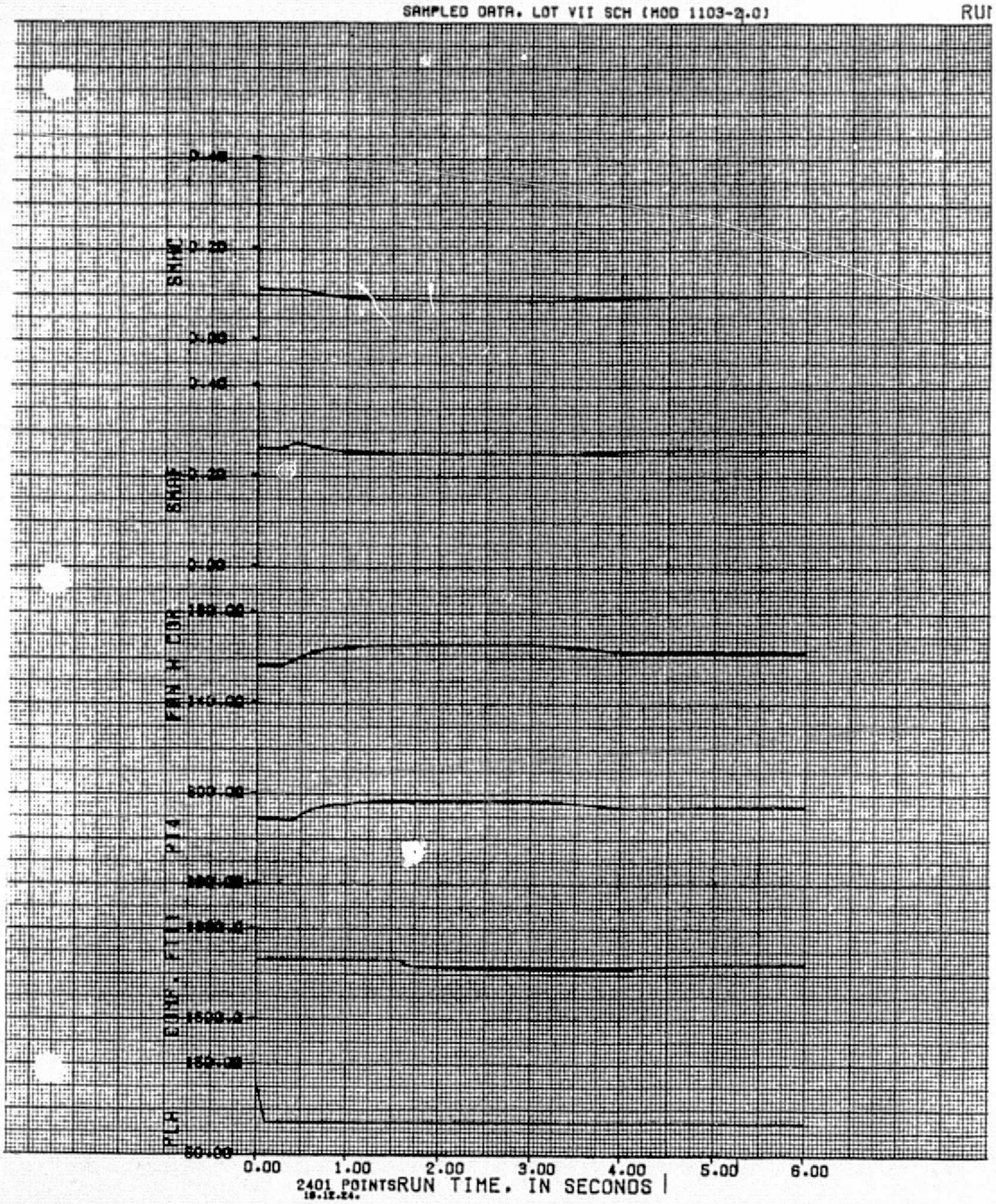
MACH 2.2. 40000 FT. MAX - INTERMEDIATE. DT =.06

SAMPLED DATA. LOT VII SCH (MOD 1103-2.0)



MACH 2.2, 40000 FT.   MAX - INTERMEDIATE. DT =.08

SAMPLED DATA, LOT VII SCH (MOD 1103-2.0)   RUN



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OF POOR QUALITY